Low-Voltage Class AB Operational Amplifier

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Abstract

This paper presents a CMOS low-voltage operational amplifier, which uses a minimum selector circuit to control the class AB operation of the output stage. The operational amplifier basic characteristics are analyzed and simulated using the SMASH 4.0 simulator with the ACM model of the MOSFET. The supply voltage is 1.5V and the total quiescent current is 4.5μA for a unity-gain frequency of 1MHz. This design is being integrated on the AMS 0.8μm CMOS technology. The operational amplifier presented here offers a competitive design choice for low-power low-voltage circuits.

1. Introduction

In the last years many efforts have been made for the reduction of both the supply voltage and the power consumed by the CMOS circuits [1], mainly due to the increasing use of portable equipment. The correct operation of analog circuits at low-voltage demands to explore new blocks and new circuits topologies. For analog circuits, the operational amplifier (opamp) is one of the most useful blocks. The opamp is usually made up of two gain stages, namely, the differential input stage and the output stage. In this paper, we will place more emphasis on the output stage due to its high current, demanded by the resistive nature of the load. In class A output stages, the maximum current is equal to the bias current. Class B output stages combine high output current capability with very low quiescent current but introduce crossover distortion. The common-source class AB stage, Fig. 1(a), presents a good trade-off between distortion and quiescent dissipation. The output transistors are biased with a small quiescent current compared to the maximum output current, which reduces crossover distortion in comparison with class B output stage. Furthermore, a minimum current in the output transistors, for any bias condition, prevents a turn-on delay of the non-active transistor and, thus, crossover distortion [7].

In Fig. 1(b) we can observe the ideal characteristic of a class AB amplifier. The quiescent current I_Q is slightly higher than the minimum current I_{min}. The maximum source and sink currents depend on both the supply voltage and the dimensions of the transistors.

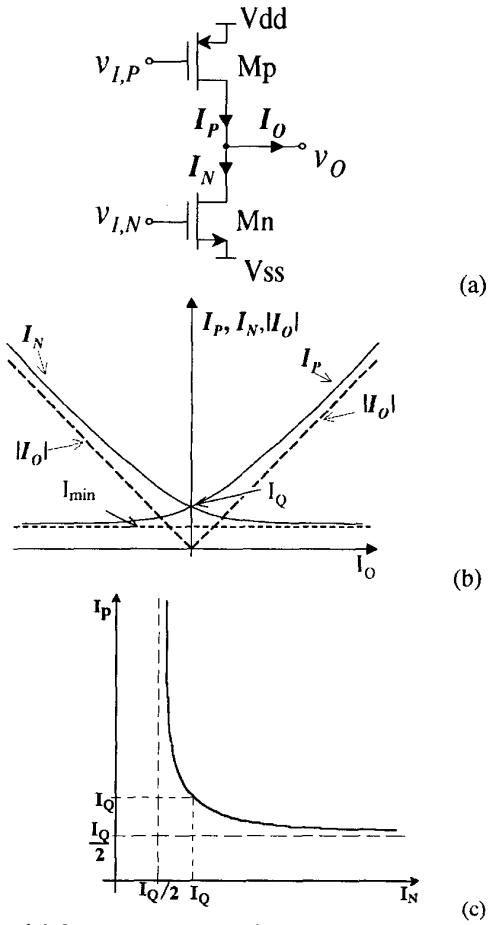

Fig. 1: (a) Common-source class AB stage. (b) Ideal characteristic for class AB stage. (c) Non-linear function for class AB control.

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In this work, an opamp with class AB output is proposed. The amplifier structure is very simple, its power consumption is low, and it can operate with supply voltages down to 1.5V. The class AB control block is composed of a translinear circuit, whose analysis and experimental results are presented in section 2. The operation of the opamp together with simulation results are shown in section 3. This opamp is intended to operate in a S/H circuit and should be capable of driving resistive loads.

2. Minimum current selector circuit

To obtain the class AB control of the output stage, a non-linear function such as the one in Fig. 1(c) is necessary and can be accomplished by a translinear MOS circuit [4]. There are several forms to implement the characteristic represented in Fig. 1(c) [4-6]. One of them, based on the minimum current selector circuit of Fig. 2 [4], was used in this work. For the analysis of the circuit in Fig. 2, assume that all transistors have the same dimensions. When I_N is much larger than I_B, transistor M1 operates in the linear region; consequently, $V_{GSM2} \approx V_{GSM3}$ and $I_P \approx I_B$. When I_P is much larger than I_B, the voltage V_{DM1} increases forcing M1 to operate in saturation and $I_N \approx I_B$. Finally, for $I_N = I_P$ $V_{GS3} = V_{GS4}$; consequently, M1 and M2 behave as the series association of two transistors. Therefore, $I_N=I_P=2I_B$. The MOS translinear stage was simulated with SMASH [14] and the advanced compact MOSFET (ACM) model [12, 14]. The ES2-0.7μm technology was chosen. The aspect ratio of all transistors are the same, 50μm/20μm, and the results of the simulation are shown in Fig. 3(a).

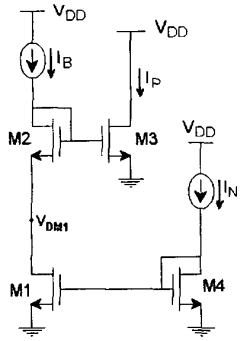
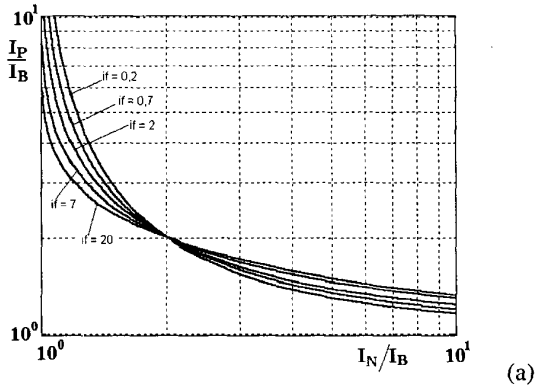
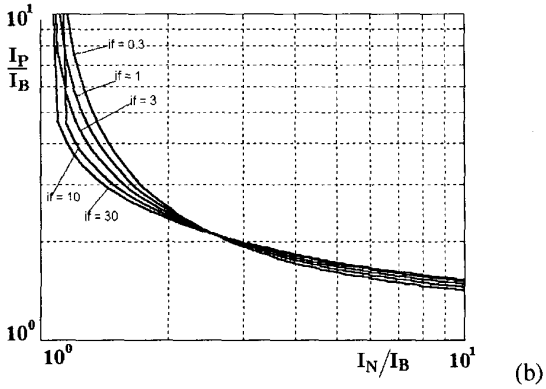


Fig. 2: Translinear structure that implements the function of Fig. 1(c).

For the experimental verification, transistors with aspect ratio 18μm /5μm from a 2μm technology were used. The experimental results shown in Fig. 3(b), are in close agreement with simulation. The difference between experimental and simulation is mainly caused by mismatch.



(a)



(b)

Fig. 3: (a) Simulated normalized transfer characteristic. I_S = 172nA. (b) Experimental normalized transfer characteristic. I_S = 200nA.

In Fig. 3, $i_f = \frac{I_B}{I_S}$ is the normalized drain current, while $I_S=\mu n C'_{ox} \phi^2_t W/2L$ is the normalization current [12].

The minimum current selector circuit as presented in Fig. 2 is asymmetric. To convert it into a symmetrical-circuit, M1 and M2 are divided into M1A, M1B, M2A, and M2B, as shown in Fig. 4.

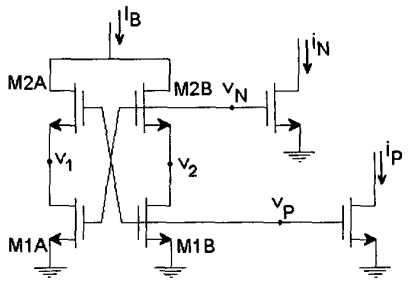


Fig. 4: Modified translinear structure of Fig. 2.

3. Class AB amplifier with minimum current control

There are several categories of CMOS class AB output stages [7, 8, 13]. The topology of our class AB opamp is based on [8], Fig. 5. In this work, we propose to implement the bias control circuit using the minimum current circuit shown in the previous section.

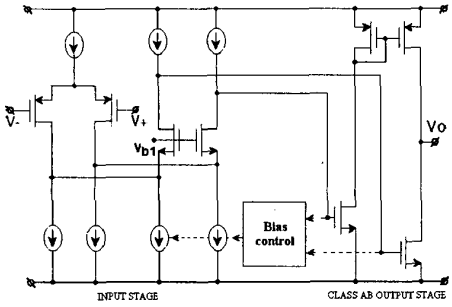


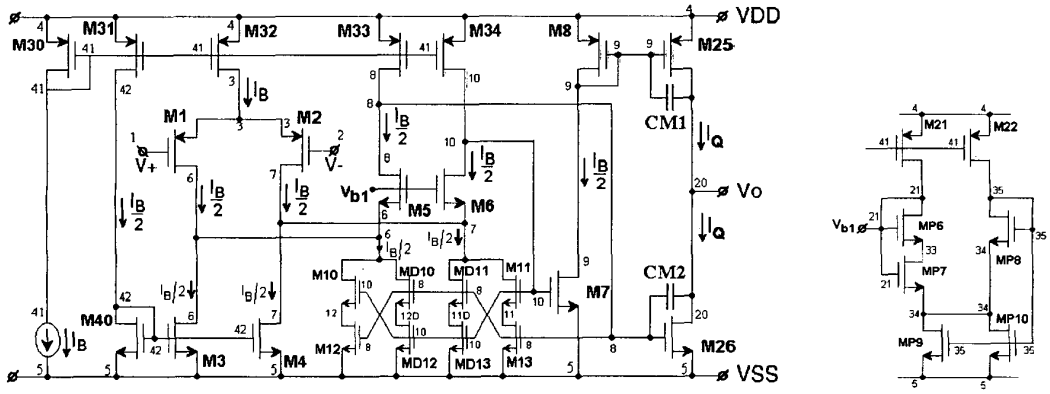
Fig. 5: Principle of class AB compact amplifier.

The new opamp (Fig. 6(a)) is constituted of two stages and the class AB control circuit. The first stage is formed by a differential amplifier (M1 and M2), followed by a cascode amplifier. The second stage is a push-pull amplifier (M25 and M26). The class AB control circuit is formed by two minimum current selectors [4], given by transistors M10-M13 and MD10-MD13. When the voltages in nodes 8 and 10 are the same the output current is null and the output quiescent current is given by:

$$I_{Q26} = I_B \frac{(W/L)_{26}}{(W/L)_{11}} \quad I_{Q25} = I_B \frac{(W/L)_7}{(W/L)_{11}} \cdot \frac{(W/L)_{25}}{(W/L)_8} \qquad (1)$$

The bias voltage Vb1 is supplied by the circuit of Fig. 6(b) [9], designed to bias M3 and M4 in the edge of saturation.

The design of a class AB amplifier for the sample-hold circuit shown in appendix A will be presented. For own application, a unity-gain frequency of 1MHz is adequate. From the analysis of the settling time [11], we chose the value of g_{mII} ($g_{mII}=g_{m25}+g_{m26}$), the transconductance of the second stage.



(a) (b)

Fig. 6: (a) Amplifier with class AB control based on the minimum current selector circuit. (b) Bias circuit for Vb1[9].

Setting the zero of the opamp frequency response at 10 times the unity-gain frequency, approximately, it follows that $g_{mI} \approx g_{mII}/10$. The compensation capacitance $C_C=CM1+CM2$ is determined from the gain-bandwidth product $GBW=g_{mI}/C_C$. The transistors were sized using the all region current-based MOSFET model of references [12, 14]. The main design equations are:

$$I_D = n \cdot \phi_t \cdot g_m \cdot \left(\frac{1+\sqrt{1+i_f}}{2} \right) \qquad (1)$$

$$\left(\frac{W}{L} \right) = \frac{g_m}{\mu_{n,p} \cdot C'_{ox} \cdot \phi_t} \left(\frac{1}{\sqrt{1+i_f}-1} \right) \qquad (3)$$

$$\left(\frac{W}{L} \right) = \frac{I_B}{I_{SQp} i_f} \qquad (4)$$

where n is the slope factor, ϕ_t is the thermal voltage, $i_f=I_D/I_S$ is the inversion level. The other symbols have their usual meanings.

Table I shows the design value for the class AB opamp with minimum current control circuit.

Table I: Design value for the class AB opamp.

	Value	Units
$V_{DD} = -V_{SS}$	0.75	V
I_B	0.6	µA
I_Q	1.5	µA
g_{mI}	7.5	µS
f_u	1M	Hz
t_s	4	µs
g_{mII}	65	µS

Given the transistor transconductances, the dimensions can be determined by specifying either the inversion level or the drain current. For this low-frequency design, operation in moderate inversion was chosen. The dimensions and inversion levels of the transistors are summarized in Table II.

Table II: Aspect ratios and inversion levels of the transistors of the class AB amplifier.

	Value	Unit
$(W/L)_{1,2}$	38/2	µm/µm
$(W/L)_{25}$	95/2	µm/µm
$(W/L)_{26}$	34/2	µm/µm
$(W/L)_{40,3,4,5,6}$ $(W/L)_{P6,P8,}$	14/4	µm/µm
$(W/L)_{21,22,31,33,34}$	8/4	µm/µm
$(W/L)_{7}$	7/2	µm/µm
$(W/L)_{10,11,12,13}$	14/2	µm/µm
$(W/L)_{8}$	19/2	µm/µm
$(W/L)_{30,32}$	16/4	µm/µm
$(W/L)_{P7,P9,P10}$	7/4	µm/µm
C_{M1}, C_{M2}	1	pF
$i_{f(M30-M34)}$	10	
$i_{f\_(remaining\ transistor)}$	2	

The opamp is going to be used in the S/H shown in Fig. A1. For both the load transistor M3 and the feedback transistor M2, W/L = 10µm/20µm, and the maximum current is 3.5µA. Thus, the opamp should supply at least 7µA. The opamp was simulated with SMASH 4.0 [14] using the ACM model. In Fig. 7 the open loop AC characteristics of the opamp are presented. The low-frequency gain is about 106dB and the phase margin is 47°.

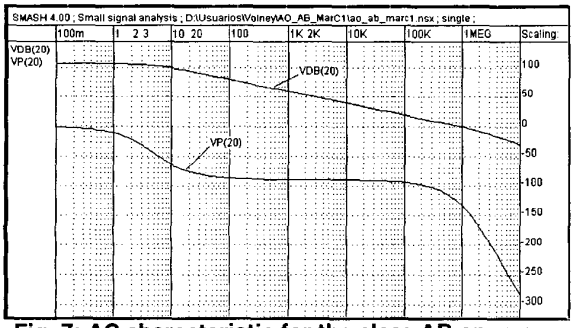


Fig. 7: AC characteristic for the class AB opamp.

Fig. 8 presents the DC transfer characteristic of the opamp of Fig. A1 operating in the sample mode. I_{in} is the current through M1. The currents of the transistors M25 and M26 are plotted. The quiescent current of M25 (or M26) is around 1.6µA and the minimum value tends towards 0.8µA. The total quiescent current of the opamp is $5I_B+I_Q$, that is, 4.5µA. The break points for input currents of the order of ±5µA are caused by voltage swing in the opamp output, which is limited to values close to V_{DD} and V_{SS}.

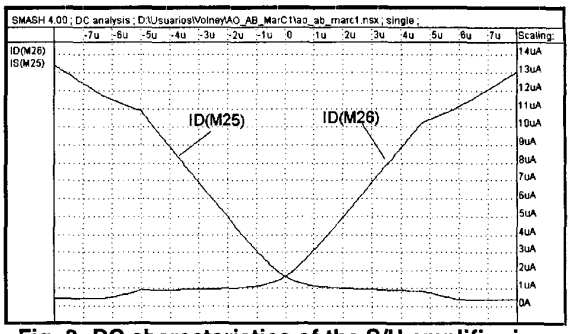


Fig. 8: DC characteristics of the S/H amplifier in Fig A1. I_{in} current is the x-axis variable

In Fig. 9, V20 and V54 represent the output voltage (Vo) and the input voltage, respectively, of the circuit of Fig. A1. The settling time to δ=04% is around 4µs. Table III summarizes the opamp characteristics simulated with SMASH [14].

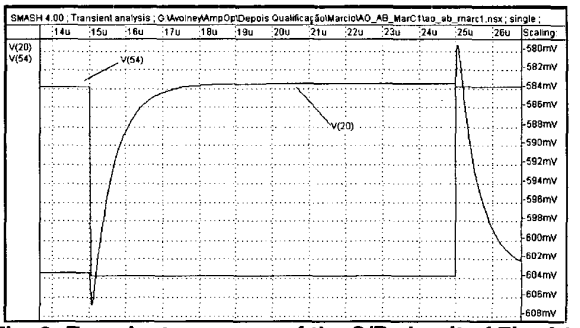


Fig. 9: Transient response of the S/R circuit of Fig. A1.

Table III: Simulated opamp characteristics.

	Value	Unit
$V_{DD} = -V_{SS}$	0.75	V
G_{DC}	106	dB
GBW	1	MHz
t_s (0.4%)	4	µs
I_{total}	4.5	µA
Bias voltage (V_B)	-0.59	V
Maximum output current	±95	µA
PSRR (V_{DD}): DC 100kHz	105 40	dB dB
PSRR (V_{SS}): DC 100kHz	115 20	dB dB
Input-referred noise spectral density (f=1kHz)	95	$nV/\sqrt{Hz}$
Input-referred noise (1Hz-10kHz)	9	µV
THD (S/H) f=1kHz , I_{in}=3µA	-71	dB
Z_{out} (open loop) (1kHz)	30k	Ω
Z_{out} (closed loop) of S/H (1kHz)	35	Ω

4. Conclusions

A very simple operational amplifier, class AB output stage for low-voltage operation was presented. The class AB control is based on the minimum current selector circuit presented in [4]. The simulation results are summarized in Table III. The opamp is being integrated on the AMS 0.8μm technology [10] and the prototype should be ready for tests in April 2001.

Acknowledgments

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Appendix A
Sample-hold

The class AB amplifier was designed to operate in a sample-hold (S/H) of the switched-MOSFET technique (SM) [2, 3], Fig. A1. The specs to be met are: unity-gain frequency of 1MHz, hold capacitor C_H = 5pF, load conductance g_L = 17μS and settling time (δ=0.4%) less than 5μs. The settling time for a S/H circuit is given by equation (A1) [11] with $g_1 = g_2 = g_3 = g_L$ where g_1, g_2, and g_3 are the conductances of the transistors M1, M2 and M3, respectively (Fig. A1).

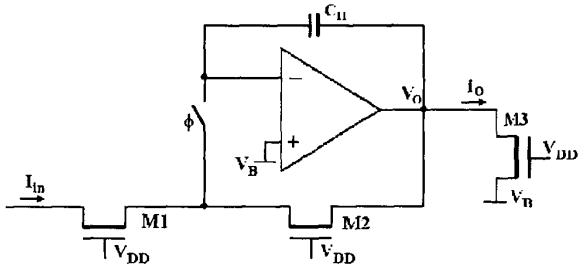

Fig. A1: S/H circuit [2, 3].

$$t_S = \left[\frac{3g_L + 2g_{mII}}{GBW g_{mII}} + \frac{C_H}{g_L}\right] \ln(1/\delta) \qquad \text{(A1)}$$

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