A Test Chip for Automatic MOSFET Mismatch Characterization

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ABSTRACT
This paper describes a test circuit for intensive characterization of MOS transistors mismatch. It aggregates analog switches, a shift register and a reference circuit, as well as the matrix of 1296 transistors to be tested. This circuit was integrated in a 0.35 μm bulk technology, and was designed to give experimental support for our MOSFET mismatch model. The test chip was characterized over a wide range of operation conditions, from weak to strong inversion, from linear to saturation region, allowing the analysis of MOSFET mismatch from bias, process and geometric parameters.

Categories and Subject Descriptors
B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms
Measurement, Performance, Experimentation.

Keywords
MOSFET, analog design, matching, mismatch, characterization.

1. INTRODUCTION
Mismatch is the denomination of time-independent variations between identically designed components [1], [2]. The performance of most analog or even digital circuits relies on the concept of matched behavior between identically designed devices. In analog circuits, the spread in the dc characteristics of supposedly matched transistors results in inaccurate or even anomalous circuit behavior. Also, for digital circuits, transistors mismatch leads to propagation delays whose spread can be of the order of several gate delays for deep-submicron technologies [3]. The shrinkage of the MOSFET dimensions and the decreasing in the supply voltage make matching limitations even more important in today advanced processes [4].

SBCCI'06, August 28 – September 1, 2006, Minas Gerais, Brazil.

Stochastic nature of local mismatch of MOS transistors makes its electrical characterization a complex, time consuming (and boring) task. A large number of samples, having different geometries, must be measured under a wide range of bias conditions, as a way to characterize device behavior and extract statistical model parameters.

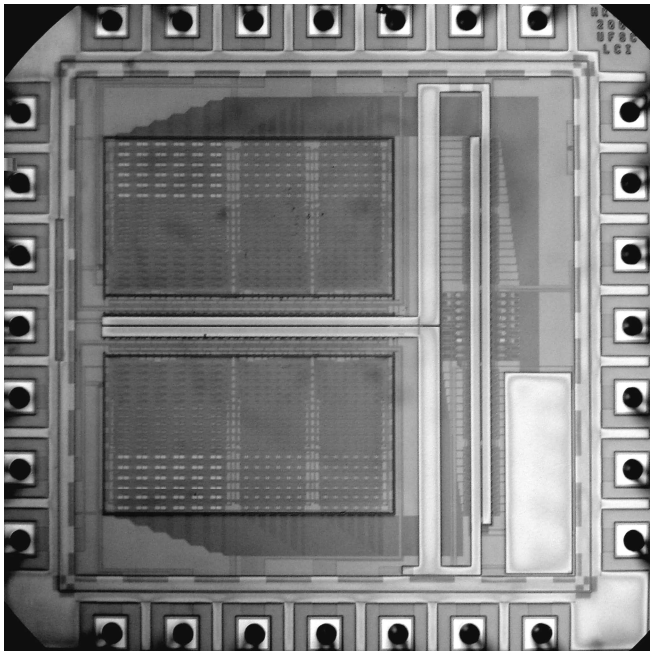

Figure 1. Microphotograph of the test chip (fabricated in the TSMC 0.35 μm process, on a 28-pad 1.5 mm square chip). The two rectangular large areas are the NMOS (down) and the PMOS (up) transistor arrays. Between them is part of the serial register (36 bits) and the selection switches. At the right side of the die is the final part of the serial register (45 bits) and the reference transistors for biasing.

Traditional design of test structures for mismatch characterization is based on grouping the transistors in an n-dimensional matrix, as a way to share the limited number of output pads. So, similar transistors are joined in common-drain (or source, or gate, or even bulk) arrays, and individually measured by selective bias applied to a specific combination of pads. In this way, for example, it is possible to have 200 transistors, divided in 5 arrays of 20 devices with the same

geometry, for the N and PMOS types, which could be individually selected using only 35 output pads [5].

Device-under-test selection can be hand-made, rendering the measurement results very susceptible to human mistakes, or can be done by high-cost servo-controlled microprobes or even by huge (and very high-cost) automated switching test equipment, being both the last options usually out of the reality of academic research laboratories.

In this paper we describe a test chip that contains 648 pairs of transistors for dc mismatch characterization, where the device selection strategy was included inside the chip, through the use of analog CMOS switches and a serial loading register. These features, besides custom software running in a PC microcomputer, and an *Agilent 4156 Semiconductor Parameter Analyzer*, result a fully automated mismatch characterization setup proper for academic laboratories. This circuit was successfully fabricated and characterized in the TSMC 0.35 μm bulk technology (Fig. 1) and is under characterization in the TSMC 0.18 μm bulk technology.

2. MISMATCH MEASUREMENT

MOSFET mismatch characterization is done through the measurement of the dc voltage-current behavior of an array of identically designed test transistors, and the accuracy and completeness of this process depend on several factors, which must be analyzed before designing the test circuit.

The first factor is the *sample size*, which means the number of identically designed devices that will form each array. Low sample size reflects a low confidence level of the results as representative of a general behavior. A too large sample size implies on a large chip size and circuit complexity. A good cost-benefit rate can be attained with a sample size around 30 to 50 samples [7].

The *number of arrays* and the way the *geometry* of each array is defined are fundamental factors when analyzing transistor geometric effects on mismatch. *Large*, *medium*, *small*, *short* and *narrow* devices are essential to estimate short and narrow-channel, or edge effects.

The way the test devices are *accessed* by the output pads and the total *number of pads* are the main restricting factors of the total number of test transistors. Direct device terminal connections, although using a matrix multiplexing structure, restrict the maximum number of devices for a given number of pads. The use of *in-circuit switches* can make the number of devices almost unlimited and reduce the number of pads. In this case the maximum number of devices is limited by the impact of the transistors drain or source *off* currents on the minimum current that must be measured from the devices. An internal digital register is also needed in this case, for *on-off* switch control. Serial data load also contributes to the reduction of the number of external pads.

The test devices can be *spatially organized* to be measured one by one (*complete pooling*), where the standard deviation is calculated over the entire array, or to have a pair of devices measured each time (*differential pooling*), where the standard deviation of mismatch is calculated over the behavioral difference of the pairs [8]. Mismatch measured by complete pooling can imply a difficult separation between local (smaller than variations of device sizes) and global (over the die gradients) effects.

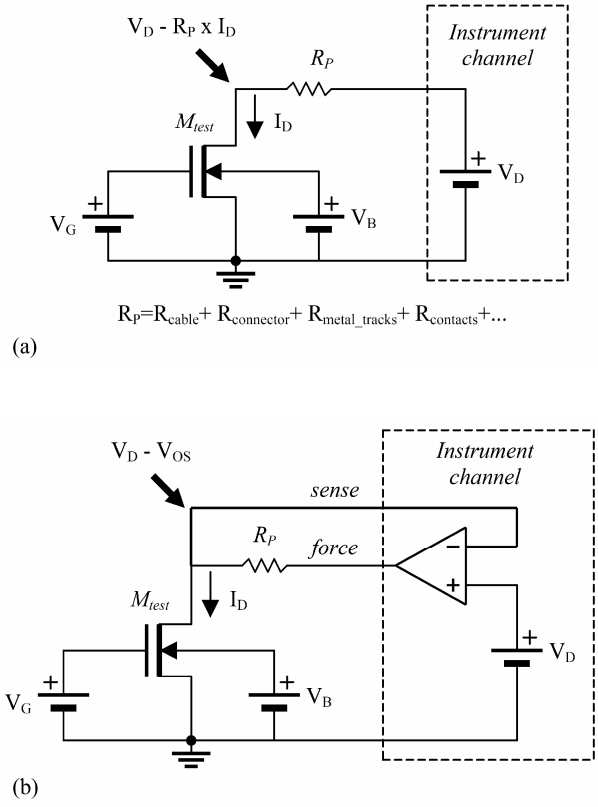

Figure 2. Measurement strategies: (a) traditional and (b) force-sense, where a feedback loop counterbalance voltage drops in the stimulus path.

The *measurement strategy* can use the traditional way, where the stimulus and the measurement are done over the same connection cable, and thus being the result vulnerable to all ohmic drops in the measurement path, or can use the *force-sense* technique, where distinct cables are used for stimulus and for measurement by the characterization equipment, establishing a negative feedback scheme (Fig. 2). The last option can be found integrated to the analog channels in modern semiconductor characterization equipments, like the *Agilent (HP) 4156* or the *Keithley 4200*, and can be used to overpass voltage drops from the equipment cables and connectors. Also, if for a given test device node, different stimulus and measurement pads and paths are included inside the circuit, in-circuit voltage drops from pins, contacts and wiring can be counterbalanced. The use of in-circuit selecting switches generally restricts the design to the force-sense option, because the voltage drops over the analog switches can mask mismatch measurements.

The *bias strategy* of the test devices could be done by applying the gate voltage directly from the characterization equipment, or by using *in-circuit reference* transistors, which are current-biased to produce the gate-source bias voltage for the test transistors. The last option is more adequate when mismatch is analyzed from the MOSFETs *inversion level* point-of-view [6].

3. TEST CIRCUIT

Our test chip was designed having the TSMC 0.35 μm (3.3 V n-well CMOS) as the target process, since this technology is widely used for analog and mixed-signal prototyping. A second version, adapted to the TSMC 0.18 μm (1.8 V double-well p-substrate CMOS), came recently from fabrication.

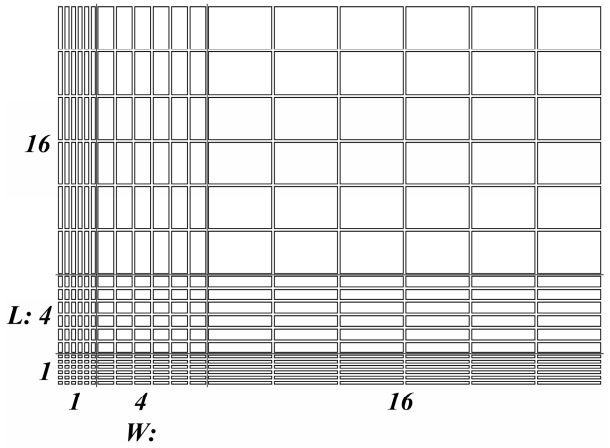

Figure 3. Spatial distribution of the 9 arrays of transistor pairs, and respective geometries. *L* and *W* are indicated in multiples of L_{min} and W_{min}, respectively.

One of the main motivations for this design is to have an improved version of our old test chips [5], with adequate accuracy for the measurement of short-channel, narrow-channel, edge, and other second order effects. So, we decided to design a rectangular matrix containing 9 arrays with 3 scaled ratios for transistors length (*L*) and width (*W*), disposed to optimize area consuming (Fig. 3). Each dimension (*L* and *W*) was scaled in 1, 4 and 16 multiples of the minimum *L* and *W*, respectively (which are L_{min} = 2λ and W_{min} = 3λ, being λ = 250 nm for the used standard rules). It resulted in *L* values of 0.5, 2 and 8 μm, and *W* values of 0.75, 3 and 12 μm.

Differential pooling was chosen, since it can highlight local mismatch causes better than complete pooling. Also, matching is generally required between two or among a few devices in most applications. So, each array was designed as a 6x6 matrix of pairs of transistors, resulting in 72 transistors per array, or 648 test transistors of each type (N and PMOS).

External access to drain terminals is multiplexed using 9 groups of 4 switches, each one being responsible for the connection of one of the identical transistors arrays. To minimize the effects of the mismatch between the equipment channels (instrumental errors), the drains of the left and right transistors of each pair can be connected to either the A or B measurement channels (Fig. 4). So, drain measuring is done in two phases, being the A and B equipment channels respectively connected to the left and right transistors at a first moment, and then being reversed in a second moment. Final measurement results from the average of these two phases. The aspect ratio of the force switches was defined to assure a maximum voltage drop of 0.5 V under the maximum characterization current, allowing at least 2.5 V of dynamic range for the drain voltage sweep. Sense switches are minimum size, since current flow through them is negligible.

One specific pair of each array can be selected by the activation of one switch, among 36, that connects its gates to the bias reference path (G). The other 35 deactivated switches keep the unselected pairs in the off condition. Since the arrays have different geometries, 9 reference transistors are needed for bias, being the respective one selected by multiplexing switches.

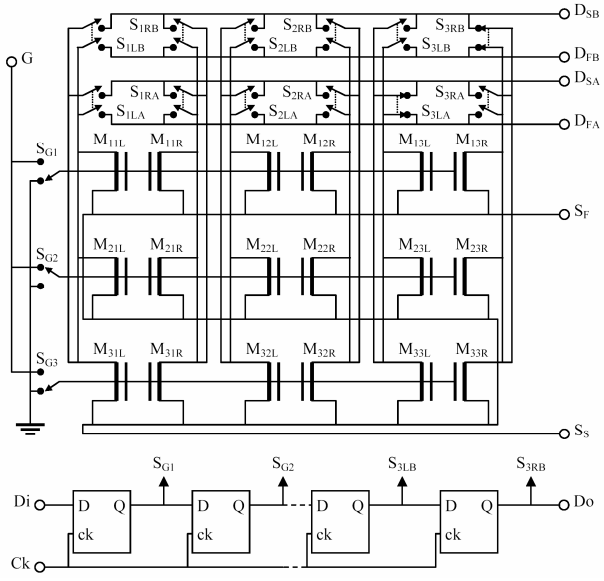

Figure 4. Simplified schematic diagram of the transistor matrix. It shows a 3x3 matrix for differential pooling, with the drain and gate selection switches and the serial register. The reference bias circuit is not shown. Common source connection also provides force-sense access.

Figure 4 shows a simplified schematic of the matrix, where the third one of the 3 vertical arrays, containing 3 identical pairs of transistors each, is connected to the A and B force and sense drain pads (D_{FA}, D_{SA}, D_{FB}, and D_{SB}) by the S_{3LA} and S_{3RB} switches. The force and sense connections are done by distinct wiring that extend to the drain of each transistor, so increasing the voltage drop compensation to that point. Also the pads connection of the common source (S_F and S_S) of all the transistors is done using the force-sense scheme. The second pair of the connected array is selected by the gate switch (S_{G2}), while the remaining transistors are kept unselected. The bias reference transistors and their selection switches are not shown. For this simplified example, an 18-bit serial register would be needed for switches control (12 for drain, 3 for gate and 3 for reference selections respectively). An 81-bit register was needed in the implemented version.

The complete circuit, containing 9 arrays, selection switches, bias references and output pads, must be doubled since we want N and PMOS characterization possibilities. As only N or PMOS characterization is done at a time, the same serial register can be used for both circuits.

Guard rings were included around the test transistor arrays, references, switches and the register array, to decrease the possibility of dc coupling through the bulk. Wide metal connections and multiple contact windows were employed in the

critical paths of the layout to lower ohmic drops [9]. The layout was done carefully, employing matching techniques to reduce undesirable global mismatch. The padframe was specifically designed for this application, since it should occupy the narrowest possible region around the die. Electrostatic protection was also included in the pads.

The mismatch test setup also includes an IBM-PC compatible computer, running the characterization software that was developed for this application. This software is responsible for the stimulus-measurement sequential stepping, controlling the *Agilent 4156* by its GPIB interface, programming the test chip serial stream, and for the data storing of the results. The serial register control is done using 3 pins of the parallel interface of the computer. An optically-isolated interface was also developed to avoid noise injection from the computer inside the test chip and to adapt the level of the interface signals. The data out signal (D_O) that comes from the register is used to check the correctness of the programming data.

4. MISMATCH COMPACT MODEL

MOSFETs mismatch results from several process and geometric factors, which were extensively studied, resulting in a dozen of different models in the last 20 years. The most famous of them is know as the Pelgrom's Model [2], which was proposed in 1989 and become an industry standard. Unfortunately this model does not consider the nonlinear nature of MOSFETs in a proper manner [10], yielding to inconsistent formulas [11]. This inconsistency has being highlighted by the shrinking dimensions and reduced supply voltage of current submicron technologies, where transistors are designed to work from very weak to very strong inversion condition [12].

Recently we developed a new mismatch model, based on the integration of the contribution of the local dopant fluctuation along the MOSFET channel [6], keeping in mind its nonlinearities through the use of the Advanced Compact MOSFET (ACM) model [13]. Doping concentration fluctuation that derives from the discrete nature of charges is widely recognized as the main mismatch cause for today's advanced technologies [14]. This model will not be described here since its detailed derivation is available in recent publications [4], [6].

The main result from our model is a compact formula for current mismatch evaluation, which predicts mismatch from geometry (W and L), bias (i_f and i_r) and technology (N_{oi} , B_{ISQ} and N^*)

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + B^2_{I_{SQ}}\right] \qquad (1)$$

where i_f and i_r are the forward and reverse inversion levels, and $N^* = -Q'_{IP} / q = nC'_{ox}\phi_t / q$ is the channel charge number density at pinch-off. N_{oi} is the main mismatch model parameter, representing the effective number of impurities per unit area in the channel depletion volume. B_{ISQ} is a less significant model parameter that accounts for variations in the specific current ($I_{SQ} = \frac{1}{2}\mu C'_{ox}\, n\phi_t^2$). The main part of the equation (1) can be simplified under specific conditions as shown in Table 1.

Table 1. Equation (1) simplified under specific conditions.

$\sigma^2_{I_D} / I_D^2$	weak inversion ($i_f << 1$)	strong inversion ($i_f >> 1$)
linear ($i_f \cong i_r$)	$\frac{N_{oi}}{WLN^{*2}}$	$\frac{N_{oi}}{WLN^{*2}}\frac{1}{1+i_f}$
saturation ($i_r \to 0$)		$\frac{N_{oi}}{WLN^{*2}}\frac{\ln(1+i_f)}{i_f}$

5. EXPERIMENTAL RESULTS

The versatility of the test chip, with individual software-controlled access to gate and drain terminals, allows a wide variety of MOSFET statistical voltage-current characterization, including the measurement of threshold voltage (V_T), slope factor (n), specific current (I_S), as well as mismatch.

Figure 5 shows the drain current (I_D) of one chip, measured from the *large* (W/L = 12µm/8µm), *medium* (3µm/2µm) and *small* (0.75µm/0.5µm) NMOS arrays. It was measured with the transistors under 1.1V of drain-source voltage (saturation), and operating in two inversion conditions: *weak inversion* ($i_f \approx 1$; figures a to c) and *strong inversion* ($i_f \approx 100$; figures d to f). Each column represents the I_D of the left transistor of a given pair in the 6x6 array. Average and standard deviation were calculated for the I_D of each array, resulting respectively: μ_a= 122 nA, σ_a= 2 nA; μ_b= 124 nA, σ_b= 7 nA; μ_c= 287 nA, σ_c= 114 nA; μ_d= 12.9 µA, σ_d= 0.066 µA; μ_e= 12.9 µA, σ_e= 0.19 µA; and μ_f= 17.2 µA, σ_f= 1.45 µA. *Small* transistors present higher I_D as a result from short-channel effects. This figure gives an idea of geometric and bias impact on mismatch.

Average specific current (I_S) was also measured from the *large*, *medium* and *small* arrays, resulting respectively: I_{S_large}= 132 nA, I_{S_medium}= 129 nA, and I_{S_small}= 149 nA. Using some mathematical processing over the I_S measurements, a first approximation of the channel length and width shifts can be calculated, resulting ΔL= 0.09 µm and ΔW= 0.08 µm ($L_{eff} = L - \Delta L$, $W_{eff} = W - \Delta W$) [15].

MOSFETs mismatch was measured from N and PMOS arrays of 10 from a lot of 40 encapsulated dies (DIP 28 package), all of them showing similar statistical behavior. Complete automatic measurement of the 9 arrays of one chip, in 6 different inversion levels, from linear to saturation condition, spends around 14 hours. This excessive time spending results from the *Agilent 4156* slow measurements of small currents, mainly below 100 nA. Also, to increase accuracy, the *Agilent 4156* is programmed to evaluate 16 samples of the same measuring point.

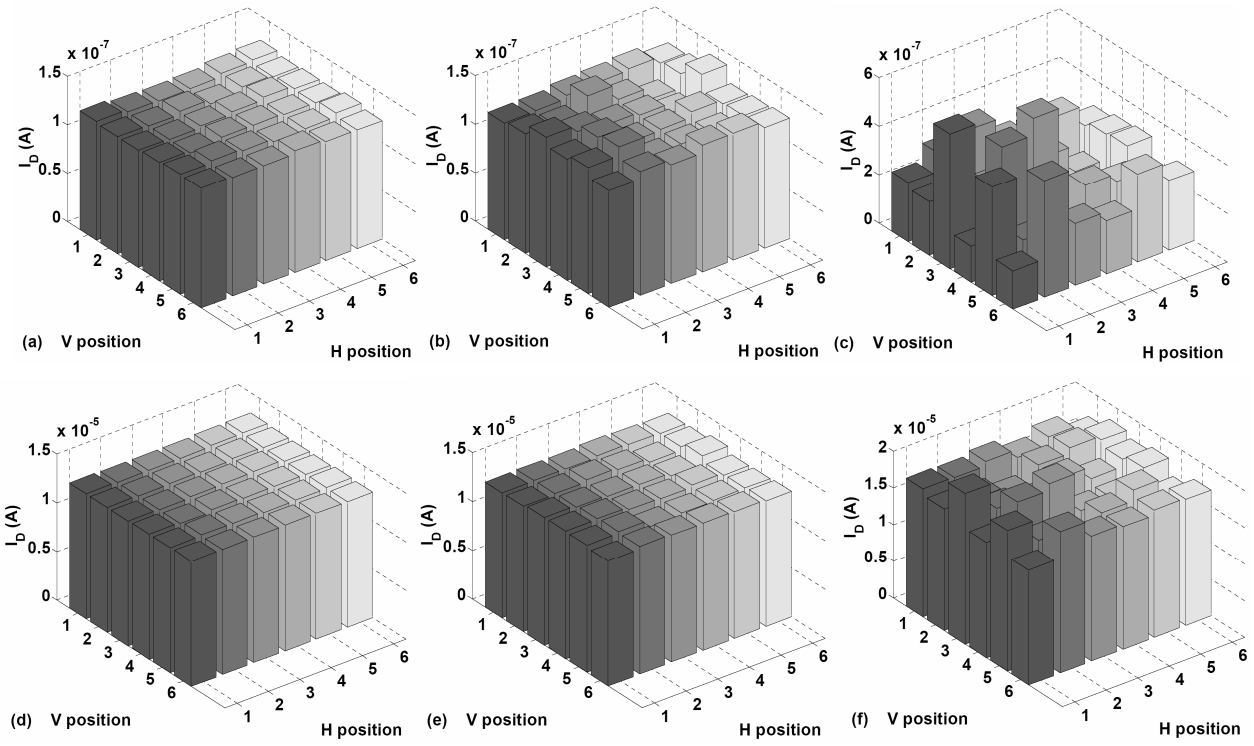

Figure 5. Drain current (I_D) measured from the (a, d) *large*, (b, e) *medium*, and (c, f) *small* arrays, when operating under saturation and in two inversion conditions (see text). Each column represents the I_D of a given transistor in the array.

Figure 6 shows the mismatch measurement (circles) from the *medium* N and P arrays of one chip, for drain to source voltage ranging from 20 mV (linear region) to 2V (saturation). Mismatch was measured for six different inversion levels (0.01, 0.1, 1, 10, 100 and 1000), covering the very weak to very strong inversion range. Solid lines were determined from our model using (1). Model parameters were calculated from *medium* and *large* size arrays, resulting N_{oi} = 1.9x10^{12} cm^{-2} and B_{ISQ}= 0.69 %-µm for the NMOS, and N_{oi} = 6.6x10^{12} cm^{-2} and B_{ISQ}= 0.77 %-µm for the PMOS.

Systemic errors of the measurement setup, like parasitic currents for example, were evaluated executing complete characterizations of some chips, but keeping all the drain switches in the off state. Experimental results showed that they impact less than 1% of the mismatch measurement for currents above 10 nA.

6. CONCLUSIONS

A mismatch test circuit that enables the characterization of a high number of closely located MOSFETs without the need for high-cost equipment has been presented. Force-sense technique provides accurate stimulus and measurement in all device terminals. Differential pooling was also used for better local mismatch perception. Nine geometries were implemented in N and PMOS test devices for the identification of second order effects and complete technological characterization. Besides mismatch, chip versatility allows a wide range of device measurements and parameter extraction. Technological, geometric and mismatch parameters and curves were presented for the TSMC 0.35µm process.

7. ACKNOWLEDGMENTS

The authors are grateful to CNPq and CAPES, Brazilian agencies for scientific development, for their financial support and to MOSIS MEP program for the test circuit fabrication.

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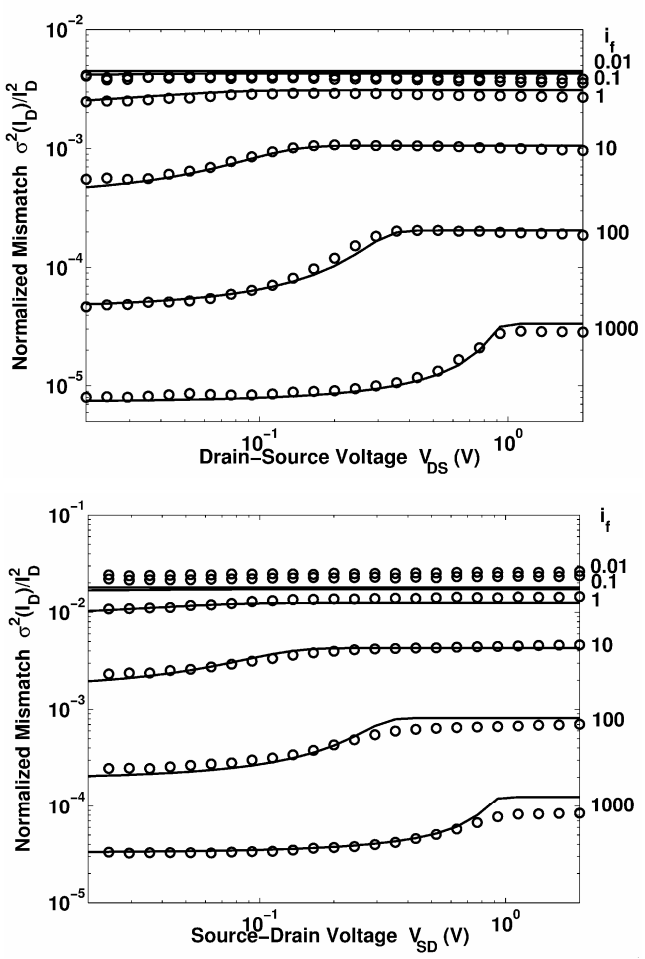

Figure 6. Normalized mismatch of 3μm/2μm (W/L) NMOS (up) and PMOS (down), from linear (20mV) to saturation (2V) region, under a wide range of inversion levels (i_f: from 0.01 to 1000). Measurements (circles) are from TSMC 0.35 μm process. Solid lines represent eq. (1).