Body-Bias Compensation Technique for SubThreshold CMOS Static Logic Gates

Luiz Alberto P. Melek Márcio C. Schneider Carlos Galup-Montoro
Universidade Federal de Santa Catarina
Campus Trindade - CTC-EEL-LCI
Florianópolis-SC-Brazil
+55-48-331-7629
pasini@eel.ufsc.br marcio@eel.ufsc.br carlos@eel.ufsc.br

ABSTRACT
This paper analyzes the performance of the conventional CMOS inverter, NAND-2 and NOR-2 static logic gates operating in the subthreshold region. The dependence of the drain currents on the process parameters can give rise to drive currents of NMOS and PMOS transistors that differ by an order of magnitude or even more. To compensate for this difference in currents, we propose three bias circuits in single-well processes that adjust the body voltage. Computer simulations using the AMS 0.8μm technology and the BSIM3v3 model were carried out to assess the compensation technique. A test chip was fabricated in both AMIS 1.5μm and TSMC0.35μm to further validate the proposal.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced Technologies, Microprocessors and microcomputers, VLSI (very large scale integration).*

General Terms
Measurement, Performance, Design, Experimentation, Theory.

Keywords
Body-bias compensation, subthreshold, CMOS, static logic, logic circuits, low-power.

1. INTRODUCTION
The use of portable equipments such as cellular phones, hand-held devices, laptops, and hearing-aid devices is increasing tremendously. Battery-operated equipment should be small and light; therefore, the power consumption should be kept to a minimum [1], [2]. Ultra-low power circuits are still in their infancy. A typical example is the digital FIR filter in [3] that can be used for biomedical signal detection, identification tags and smart cards. It is an 8-tap, 8-bit filter that dissipates 4.75μW only, at 1V supply and 500 kHz clock frequency. Another example is the voice controlled digital video decoder of [4] for wristwatch applications. Operating at 1V and 1MHz the circuit dissipates only 60μW. To fulfill the requirement of (ultra)-low power dissipation in the range of a few microwatts, while working at several megahertz, as in these applications, static logic gates operating in subthreshold are strong candidates [1].

In this paper, we present three bias circuits that provide appropriate body-bias voltage to compensate for structural differences or parameter deviations [5] of NMOS and PMOS transistors employed in static gates. Analytical formulations for the DC transfer function, transient time and power dissipation of a compensated inverter in weak inversion are shown in Section 3. In Section 4, we extend the analysis of the inverter to the NAND and NOR gates. Conclusions are summarized in section 5.

SBCCI'04, September 7–11, 2004, Pernambuco, Brazil.

2. COMPENSATION FOR PROCESS VARIATIONS
The subthreshold current of the N(P)-MOS transistor is given by [6]

$$I_{DN(P)} = I_{ON(P)} \cdot \exp\left((-)\frac{V_{GB} - V_{TN(P)} - n_{N(P)} \cdot V_{SB}}{n_{N(P)} \cdot \phi_T}\right)\left[1 - \exp\left(-(+)\frac{V_{DS}}{\phi_T}\right)\right] \quad (1)$$

where I_O is a scaling current, proportional to mobility, oxide capacitance per unit area, aspect ratio W/L, and n is the slope factor [6]. As shown in (1), the subthreshold current of a MOSFET is very sensitive to variations in temperature and process parameters, as is the performance of the inverter. Fig. 1 shows a typical current ($I_{DN(P)}$) transfers versus gate-bulk voltage (V_{GB}) using AMS0.8μm technology with V_{TN}=0.843V and V_{TP}=-0.744V and BSIM3v3 model for $(W/L)_N=(W/L)_P$=2μm/0.8μm. Three different curves are shown for each transistor (with nominal threshold voltage and with ±50mV deviation). As can be observed, a deviation of only ±50mV in the threshold voltage of the transistors can lead to a difference of more than an order of magnitude in the drain current. Deviations in the scaling current I_O produce a proportional variation in the drain current.

Expression (1) also shows that the variation of the source-to-body voltage V_{SB} of the transistor affects the drain current. With a proper source-to-substrate voltage the same drive current in the NMOS and PMOS transistors can be achieved regardless their sizes and technological parameters. This means that both NMOS

and PMOS can be drawn with minimum sizes allowed by the technology employed, thus saving chip area and increasing speed.

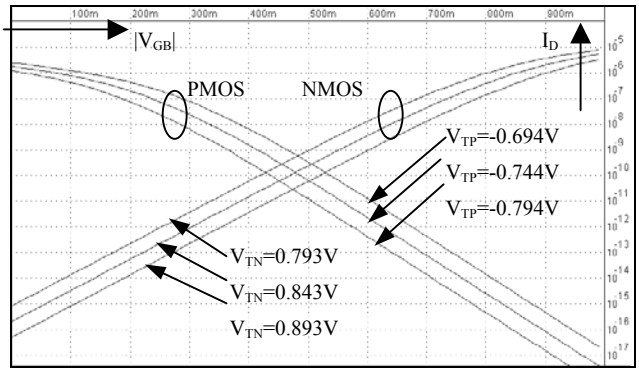

Figure 1: Typical drain current I_D x $|V_{GB}|$

Now consider, for instance, the conventional CMOS inverter. Assume that for a given supply voltage, the drive currents of the PMOS and NMOS transistors in subthreshold are different by an order of magnitude due to process deviations. As a consequence, the rise and fall times will also differ by an order of magnitude. The result is a waste of energy due to the higher current since the switching frequency is mostly determined by the higher of the rise and the fall times. So, compensation techniques that provided proper body-biasing must be applied to compensate the drive currents and avoid energy waste.

In Fig. 2, three circuits that can be used to compensate for process variations by providing an appropriate body-bias voltage V_W are shown. In all three bias circuits, the voltage V_W stabilizes at a value such that the current of the PMOS and NMOS devices are the same. In these circuits, two source-to-bulk diodes are forward-biased; thus, the compensation techniques should be limited to sub-1V power supplies. Low-voltage operation is also recommended to avoid latch-up. The circuit in Fig. 2(a), which equalizes the "off" currents of the complementary devices, has been proposed in [5] and has been a great source of inspiration to our work. The circuit in Fig. 2(b) provides an equalization of the driving currents while that in Fig. 2(c) equalizes the currents for an input equal to the gate threshold voltage, V_{TH}. Unless stated otherwise, from now on we will concentrate our analysis, simulation and experiments on the circuit in Fig. 2(c).

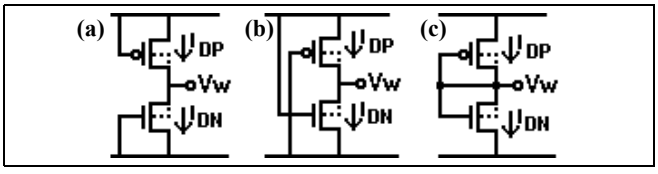

Figure 2: Bias circuits

Considering both NMOS and PMOS saturated, the analysis of Fig.2.(c) using (1) yields

$$V_W = V_{TH} = \frac{V_{DD}}{2} + \frac{V_{TN}}{2 \cdot n_N} - \frac{|V_{TP}|}{2 \cdot n_P} + \frac{\phi_T}{2} \cdot ln\left(\frac{I_{OP}}{I_{ON}}\right) \quad (2)$$

In Fig. 3, we show the experimental results for V_W as a function of the supply voltage. The result was obtained with the test chips for AMIS 1.5µm and TSMC0.35µm technologies. Near minimum size transistors were used for both NMOS and PMOS, with designed sizes are $(W/L)_{AMIS}$=2µm/1.5µm and $(W/L)_{TSMC}$=0.65µm/0.5µm. We observe that V_W adapts its value according to the supply voltage, threshold voltage, slope factors and current scaling deviations. Note that for low-voltages the value of V_W is close to zero and does not follow V_{DD} linearly. This can be explained by recalling that (2) assumes that both transistors are in saturation, which is not true for low supply voltages.

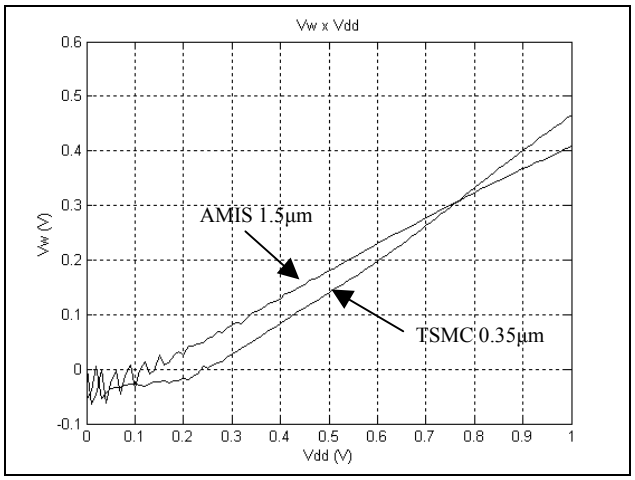

Figure 3: V_W as a function of the supply voltage

3. THE INVERTER

3.1 DC Transfer Characteristic

The analysis of the CMOS inverter starts with the DC voltage transfer curve, by replacing the transistors with equivalent conductances [7], as shown in Fig. 4. At the price of slightly lesser accuracy, modeling transistors by controlled conductances provides simpler expressions than that obtained using their current source counterpart, especially for more complex logic gates. The conductance is defined here as the derivative of the drain current, I_D, with respect to the drain-source voltage, for V_{DS}=0.

Assuming that the bias circuit of Fig. 2(c) provides the voltage V_W for biasing the inverter, analyzing the circuit in Fig.4(b), we obtain

$$V_{out} = \frac{V_{DD}}{1 + e^{\left[\frac{Vin - V_{TH}}{\phi_T} \cdot \left(\frac{1}{n_N} + \frac{1}{n_P}\right)\right]}} \quad (3)$$

Fig. 5 shows the DC voltage transfer characteristic (VTC) with different ratios of I_{ON} to I_{OP}, obtained from computer simulation and from the conductance model for a 650mV supply voltage. Simulation results show voltage transitions steeper than the

conductance model, which can be readily explained by recalling that conductance is a very simplified description of the MOSFET. I_{ON}/I_{OP}=5.8 corresponds to $(W/L)_N=(W/L)_P$=2μm/0.8μm, taking into account lateral diffusion. Table 1 presents a comparison between the inverter threshold voltage from (3) and from simulation.

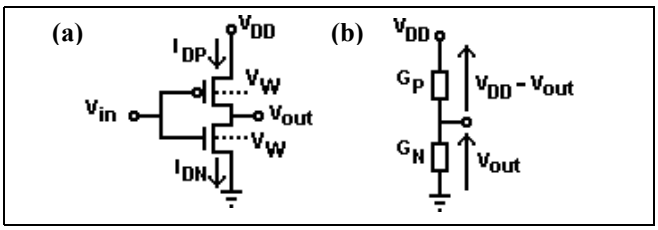

Figure 4: (a) CMOS inverter (b) Conductance model

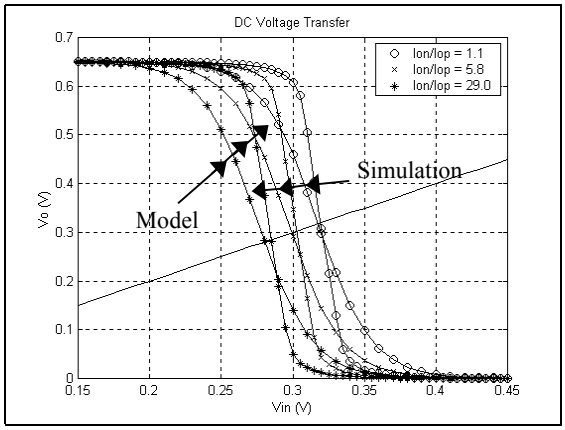

Figure 5: DC VTC for different I_{ON}/I_{OP} ratios.

Table 1: V_{TH} for different I_{ON}/I_{OP} ratios

I_{ON}/I_{OP}	V_{TH} (mV)	
	Model	**Simulation**
1.1	315.6	312.7
5.8	294.9	293.0
29.0	274.0	273.0

Fig.6 shows experimental results obtained from the test chips for TSMC 0.35μm technology. Voltage transfer was obtained with the same chip for different supply voltages. Very similar results can be obtained using the body-biasing circuits of Fig.2(a)-(b).

The inverter current can be calculated from (1) for any input voltage. Particularly, the maximum current, given in (4), is reached when both P and N-channel devices operate in saturation. Comparisons between the model, which assumes n_N=1.58 and n_P=1.37, and simulations using AMS 0.8μm and BSIM3v3 model are provided in Table 2 for different supply voltages and $(W/L)_N=(W/L)_P$=2μm/0.8μm.

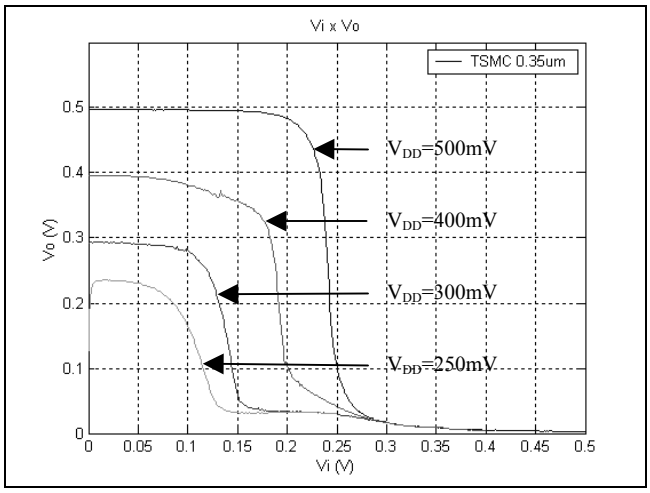

Figure 6: DC VTC – Experimental results.

$$I_{D,TH} = \sqrt{I_{OP} \cdot I_{ON}} \cdot e^{\frac{V_{DD}}{2 \cdot \phi_T} - \frac{V_{TN}}{2 \cdot n_N \cdot \phi_T} - \frac{V_{TP}}{2 \cdot n_P \cdot \phi_T}} \quad (4)$$

Table 2: Maximum current, $I_{D,MAX}$

V_{DD} (mV)	$I_{D,MAX}$ (pA)	
	Model	Simulation
400	3.16	1.42
500	14.57	10.18
600	69.88	72.55
700	394.49	515.00

3.2 Transient Analysis

The rise and fall times of the compensated inverter can be evaluated by calculating the time needed to charge and discharge the output capacitor, C_O, through the transistors as shown in Fig.7. They are determined by

$$t_{HL(LH)} = \frac{0.8 \cdot C_O \cdot V_{DD}}{I_{DRIVE,N(P)}} \quad (5)$$

where $I_{DRIVE,N(P)}$ is the drive current of the N(P) transistor determined from (1). During most part of the fall(rise) time the N(P) transistor is saturated, and current is almost constant and independent of the drain-source voltage. t_{HL} is the 90% to 10% fall time and t_{LH} is the 10% to 90% rise time.

The output capacitor, in (6) comprises the overlap capacitance (C_{OV}), drain junction capacitance (C_{jD}), interconnection (C_{INT}) and the next stage input capacitance (C_{GATE}).

$$C_O = \sum_{N,P} \left(C_{OV} + C_{jD} \right) + C_{INT} + \sum_{N,P} C_{GATE} \quad (6)$$

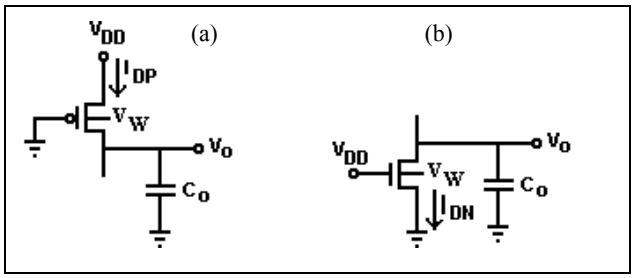

Figure 7: (a) Charge (b) discharge equivalent circuits.

Fig.8 compares the rise and fall times of the inverter for different supply voltages, with $(W/L)_N=(W/L)_P=2\mu m/0.8\mu m$, the AMS 0.8µm technology parameters and a fan-out of 5. The difference between the model and simulation can be readily explained because for higher voltages the inverter operates in moderate/strong inversion and (1) is no longer valid. Note that the aspect ratio of the PMOS is equal to that of the NMOS, not the usual design procedure for inverters operating in strong inversion. The body-bias technique used in this work provides the benefit of equalization of rise and fall times for minimum transistor dimensions of both PMOS and NMOS devices. The consequence of using minimum transistor dimensions is a reduced load capacitance.

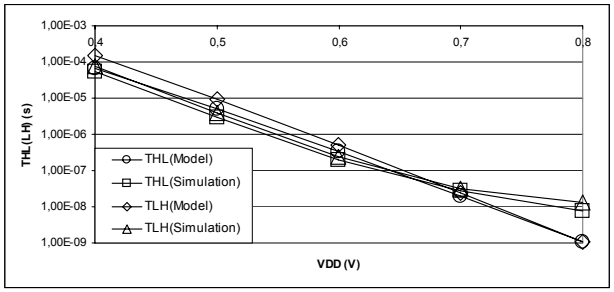

Figure 8: Output voltage transient

Fig.9 shows a comparison between the drive currents of the transistors of an inverter with and without body-bias compensation. The local substrates in the uncompensated circuit are connected to the supply voltages as is usual for higher supply voltages. In this case, the drive currents of the PMOS and NMOS transistors can differ by more than two orders of magnitude due to mismatch of both threshold voltages and slope factors, and rise and fall times can differ accordingly. However, applying V_W to both NMOS and PMOS transistors, the currents are equalized and rise and fall times are almost the same.

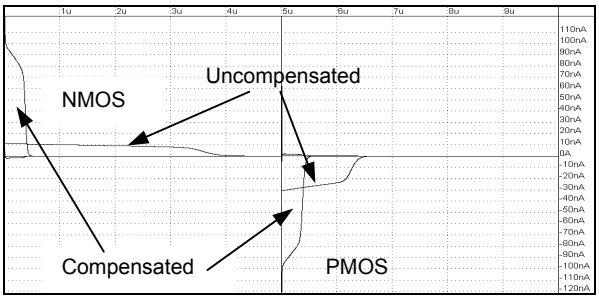

Figure 9: Current in the transistors

3.3 Power Dissipation

Usually, power dissipation in a circuit is split into dynamic power, short-circuit power and static power [8]. The dynamic power of the subthreshold CMOS logic inverter can be calculated from the results already published in textbooks [7], and is a function of the operating frequency. It is included in (7) for completeness. It can be demonstrated that the short-circuit power is considerably lower than the dynamic power, and will be neglected.

$$P_{DIN} = C_O \cdot V_{DD}^2 \cdot f \tag{7}$$

Static power is defined as the average power dissipated in the transistors when they are "cut off". But in our case, the bodies of the transistors are biased by the same voltage V_W; therefore source/drain diodes can be forward-biased as shown in Fig.10. These diodes dissipate an amount of power usually much higher than that due to transistor currents. The static power in (8) neglects the transistor leakage currents and accounts for dissipation in diodes only. Knowing that the current in a diode is an exponential function of its terminals voltages, static power can be expressed by (8) accepting that two diodes are always forward-biased and other two are biased according to the output voltage. I_{SN} and I_{SP} are the NMOS and PMOS source/drain diode scaling currents, respectively, and η is the emission coefficient.

$$P_{st} = \frac{3 \cdot V_{DD}}{2} e^{\frac{V_{DD}}{2\eta \cdot \phi_T}} \cdot \left(I_{SN} + I_{SP}\right) \tag{8}$$

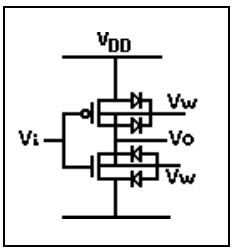

Figure 10: Source/Drain Diodes

4. NAND/NOR GATES

4.1 DC Transfer Characteristics

The analysis carried out for the inverter can be extended to more complex logic gates such as the NAND and the NOR, shown in Fig.11. Substituting the transistors in these gates by equivalent conductances the voltage transfer characteristics are expressed by (9) and (10) for the NAND and NOR gates, respectively.

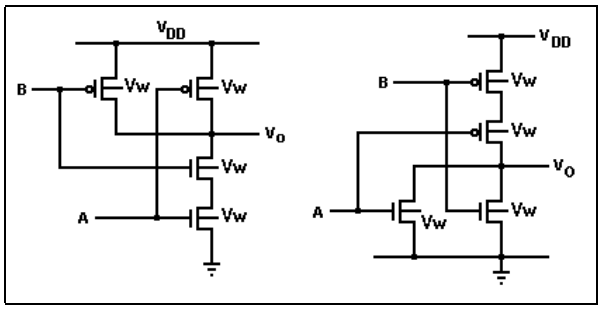

Figure 11: (a) NAND (b) NOR

$$V_O = \frac{V_{DD}}{1+\left(e^{-\frac{V_A - V_{TH}}{n\cdot\phi_T}} + e^{-\frac{V_B - V_{TH}}{n\cdot\phi_T}}\right)^{-2}} \tag{9}$$

$$V_O = \frac{V_{DD}}{1+\left(e^{\frac{V_A - V_{TH}}{n\cdot\phi_T}} + e^{\frac{V_B - V_{TH}}{n\cdot\phi_T}}\right)^{2}} \tag{10}$$

where V_A and V_B are the input voltages. Fig.12 shows the experimental results obtained for the 2-input NAND gate fabricated with TSMC 0.35μm technology and a 500mV supply voltage.

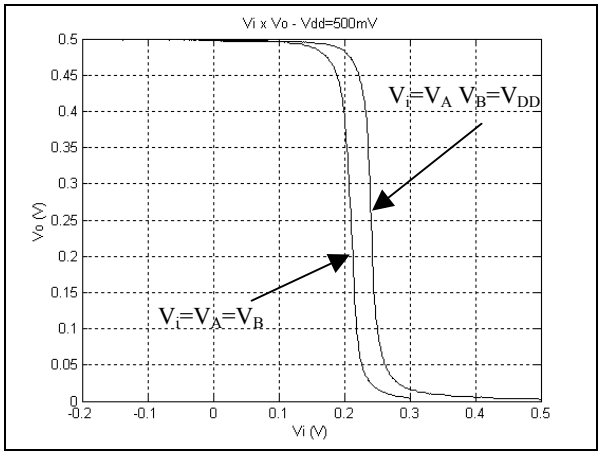

Figure 12: NAND-2 voltage transfer

4.2 Transient Analysis

Rise and fall time for the NAND and NOR gates can be evaluated by the same expression (5) of the inverter, with a few modifications. To calculate I_O, which is proportional to the aspect ratio, we use the equivalent aspect ratio that depends on the switching event. The equivalent aspect ratio for the NAND gate during rise time is expressed by (11) and by (12) during the fall time. Similar conditions can be formulated for the NOR gate. Also, the output capacitance seen by the gate is almost doubled if compared to the inverter, since these gates have twice the number of transistors.

$$\left(\frac{W}{L}\right)_{eq} = \begin{cases} \left(\frac{W}{L}\right)_{A,B}, if \quad one \quad input \quad \text{var}ies \\ \left(\frac{W_A + W_B}{L}\right), if \quad both \quad inputs \quad \text{var}\, y \end{cases} \tag{11}$$

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L_A + L_B}\right) \tag{12}$$

5. SUMMARY

The operation of a CMOS inverter in weak inversion was investigated and two new bias circuits were proposed to equalize drive currents of PMOS and NMOS transistors. Transistor operation is unusual: supply voltage is below the transistor threshold voltages, the body of the transistors are not connected to the supply voltages but to a bias voltage that compensates technological parameters deviations and, finally, the source/drain diodes of the transistors are forward biased. Simple analytical models for the DC transfer characteristics and transient response were presented. Formulation for the static power dissipation was also developed, including the forward-biased source/drain diodes.

As expected, the rise and fall times for logic gates operating in the subthreshold region are quite high and low/medium performance can be achieved. But power dissipation is very low, making this technique a very promising candidate for (ultra)-low power circuits. Future technologies tend to benefit from this proposal since they have lower threshold voltages.

6. ACKNOWLEDGEMENTS

We would like to thank the financial support of CAPES and CNPq, Brazilian funding agencies for research and development. Also, we would like to thank MOSIS for fabricating the test chips through the MEP research program.

7. REFERENCES

[1] H. Soeleman, K. Roy, "Ultra-Low Power Digital Subthreshold Logic Circuits", International Symposium on Low Power Electronics and Design, 1999, pp.94-96.

[2] H. Soeleman, K. Roy, B. Paul, "Sub-Domino Logic: Ultra-Low Power Dynamic Sub-Threshold Digital Logic", IEEE International Conference on VLSI and Design, 2001, pp211-214.

[3] Amirtharajah, R., Chandrakasan, A., "Self-Powered Signal Processing Using Vibration-Based Power Generation", IEEE J. Solid-State Circuits, vol. 33, No. 5, May 1998.

[4] Bolcloni, L., Borgatti, M., Felici, M., Rambaldi, R., Guerrieri, R., "A low-power, voice-controlled, H.263 video decoder for portable applications", IEEE Journal of Solid-State Circuits, vol. 33, no. 11, November 1998.

[5] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, E. Nowak, "Low-Power CMOS at Vdd=4kT/q", Device Research Conference 2001.

[6] Tsividis, Y. P., *"Operation and Modeling of the MOS Transistor"*. McGraw Hill, 1999.

[7] C. Mead, L. Conway, "Introduction to VLSI Systems", Addison Wesley, 1980.

[8] R. Gonzalez, B.M. Gordon, M.A. Horowitz, "Supply and threshold scaling for low power CMOS", IEEE J. Solid-State Circuits, Vol.32, no.8, August 1997.