An Ultra-Low-Power Self-Biased Current Reference

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ABSTRACT
This paper presents the design of an ultra-low-power self-biased 400pA current source. An efficient design methodology has resulted in a cell area around 0.045mm^2 (0.027mm^2) in the AMIS 1.5µm (TSMC 0.35µm) CMOS technology and power consumption around 2nW for 1.2V supply. Simulated and experimental results validate the design and show that the current sources can operate at supply voltages down to 1.1V with a good regulation (< 4%/V variation of the supply voltage in a 0.35µm technology). This current source is suitable for very-low-power applications.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General.

General Terms
Design

Keywords
Current reference, self-cascode MOSFET, design methodology, ultra-low-power, low-voltage, inversion level.

1. INTRODUCTION
Current references are essential blocks for properly biasing analog components of integrated circuits. In the selection of current references, efficient, simple and easy-to-design structures are highly desirable [4], [6], [8].

Methodologies for CMOS analog design based on the concept of inversion level [7], [10] have been shown to provide a robust alternative for high performance in very-low-power [5] and low-voltage circuits [4]. Analog circuits based on such a design technique require a current reference to be generated on-chip. An important benefit of the generation of on-chip current references is the avoidance of extra pads to communicate with the external environment [1].

Several self-biased current source (SBCS) circuits are found in the literature [1-3] - [5-9], but none of them has proved to be suitable for extremely low-power applications. Papers [1]-[3] present current references based on the properties of the MOSFET biased in strong inversion, which exhibit relatively high consumption and are not appropriate for low supply voltage since they use stacked transistors biased in strong inversion. The SBCS in reference [6] is dependent on the thermal voltage and on a resistance value that for very low currents would require a very large silicon area. The large current gains required for the current mirrors to implement the SBCS presented in [7] degrade its power efficiency. To avoid the need for a resistor, the authors of [8] use a MOSFET working in the triode region to replace the resistor. Even though simple, the SBCS of [8] is not suitable for low voltage operation, as pointed out in [9]. The circuit in [9] uses a self-cascode MOSFET (SCM) in strong inversion and a proportional-to-absolute temperature (PTAT) voltage reference generated by means of a weakly inverted pair of transistors. Neither the power efficiency nor the low-voltage capability of the current source in [9] are optimal due to both the use of slightly more complex structures than in [6] and [8] and the operation of some transistors in strong inversion.

The SBCS we propose here shares some similarities with the circuits proposed in [7]-[9], namely: (i) the proposed circuits derive a PTAT voltage from MOSFETs biased in weak inversion; (ii) the proposed SBCS outputs a current proportional to the MOSFET specific current [10].

Our SBCS circuit uses MOSFETs only, operating in either weak inversion or moderate inversion. As a result, the SBCS in this study is able to operate at lower supply voltages and consumes less power than all the previously reported SBCS since operation in strong inversion is avoided. Our current reference can operate down to 1.1V supply in 1.5 µm CMOS technology and is potentially able to operate at 0.7V in sub-0.18µm technologies.

In Section 2, we review the ACM model [10] and the concept of inversion level. We develop the basic design equations for the SBCS in Section 3. Section 4 introduces the low-voltage CMOS SBCS. The design methodology of the SBCS is formulated in Section 5. Two very low power SBSCs are implemented in both the AMIS 1.5µm and TSMC 0.35µm CMOS processes. Simulation and experimental results are presented in Section 6. Finally, concluding comments are drawn in Section 7.

2. THE ACM MODEL
In the design methodology for the SBCS, we have employed ACM, a current-based MOSFET model that uses the concept of inversion level [10]. According to the ACM model, the drain current can be split into the forward (I_F) and reverse (I_R) currents

$$I_D = I_F - I_R = I_S(i_f - i_r) \quad (1)$$

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$$I_S = I_{SQ}\left(\frac{W}{L}\right) = I_{SQ}(S) \tag{2}$$

$$I_{SQ} = \mu C'_{ox}\, n \frac{\phi_t^{\,2}}{2} \tag{3}$$

I_F (I_R) depends on the gate and source (drain) voltages. In forward saturation, $I_F >> I_R$; consequently, $I_D \cong I_F = I_S\, i_f$. I_S is the normalization (specific) current and I_{SQ} is the sheet specific current (I_S for $W = L$), i_f(i_r) is the forward (reverse) inversion level, and μ, C'_{ox}, n, ϕ_t, and $W/L=S$ are the mobility, gate oxide capacitance/area, slope factor, thermal voltage, and the transistor aspect ratio, respectively. The relationship between current and voltage [10] is given by

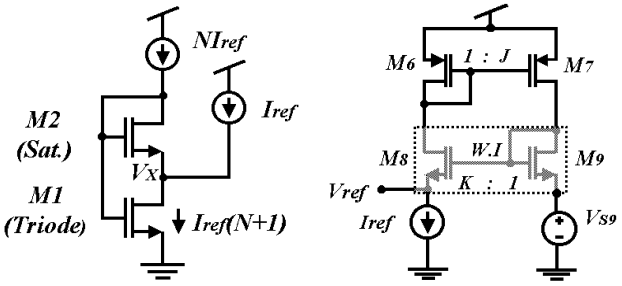
$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{4}$$

where $V_P \cong (V_G - V_{TO})/n$ is the pinch-off voltage and V_{TO} is the zero bias threshold voltage. More details regarding (1)-(4) can be found in [10]. The sheet specific currents for the AMI 1.5µm (and TSMC 0.35µm) technology are approximately I_{SQN}=28nA(70nA) and I_{SQP}=10nA(25nA) calculated assuming n=1.2(1.3) for N- and P-channel devices, respectively, while V_{TP} = -0.9V(-0.7V) and V_{TN} = 0.6V(0.6V).

The self-biased current-source circuit proposed here is an extractor of the normalization (specific) current I_{SQ} [7] optimized for low-voltage and very low power applications.

3. DESIGN EQUATIONS

The core of the SBCS is the SCM shown in Fig.1 (a). The V-I characteristic of the SCM is very appropriate for building low-voltage analog blocks such as current references and sub-100mV PTAT voltage references [5-9].



(a) (b)

Fig. 1. (a) Schematic of the self-cascode MOSFET (SCM)
(b) Voltage-Following Current Mirror (VFCM).

$$I_2 \cong I_{F2} = I_{S2} i_{f2} \tag{5}$$

$$I_{D1} = I_{F1} - I_{R1} = I_{S1}(i_{f1} - i_{r1}) = (N+1) I_{ref} \tag{6}$$

Since $V_{P1}=V_{P2}=V_P$ and $V_{D1}=V_{S2}$, then $i_{r1}= i_{f2}$; thus, from (5) and (6) we can find the relationship between i_{f1} and i_{f2}

$$i_{f1} = i_{f2}\left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] \tag{7}$$

The application of (4) to node V_X for M_2 results in

$$\frac{V_P - V_x}{\phi_t} + 1 = \left(\sqrt{1 + i_{f2}} - 1\right) + \ln\left(\sqrt{1 + i_{f2}} - 1\right) \tag{8}$$

while, for the source of M_1, expression (4) gives

$$\frac{V_P}{\phi_t} + 1 = \left(\sqrt{1 + i_{f1}} - 1\right) + \ln\left(\sqrt{1 + i_{f1}} - 1\right) \tag{9}$$

Equations (7)-(9) with three unknowns (V_P, i_{f1}, i_{f2}) have been instrumental in the development of the design methodology of the SBCS. If we assume that a voltage generator sets V_X at a given value and a PMOS current mirror defines N, the inversion levels i_{f1} and i_{f2} as well as the current flowing through M_1 and M_2 are readily determined. In the following, we show a possible implementation of a reference voltage for V_X.

The Voltage-Following Current Mirror (VFCM) [12] in Fig. 1(b) can be used to generate V_X at the intermediate node of the SCM [6]. V_{ref} can be calculated using (4) and assuming M_8-M_9 to be operating in weak inversion saturation. Noting that $V_{P8}=V_{P9}$, $I_{D8}=I_{D9}/J$, and $V_{ref}=V_{S8}$, then

$$V_{ref} = V_{S9} + \phi_t \ln(JK) \tag{10}$$

where $J=S_7/S_6$ and $K=S_8/S_9$. In our circuit topology, V_{S9} can be either zero or a PTAT voltage generated by means of a second SCM operating in weak inversion, as shown in Fig. 2. The application of expressions (7)-(9) to the SCM M_3-M_4 operating in weak inversion gives

$$V_{S9} = V_{X(W.I)} = \phi_t \ln\left[1 + (1+J)\frac{S_4}{S_3}\right] \tag{11}$$

4. THE PROPOSED LOW-VOLTAGE SBCS

The circuit shown in Fig. 2 operates as follows. When both M_8 and M_9 are biased in weak inversion there is a PTAT voltage shift ($KJ>1$) between the two MOS devices. If the switch is connected to ground, the PTAT voltage is given by (10), with V_{S9}=0. This simple topology is stable for $KJ>1$ and is very accurate for $KJ>10$ [9].

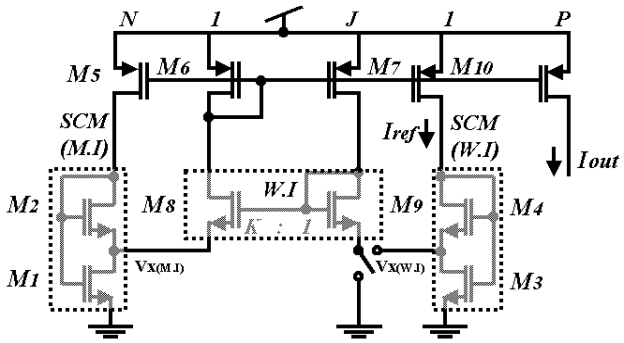


Fig. 2. Self-biased current source circuit.

If the switch is connected to M_3-M_4, then V_{S9} is given by (11). This second implementation results in improved symmetry (for K=J=1) and matching of the structure.

5. DESIGN METHODOLOGY

The design specifications of the current reference are usually the minimum supply voltage (V_{DDmin}), power dissipation, silicon area, and sensitivities, in addition to I_{ref}, the value of the current itself. The design methodology can be applied to either the simple topology (switch connected to ground) or the symmetric topology (switch connected to node $V_{X(WI)}$) in Fig. 2. The only difference between these two topologies as regards design methodology is the way the voltage $V_{X(MI)}$ is generated.

The minimum supply voltage, which is determined by the constraints imposed by the two leftmost branches in Fig. 2, can be written as

$$V_{DD} \geq \max\{|V_{DSsat,P}| + V_{GS,M1}, |V_{GS,P}| + V_{DSsat,M8} + V_x\} \quad (12.a)$$

where $V_{DSsat,M8} \cong 100$mV since M_8 operates in weak inversion. The p-channel transistors are sized to operate in weak inversion, with an inversion level close to 1 or smaller; therefore, $|V_{DSsat,P}| \cong 100$ mV and $V_{GS,P} \cong V_{TP}$ or less. V_X is chosen to be less than 100 mV while M_2 is sized so as to operate in moderate inversion, with i_{f2} within the range 3 to 8. This choice of i_{f2} has two purposes: (i) M_2 should not be operating in weak inversion in order to reduce the sensitivity of the reference current to both mismatch and supply voltage and (ii) the selected inversion level of M_2 should have a relatively small value in moderate inversion so that its gate-to-source voltage is only slightly higher than the threshold voltage. Since, in this case, V_X<100 mV and i_{f2} is within the range 3 to 8, then $V_{GS,M1} = V_{GS,M2} \cong V_{TN}$ + 100 mV. Hence, we can use the first-order approximation for (12.b)

$$V_{DD} \geq \max\{|V_{TP}|, V_{TN}\} + 200mV \quad (12.b)$$

to calculate the minimum supply voltage. Although expression (12.b) is a rough approximation, it is very useful for predicting the minimum supply voltage required to start up the current reference circuit.

The sensitivity of the current to the power supply is mostly associated with the Early effect of M_7 and M_8. The Early effect can be reduced using long channel transistors. However, this demands a large silicon area. One approach to obtaining long channel lengths with moderate area is the trapezoidal transistor proposed in [11]. We have employed trapezoidal transistors for implementing M_8 and M_9 as well as the PMOS transistors.

In our design methodology, we have designed M_2 to operate in moderate inversion with i_{f2}=3 or, equivalently, $V_P = V_{x(M.I)}$ (see (8)), and $J=1$. Using the simple topology ($V_{S9}=0$) for a given K factor, we can readily calculate i_{f1} from (8) and (9) by solving

$$1 + \ln(K) = x + \ln(x) \quad (13.a)$$

for $x = \left(\sqrt{1+i_{f1}} - 1\right)$. Once x has been calculated for a given K, one can calculate S_2/S_1 from (7), which, for $i_{f2}=3$, yields

$$\frac{S_2}{S_1} = \frac{(x+1)^2 - 4}{3(1+1/N)} \quad (13.b)$$

From

$$i_{f2} = I_{D2}/(I_{SQ}S_2) = NI_{ref}/(I_{SQ}S_2) \quad (13.c)$$

we find $S_2 = NI_{ref}/3I_{SQ}$. For $JI_{ref} << I_{SQ}$, $S_9 = J$ keeps M_9 in weak inversion and the factor N defines a trade-off between power consumption and area. The aspect ratio (S_P) of the PMOS transistors M_5-M_7 and M_{10} is calculated using (2) and the appropriate inversion level, which is usually less than 1 for low-voltage applications.

For the design of the symmetric topology we have used the same methodology but with $K=1$, and S_3, S_4 calculated from (11) for a given V_{S9}.

6. RESULTS

The circuit topologies with the switch connected either to ground or to the $V_{X(WI)}$ node in Fig. 2 have been designed for the AMIS 1.5μm and TSMC 0.35μm CMOS technologies. A comparison of post layout simulation using the BSIM 3v3 model and experimental results is given in Table I for I_{ref}=400pA, $N=J=1$, $S_9=1.6$ and $S_2/S_1=1.2$. The transistor dimensions for the symmetric topology (TSMC 0.35μm) are presented in Table II.

TABLE I- SUMMARY OF SIMULATIONS AND EXPERIMENTS

Parameter	Simple topology K=9		Symmetric topology, K=1		Unit
Technology	AMIS 1.5μm		0.35μm	1.5μm	
	Simulation	Experiment	Experiment	Experiment	
V_{DDmin}	1.1	1.1	1.05	1.1	V
Power (at 1.1V)	1.5	1.5	2.0	2.0	nW
V_{ref} sensitivity to V_{DD}	0.9	1.6	0.85	1.3	%/V
V_{ref} sensitivity to T	+0.32	X	X	X	%/°C
I_{ref} sensitivity to V_{DD}	4.7	6.2	4.0	6.0	%/V
I_{ref} sensitivity to T	+0.047	X	X	X	%/°C

TABLE II – TRANSISTOR SIZES FOR THE SYMMETRIC TOPOLOGY IN TSMC 0.35μm

Transistor	W [μm]	L [μm]	i_f
M_1	2	18x60*	10.2
M_2	2	15x60	3
M_3	10	6	0.008
M_4	4x10	6	0.001
$M_{5,7,10}$[&]	4	10	0.04
M_{8-9}[&]	10	6	0.004

[&]Trapezoidal transistors were implemented. The dimensions of the transistor connected to the source are W and L as given in Table II while the one connected to the drain is sized 8W and L.

* Series association of 18 transistors having W=2μm and L=60μm.

The experimental results show that the sensitivity of the reference current to the supply is relatively low and quite acceptable for most applications. Two major factors are primarily responsible for the discrepancies between the simulated and experimental results for both the current and voltage regulation namely, poor modeling of the MOSFET output conductance in the BSIM 3v3 model and leakage through the protection diodes of the I/O pads.

The area of the core cell of the 0.35µm symmetric SBCS shown in Fig. 5 is around 200x135µm^2. Simulation and experimental results for the current references are compared in Fig. 3 and 4. A statistical analysis chip-to-chip of 40 samples in 0.35µm with correlation coefficient of 0.4 is presented in Fig. 4. It indicates that the major error source in the current generation is the variation of the voltage reference. Also, a slight increase of V_{DDmin} in the SBCS implemented in 0.35µm was generated by an increase in the threshold voltages. These results validate the design and show that the current source can operate at voltages down to the value resulting from (12.b). As can be observed in Figs. 3 and 4(b), the variation of the reference current around the nominal value is relatively low. For AMIS 1.5µm, the average current reference obtained from two sets of five samples with two different layouts is 410pA with a maximum deviation of ±10% at 1.2V supply.

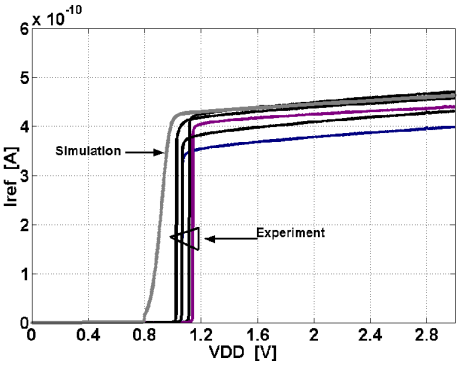


Fig. 3. Current reference AMIS- 1.5µm against supply voltage for the symmetric topology (K=1)

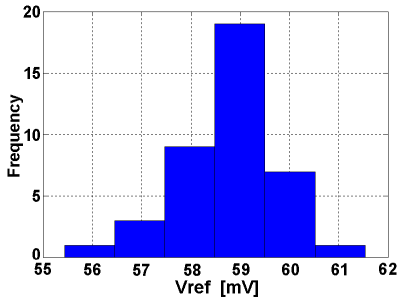


Fig. 4(a). Histogram of V_{ref} for TSMC 0.35µm.

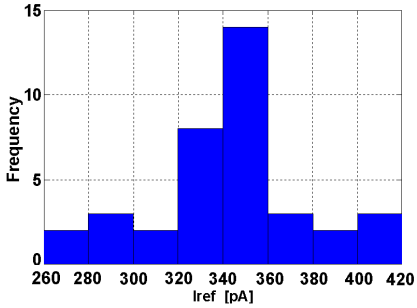


Fig. 4(b). Histogram of I_{ref} for TSMC 0.35µm.

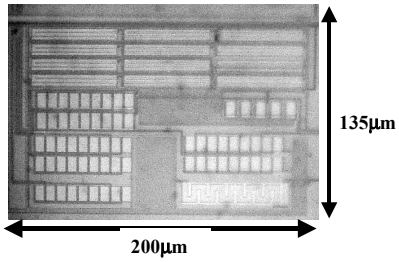


Fig. 5. Micrograph of the symmetric topology in TSMC 0.35µm.

7. CONCLUSIONS

A low-voltage low-power self-biased current-source has been proposed. The proposed circuit is process-independent and reproducible in any standard CMOS technology. Simulation and experimental results have shown that the self-biased current source provides ultra-low-power operation, low sensitivity to changes in the supply voltage, small silicon area and can operate at power supply voltages down to 1.1 V in 1.5µm and 0.35µm CMOS technologies. The SBCS and design methodology proposed here were demonstrated to be particularly suited to very-low-power low-voltage applications.

8. ACKNOWLEDGMENT

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