Fully-Integrated 86 mV – 1V Step-up Converter for Energy Harvesting Applications

Marcio Bender Machado[1,2,3], Marcio Cherem Schneider[1], Mohamad Sawan[3], and Carlos Galup-Montoro[1]
[1]UFSC – Federal University of Santa Catarina, SC, Brazil
[2]IF-Sul – Federal Institute Sul-Rio-Grandense, RS, Brazil
[3]Polystim Neurotech Lab – Polytechnique Montreal, QC, Canada
marciobma@gmail.com

***Abstract*— In this paper, we present a fully-integrated step-up converter for energy-harvesting applications able to operate from supply voltages below $4kT/q \cong 100$ mV. Expressions for the operation of the main blocks of the topology, the enhanced swing ring oscillator and the Dickson charge pump operating at ultra-low-voltages, are derived. A fully-integrated converter design implemented in a 130 nm CMOS technology confirmed the ultra-low-voltage operation of the converter, generating a DC output of 1V at a current consumption of 1 μA from an input voltage of 86 mV.**

Keywords—ultra-low-voltage circuits; ultra-low-voltage DC-DC converters; energy harvesting; zero-VT MOSFET; Dickson charge pump; enhanced swing oscillator.

I. INTRODUCTION

Motivated by energy harvesting applications, the search for boost converters with the ability to operate from ultra-low-voltages (ULV) has never been more intense. Power sources such as solar cells in dark environments, wearable thermoelectric generators and implantable glucose fuel cells [1], which usually generate less than 100 mV, have been presented as important alternatives to power the electronics of modern sensor networks and biomedical applications. However, due to the ultra-low voltages generated by these energy harvesters, the use of a boost converter is mandatory to provide a supply voltage of the order of 1 V, as commonly required in the current electronics sector.

Nevertheless, independently of the step-up converter topology, inductive boost or charge pump, an oscillatory signal is needed in order to control the energy transfer between energy storage devices. However, the generation of oscillations from extremely low voltage energy harvesters represents a 'bottleneck' in the design of ULV converters. Despite the fact that in the last few years some topologies have addressed this subject using either mechanical switches or external devices such as inductors or transformers [2-5], obtaining a fully-integrated solution remains an unsolved problem.

In this paper, we present a fully-integrated converter that operates with very low supply voltages. The converter is suitable for starting up boost converters or directly driving microwatts loads.

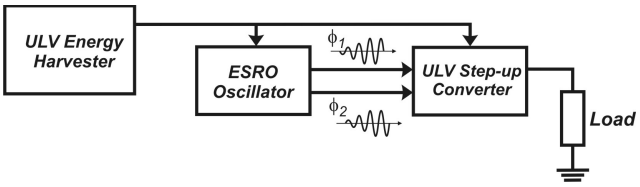

Fig. 1. Proposed topology to boost extremely low voltages.

Using zero-threshold-voltage (zero-VT) transistors, we designed an enhanced swing ring oscillator (ESRO), which can generate oscillations even when powered with voltages below 100 mV. This oscillator, besides providing the AC signal required for the operation of a ULV charge pump (next stage of the topology), boosts the peak-to-peak voltage at its output, increasing the converter output voltage. A model of the ULV charge pump (Dickson converter), taking into account the diode parameters and the load specifications, was developed and is described herein. In order to boost DC levels as low as 100 mV in a fully-integrated version, we designed an eleven-stage Dickson converter built with zero-VT transistors available in a standard CMOS process.

The step-up converter architecture proposed in this paper is presented in Fig. 1. As can be seen in the figure, the oscillator and the converter are powered from the same source.

This paper is organized as follows. In Sections II and III we present the analysis of the ULV oscillator and the modeling of the ULV Dickson converter, respectively. The design of a fully-integrated converter operating down to a supply voltage of 86 mV, along with experimental results, is reported in Section IV. Section V provides a comparison with recent work, and Section VI concludes the paper.

II. THE ENHANCED SWING RING OSCILLATOR (ESRO)

For energy harvesting applications, the oscillator that provides the AC signal for the boost converter must (i) oscillate even when powered with very low supply voltages; and (ii) boost the output magnitude as much as possible in order to improve the overall converter efficiency. The enhanced swing ring oscillator (ESRO) [6] complies with both requirements.

The ESRO is a conventional cross-coupled oscillator that uses a coupling inductor (L_2) between stages. It is able to boost the oscillation amplitude far beyond the supply rails even when operating with very low supply voltages. Moreover, the two

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complementary signals required in the charge pump are naturally obtained with a two-stage ESRO, as shown in Fig. 2, where the charge pump converter (next stage of the topology) is represented as a load indicated by a conductance G_O.

The transfer function of a single stage of the ESRO, according to the model shown in Fig. 3, is

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{\left(g_{md}+G_{P1}+\frac{1}{sL_1}\right)\left[(sC+G_O)(sL_2+R_{S2})+1\right]+sC+G_O} \tag{1}$$

or, equivalently

$$\frac{V_{out}}{V_{in}} = \frac{-g_m}{(g_{md}+G_{P1})\left(1-L_2C\omega^2+G_OR_{S2}\right)+\frac{R_{S2}C}{L_1}+G_O\left(1+\frac{L_2}{L_1}\right)} \times \frac{1}{1+j\left(\frac{\left[(L_1+L_2)C+L_1(R_{S2}C+L_2G_0)(g_{md}+G_{P1})\right]\omega^2-G_0R_{S2}-1}{(g_{md}+G_{P1})\omega L_1\left(1-L_2C\omega^2+R_{S2}G_0\right)+(L_1+L_2)G_0\omega+R_{S2}C\omega}\right)} \tag{2}$$

where g_m and g_{md} represent the MOSFET gate and drain transconductances, respectively, C is the sum of all capacitances between the drain node and the ac ground, R_{S2} is the series resistance of inductor L_2, G_{p1} is the parallel conductance of L_1, and G_o models the output load. The phase shift ϕ between V_{out} and V_{in}, calculated from (2), is

$$\phi = \pi - \tan^{-1}\left(\frac{\left[(L_1+L_2)C+L_1(R_{S2}C+L_2G_0)(g_{md}+G_{P1})\right]\omega^2-G_0R_{S2}-1}{(g_{md}+G_{P1})\omega L_1\left(1-L_2C\omega^2+R_{S2}G_0\right)+(L_1+L_2)G_0\omega+R_{S2}C\omega}\right) \tag{3}$$

For the occurrence of oscillations, the phase shift of the single stage shown in Fig. 2 is π [6][6]; thus, the oscillation frequency ω calculated from (3) is

$$\omega = \sqrt{\frac{G_0R_{S2}+1}{(L_1+L_2)C+L_1(R_{S2}C+L_2G_0)(g_{md}+G_{P1})}} \tag{4}$$

Finally, the greater-than-unity gain required to start up oscillations is achieved for

$$g_m > (g_{md}+G_{P1})\left(1-L_2C\omega^2+G_OR_{S2}\right)+\frac{R_{S2}C}{L_1}+G_O\left(1+\frac{L_2}{L_1}\right) \tag{5}$$

III. The ULV charge Pump Analysis

For ULV operation, the conventional approach involving a constant diode forward voltage drop for the model of the Dickson charge pump [7] shown in Fig. 5 is not applicable. To analyze the Dickson converter down to input voltages of the order of the thermal voltage kT/q or even less, we introduce a converter model which includes both the load current and the more realistic exponential current-voltage characteristic of the diode.

For the N-stage Dickson converter, assuming steady-state operation as in [8], [9] and, for the sake of simplicity, a square signal $V\phi$, the voltage waveform V_D of each diode of the circuit is shown in Fig. 4, where Vd is the diode forward voltage drop, and V_P is the peak voltage of $V\phi$.

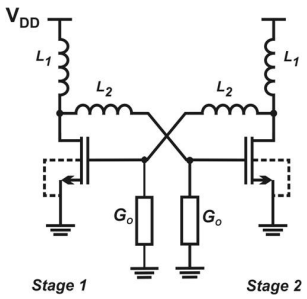

Fig. 2. Schematic diagram of the two-stage enhanced swing ring oscillator (ESRO) with the output load modeled as a conductance G_O.

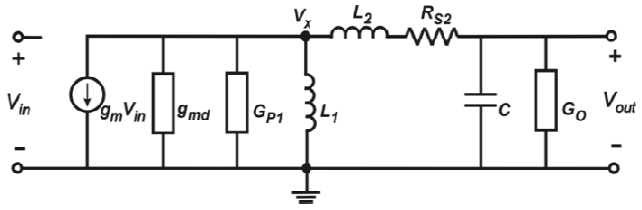

Fig. 3. Simplified small-signal model of a single stage of the ESRO based on the triode MOSFET small-signal model presented in [6].

As can be seen in Fig. 4, one of the terminals of both the leftmost and rightmost diodes, D_1 and D_N, is connected to DC nodes (V_{in} and V_{out}, respectively). The voltage waveforms across them differ from those across the intermediate diodes. For this reason, the forward voltage drop will be the same (V_{d1}=V_{dN}) in the two cases. For the other diodes, the forward voltage drop will be the same (V_{d2}=…= $V_{dN\text{-}1}$). Thus, the DC output voltage of the converter is

$$V_{out} = V_{in} + (2N-2)V_P - 2V_{d1} - (N-2)V_{d2} \tag{6}$$

where N is the number of diodes. To calculate the diode forward voltage drop (V_{d1} and V_{d2}) we assume, as in [8], that the I-V characteristic of the diode follows the Shockley model, *i.e.*,

$$I_D = I_{sat}\left(e^{V_D/n\phi_t}-1\right) \tag{7}$$

where I_{sat} is the saturation current and n is the ideality factor. The average value of each diode current over a complete cycle of the oscillating signal is equal to the load current, I_L, *i.e.*,

$$I_L = \int_{-T/2}^{T/2} I_D dt \tag{8}$$

For the waveforms V_{D1} and V_{D2} (shown in Fig. 4), (8) results, respectively, in

$$\begin{aligned}\left(1+\frac{I_L}{I_{sat}}\right)T &= \int_{-T/2}^{0}\exp\left(\frac{V_{d1}}{n\phi_t}\right)dt + \int_{0}^{T/2}\exp\left(\frac{V_{d1}-2V_P}{n\phi_t}\right)dt \\ \left(1+\frac{I_L}{I_{sat}}\right)T &= \int_{-T/2}^{0}\exp\left(\frac{V_{d2}}{n\phi_t}\right)dt + \int_{0}^{T/2}\exp\left(\frac{V_{d2}-4V_P}{n\phi_t}\right)dt\end{aligned} \tag{9}$$

Assuming that the capacitors are sufficiently high to keep the voltages at each node constant over a half-cycle, the forward voltage drops V_{d1} and V_{d2} are

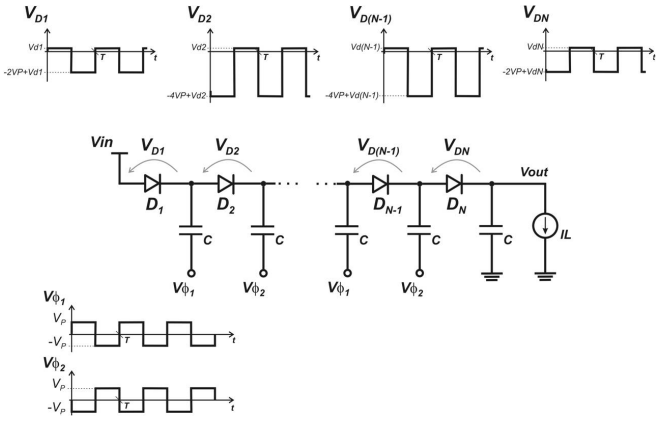

Fig. 4. Dickson charge pump topology.

$$V_{d1} = V_P - n\phi_t \ln\left[\frac{\cosh\left(V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right]$$
$$V_{d2} = 2V_P - n\phi_t \ln\left[\frac{\cosh\left(2V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right] \quad (10)$$

From (6) and (10), we can write the converter output as

$$V_{out} = V_{in} + 2n\phi_t \ln\left[\frac{\cosh\left(V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right] + \left(N-2\right)n\phi_t \ln\left[\frac{\cosh\left(2V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right] \quad (11)$$

Now, assuming that the AC signal is a sinusoid instead of a square wave, the result in (11) can be written [8] as

$$V_{out} = V_{in} + 2n\phi_t \ln\left[\frac{I_0\left(V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right] + \left(N-2\right)n\phi_t \ln\left[\frac{I_0\left(2V_P / n\phi_t\right)}{1 + I_L / I_{sat}}\right] \quad (12)$$

where I_0 is the modified Bessel function of the first kind.

IV. Experimental Results

Based on the theoretical analysis provided herein, we designed and implemented the converter topology shown in Fig. 5 using a conventional IBM 130 nm technology. The main design goal was to reduce the minimum operation voltage of the fully-integrated step-up converter as much as possible. As shown in Fig. 5, the step-up converter is based on a two-stage enhanced swing ring oscillator ESRO connected to a Dickson charge pump.

As regards the oscillator design, the inductors were designed to achieve a relatively high L_2/L_1 ratio (L_1 = 18 nH and L_2 = 66 nH), in order to reduce the minimum V_{DD} required for oscillation. Both inductors have a quality factor Q of around 8 at 500 MHz, which is close to the maximum value reached in the technology under consideration.

The W/L ratio of the zero-VT transistors of the oscillator was determined in order to achieve the required capacitance for a specified oscillation frequency of around 500 MHz. After some fine tuning by simulation, we obtained a W/L ratio of 500 µm/0.42 µm.

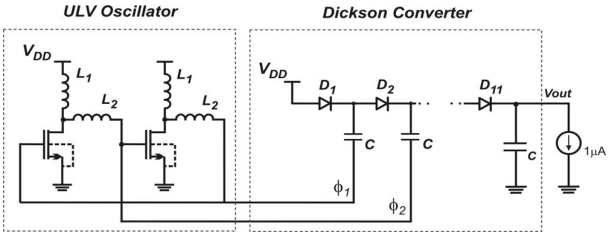

Fig. 5. The step-up converter topology based on a two-stage ESRO connected to a Dickson charge pump.

Bearing in mind the minimum voltage required to start up the converter and the design target of V_{out}=1 V and I_L=1 µA, we implemented an eleven-stage Dickson charge pump, using zero-VT transistors connected as diodes. Zero-VT transistors were used in the charge pump due to their higher saturation current value in comparison with the standard transistor available in the same 130 nm technology. With W/L = 4.2 µm/0.42 µm, the zero-VT transistor connected as a diode presents I_{sat} = 550 nA against I_{sat} = 1.5 nA of the standard transistor with the same aspect ratio.

The micrograph of the chip fabricated in a 130 nm technology is shown in Fig. 6. Wide connection metal lines were used in order to reduce the ohmic losses. In our design we decided to externally connect the oscillator to the Dickson charge pump; in this way, we could test the two components separately.

Considering that a single voltage source was used to supply the oscillator and the charge pump, the fully-integrated prototype of Fig. 6 can start up from 73 mV of V_{DD} at an operation frequency of around 550 MHz. As shown in Fig. 7, the target specification of 1V of output voltage and 1 µA of load current is obtained at V_{dd} = 86 mV, for a power converter efficiency of around 1%. The relation between the input voltage (V_{DD}) and the output power (P_{out}) in terms of the output voltage is also shown in Fig. 7.

As can be seen in Fig. 7, even when built with quality-factor inductors of around 8, the circuit can provide more than 5 µW at the output for an input voltage of around 108 mV.

V. Discussion

In recent years, several topologies and techniques have been proposed in order to start up boost converters with less than 100 mV. However, the solutions so far presented require the use of external devices such as inductors, transformers, capacitors, or mechanical switches [2], [3]. However, some topologies have been proposed considering fully-integrated solutions to start up ULV converters, such as the use of a tuned oscillator [4], at the price of post-fabrication trimming. A comparison between state-of-the-art fully-integrated approaches and our strategy, as regards the minimum start-up voltage and some design characteristics, is shown in Table I. As can be observed, we present a fully-integrated solution which, besides starting up at a supply voltage of 73 mV, is implemented in CMOS standard technologies without the need for post-layout tuning.

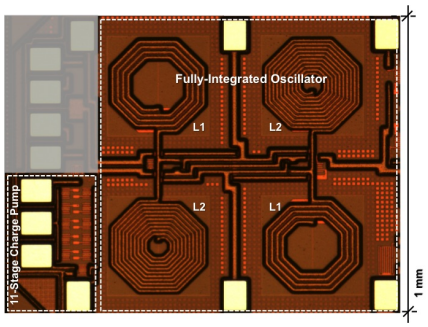

Fig. 6. Chip micrograph of the fully-integrated converter (Fig. 5) implemented in a 130 nm technology.

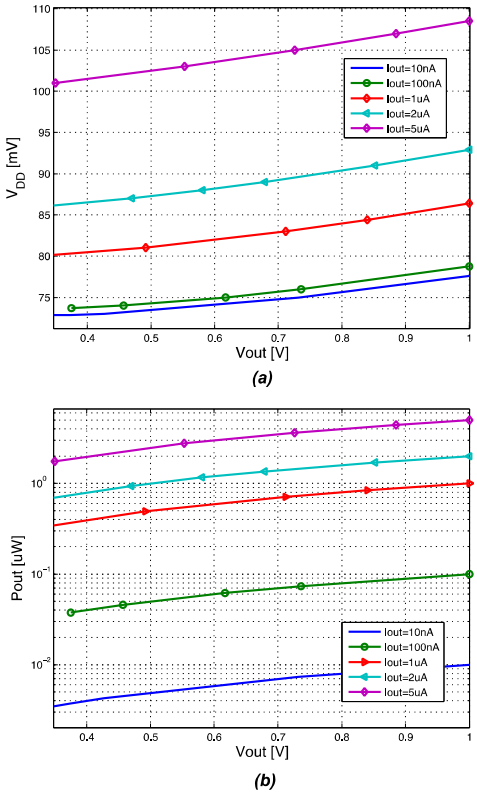

Fig. 7. Experimental relation (measured with the prototype of Fig. 6) between (a) the supply voltage (V_{dd}=V_{in}) and (b) the output power (P_{out}), of the fully integrated converter in terms of the output voltage, for a load current ranging from 10 nA to 5 µA.

To the best of our knowledge, this is the lowest supply voltage at room temperature ever reported for a fully-integrated step-up converter in a conventional CMOS technology.

I. Conclusions

In this paper, we have presented an ultra-low-voltage step-up converter topology that can operate with supply voltages of less than 100 mV, even when built with fully-integrated inductors, with quality factors of the order of 8.

TABLE I. Comparison between some state-of-the-art fully integrated start-up converters.

Ref.	Min. start up	Start-up topology	Process	Characteristics
[4]	80 mV	Charge pump	65 nm	Post-layout threshold voltage adjustment
[5]	270 mV	Charge pump	0.13 µm	Fully-integrated
[10]	100 mV	AC/DC multiplier	0.18 µm	Fully-integrated – simulated results
[10]	100 mV	Charge pump	0.18 µm	Fully-integrated – simulated results
This study	73 mV	Charge pump	0.13 µm	Fully-integrated

Accurate analysis considering the start-up conditions of the oscillator and the charge pump output voltage was performed based on the physical parameters of the diode and the load current. Experimental results obtained with a fully-integrated prototype implemented in a 130 nm process verified the possibility of boosting a voltage level as low as 86 mV to the voltage levels required by present day electronics.

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