

A 20 μ W, 50 mV, Fully-Integrated Cross-Coupled Oscillator for On-Body IoT Applications

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Abstract—An ultra-low-power oscillator for on-body-devices wireless transmitters is designed and implemented in 130 nm CMOS process. This paper explores the reduction of the supply voltage to reduce the power consumption of LC oscillators used in transmitters, complying with imperative requirements of low power dissipation for connected on-body and implanted medical devices. The limits of the voltage supply reduction on the performance of the LC oscillators are researched and important parameters such as phase noise, power consumption and the typical figure of merit are inspected. Measurements results show that the oscillator achieves -88 dBc/Hz of phase noise for a 50-mV supply voltage and -111 dBc/Hz for 200 mV at $Df = 200$ kHz, while consuming only 20 mW and 118 mW of DC power, respectively.

Keywords — ultra-low-voltage, ultra-low-power, MICS band, LC oscillator, cross coupled oscillator.

I. INTRODUCTION

The human body has a strong potential for different Internet of Things (IoT) applications such as wearable health monitoring devices, connected implanted medical devices, real-time streaming, aids for sports training, etc. [1]. In order to establish the communication between on-body devices, protocol standards such as IEEE 802.15.6 have been developed, allowing the deployment of short-range wireless body area networks (WBANs) with low power consumption, meeting the requirements of device portability and battery size and even enabling autonomous devices supplied by energy harvesters. The frequency band of 402–405 MHz, which is allocated for medical implant communication services (MICS) by the Federal Communications Commission (FCC), is of special interest for WBANs applications. This band is used for implantable applications and provides appropriate propagation through human tissues using antennas of moderate size [2].

In an implantable WBAN device, the RF transceiver is responsible for most of the power consumption; therefore, low-power oscillators are desirable to reduce the power consumption in the transceiver. In the frequency range of 400 MHz, LC oscillators operating at V_{DD} around 1 V [3]–[4] are commonly adopted in WBAN devices, providing appropriate phase noise performance at the expense of relatively high power-consumption. Recent works (870 mV [5], 700 mV [6]) exploit the reduction of the supply voltage of LC oscillators, but the power consumption is of the order of hundreds of mW. The adoption of ring oscillators (ROs) with reduced supply voltage (600 mV [7], 500 mV [8]) is also a common strategy to decrease power consumption, although at a poorer phase noise performance when compared to LC oscillators.

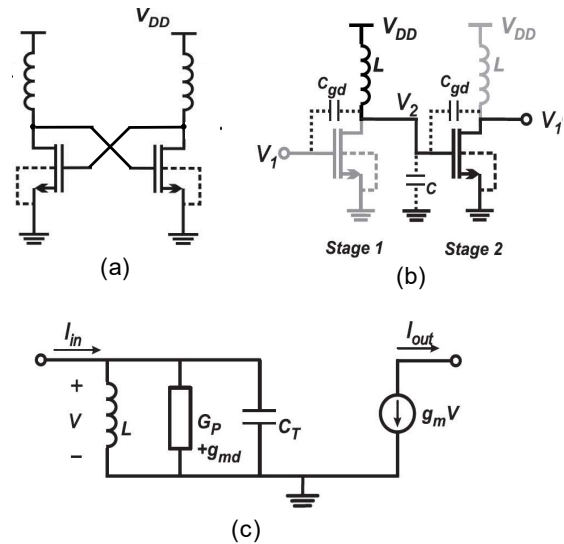


Fig. 1. (a) The cross-coupled oscillator; (b) a single stage, considering the interaction between the adjacent stage; (c) simplified small-signal model of a single stage of the cross-coupled oscillator.

In this paper we present the design and realization of an ultra-low-power LC oscillator operating at a frequency around 400 MHz aimed to investigate the limits of power supply reduction and its effects on the oscillator performance. The effect of the reduced supply voltage on the oscillator consumption, phase noise and in the typical figure of merit (FOM) is experimentally verified. This paper is organized as follows: Section II provides the theoretical background for the oscillator design. Section III presents the design and experimental results of the implemented prototype, as well as a comparison of the prototype with state-of-the-art designs. Section IV draws the conclusions.

II. THE CROSS-COUPLED OSCILLATOR

The inductive ring oscillator (IRO) presented in [9] and [10] can operate from low supply voltages but with an amplitude of oscillation beyond the supply voltages. When the number of stages of the IRO is equal to 2, the IRO is reduced to the widely used cross-coupled LC oscillator (XCO) shown in Fig. 1 (a).

The analysis of the XCO is based on the simplified small-signal equivalent circuit of a single stage, shown in Fig. 1 (b) and (c), where g_m and g_{md} represent the gate and drain transconductances, respectively and G_P models the inductor losses. The value of C_T is

$$C_T = C + 4C_{gd}, \quad (1)$$

where C , is the sum of all capacitances between the drain node and the AC ground and C_{gd} models the gate-drain capacitance of a single stage.

The transfer function of the single stage in Fig. 1(c) is given by

$$\frac{I_{out}}{I_{in}} = -\frac{g_m}{g_{md} + G_P + \frac{1}{sL} + sC_T}. \quad (2)$$

The condition of loop gain equal to unity for oscillation requires the phase shift between the two stages of the XCO to be $\phi = \pi$. Therefore, from (2), we can calculate the oscillation frequency ω as

$$\omega = \frac{1}{\sqrt{LC_T}}. \quad (3)$$

According to the Barkhausen criteria, the loop gain needs to be equal to or slightly higher than unity, *i.e*

$$\frac{g_m}{g_{md}} \frac{1}{1 + \frac{G_P}{g_{md}}} \geq 1. \quad (4)$$

Since the relation between source, drain and gate transconductances, g_{ms} , g_{md} , and g_m , respectively, is $g_m = (g_{ms} - g_{md})/n$ [11], where n is the transistor slope factor, the minimum transistor gain g_{ms}/g_{md} required for oscillation is obtained from (4) as

$$\frac{g_{ms}}{g_{md}} \geq 1 + n \left(1 + \frac{G_P}{g_{md}} \right). \quad (5)$$

In this paper we have used the Advanced Compact Model (ACM) [11] for MOSFETs, which presents equations valid in all operation regions. From this model, the drain-source voltage (V_{DS}) can be expressed in terms of the drain and source transconductances as

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S} g_{md} \left(\frac{g_{ms}}{g_{md}} - 1 \right) + \ln \frac{g_{ms}}{g_{md}}. \quad (6)$$

Since $V_{DS} = V_{DD}$, the substitution of (5) into (6) yields

$$V_{DD} \geq \frac{\phi_t^2}{2I_S} n g_{md} \left(1 + \frac{G_P}{g_{md}} \right) + \phi_t \ln \left[1 + n \left(1 + \frac{G_P}{g_{md}} \right) \right]; \quad (7)$$

Thus, from (7), the minimum supply voltage when the transistors operate in weak inversion is

$$V_{DD} \geq \phi_t \ln \left[1 + n \left(\frac{g_{md} + G_P}{g_{md}} \right) \right]. \quad (8)$$

Assuming that the inductors are lossless, the supply voltage limit of (8) is given by

$$V_{DD} = \phi_t \ln(1 + n). \quad (9)$$

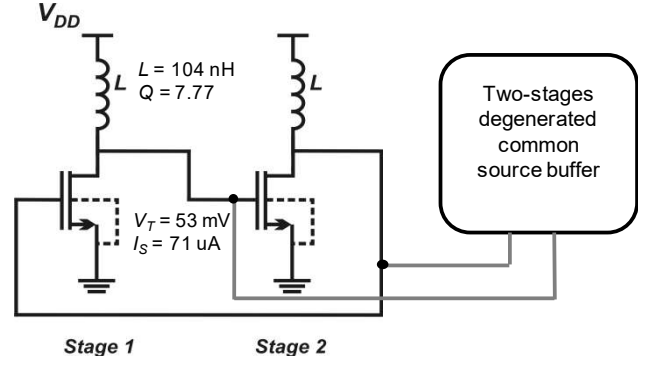


Fig. 2. Schematic diagram of the cross-coupled oscillator along with the voltage buffer. Inductor parameters extracted at 400 MHz; MOSFET parameters experimentally extracted.

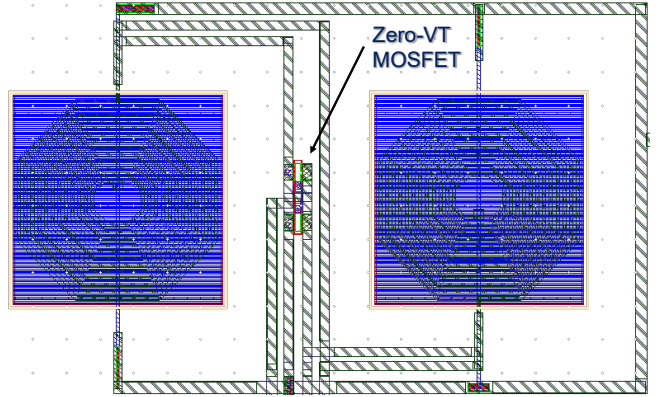


Fig. 3. Layout of the fully integrated cross-coupled oscillator fabricated in the CMOS RF 130 nm technology.

Assuming that $n=1$, the theoretical limit given by (9) is around 18 mV at room temperature. As can be seen in the next section, using large native transistors the limit of 50 mV of power supply can be achieved even using integrated inductors. The design and the experimental results are presented in Section III.

III. EXPERIMENTAL RESULTS

From the oscillation frequency specification of around 400 MHz, we designed a cross-coupled oscillator for on-body IoT applications in CMOS RF 130 nm technology. To reduce the power consumption of the LC oscillator, our strategy was to reduce the supply voltage to 100 mV, or even less. Native transistors were employed to maintain the necessary current drive capability at voltages below 100 mV.

In order to maximize the inductor quality factor for the frequency of 400 MHz, we employed a high integrated inductance of around 104 nH and quality factor around 7.7, both values characterized by the Spectre simulator at the design frequency. Once the inductor parameters are known, a wide zero-VT transistor ($W/L = 180 \mu\text{m}/420 \text{ nm}$) was designed to reach two goals. The first one was to provide enough drive capability to compensate the inductor losses, while the second one was to achieve the required capacitance for the specified oscillation frequency. The transistor was built as a parallel association of $30 \times 6 \mu\text{m}$ -width transistors with minimum channel length for the zero-VT device.

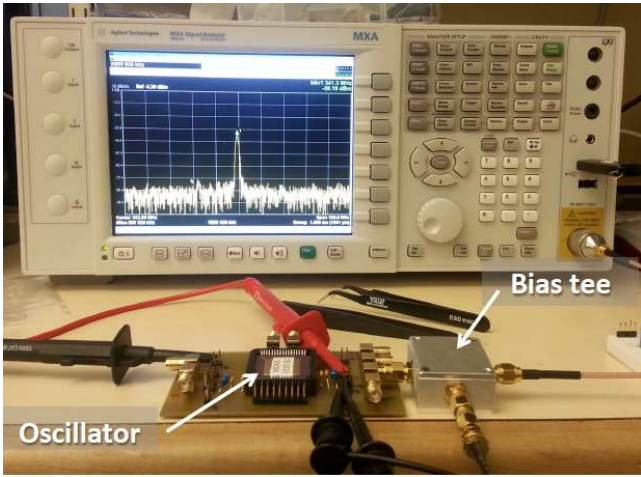


Fig. 4. Photograph of the oscillator being tested by spectrum analyzer Agilent MXA 9020A.

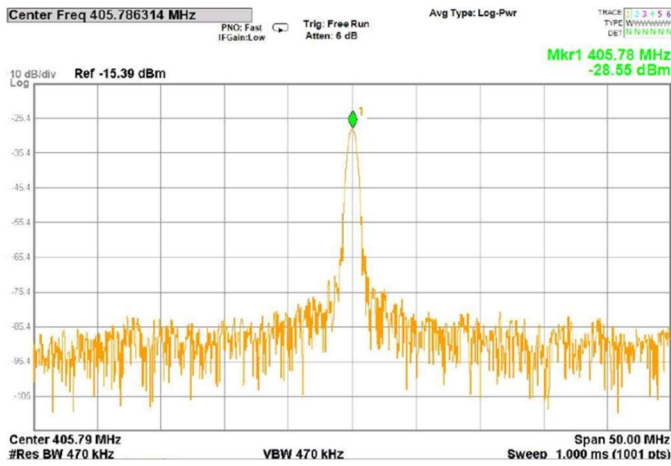


Fig. 5. Spectral diagram of the signal of the two-stage LC oscillator at $V_{DD}=50$ mV.

Since the main purpose of this work was evaluate the performance of the oscillator under ultra-low-voltage operation, with no strict requirements for frequency accuracy, no adjustable capacitor was used for fine-tuning the frequency. In order to characterize the circuit, a 50 W degenerated common source buffer was coupled to the oscillator output. The DC buffer was biased through a commercial bias tee circuit, the Mini-Circuits ZFBT-4R2G+.

The layout of the circuit, implemented in the CMOS RF 130 nm technology, is shown in Fig. 3. To operate at such a low voltage, a special layout was designed to decrease the parasitics. As can be seen in Fig. 3, ohmic losses were attenuated using large paths from the last two metal layer available in the process. In some key paths a sandwich, composed of the two last metal layers shorted by hundred vias, was employed to reduce the ohmic losses and decrease even more the minimum voltage to start-up the oscillator.

Using the Keithley source meter 2450 and spectrum analyzer Agilent MXA 9020A, the minimum voltage to start up oscillations, the DC power consumption and the oscillation frequency were measured. Fig. 4 shows the test bench. The spectrum of the signal generated by the XCO for $V_{DD}=50$ mV is shown in Fig. 5. For this supply voltage, the power consumption is around 20 μ W.

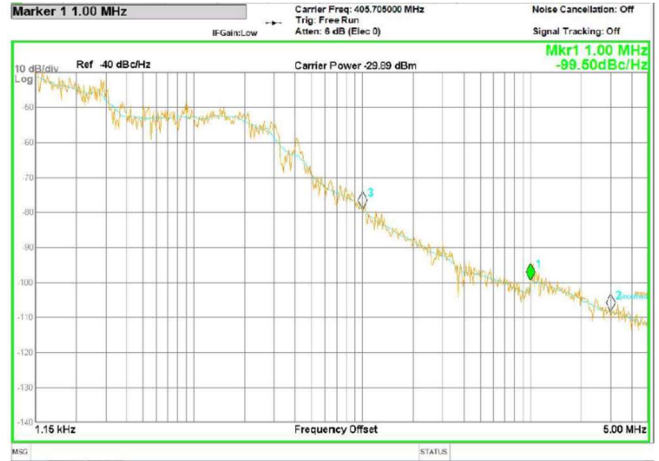


Fig. 6. Measured phase noise of the two-stage LC oscillator at $V_{DD}=50$ mV.



Fig. 7. Measured phase noise of the two-stage LC oscillator at $V_{DD}=200$ mV.

The oscillator phase noise ($L\{Df\}$), measured with the Agilent N9068A for $V_{DD} = 50$ mV, is -88 dBc/Hz as can be seen in Fig. 6. For $V_{DD} = 200$ mV, the measured phase noise is -111 dBc/Hz (Fig. 7), while consuming 118 μ W of DC power. Both phase noise values were measured at $Df = 200$ kHz. The output voltage taken at the buffer output, for $V_{DD} = 50$ mV, is shown in Fig. 8.

The variation on the minimum supply voltage and DC power consumption at $V_{DD} = V_{DD,min}$ is shown in Fig. 9, for five samples of the oscillator. As can be seen, the differences in the startup voltages of the five samples does not exceed 2 mV. It is worth mentioning the extremely low power consumption, of an average value of around 12 μ W, for all samples.

Table I shows a comparison of the oscillator designed herein with others for similar applications. The data shows that the oscillator designed in this study presents a remarkably low power consumption with acceptable phase noise characteristics, opening new opportunities for extremely low power RF applications. The LC oscillator powered with ultra-low V_{DD} can provide lower power consumption and, at the same time, better phase noise performance and better FoM when compared to ring oscillators. In Table I, the oscillator figure of merit (FoM) is given by

$$FoM = L\{\Delta f\} + 10 \log\left(\frac{P_{DC}}{1 \text{ mW}}\right) - 20 \log\left(\frac{f_0}{\Delta f}\right) \quad (10)$$

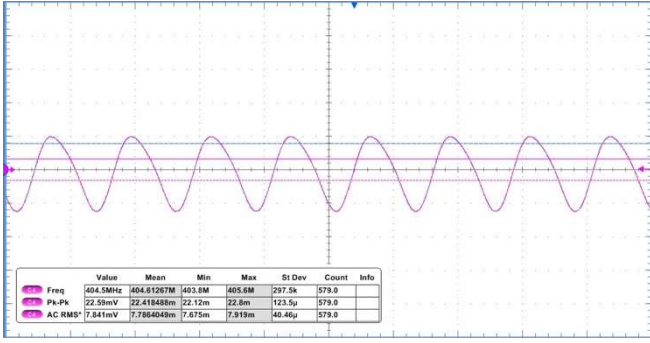


Fig. 8. The oscillator waveform taken at the buffer output for $V_{DD} = 50 \text{ mV}$. Scale: X = 10 mV/div; Y = 2 ns/div.

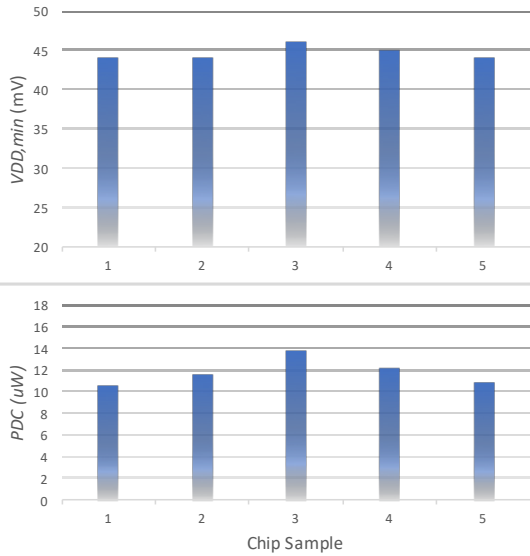


Fig. 9. $V_{DD,min}$ and power consumption at $V_{DD,min}$ for five chips.

TABLE I - Comparison with the state of the art oscillators .

Ref.	V_{DD} (V)	Power (mW)	Phase Noise (dBc/Hz)	Process	Freq. (Mhz)	FoM (dBc/Hz)	VCO Type
[12]	-	600	-106@100kHz	130 nm	405	-156	LC
[8]	0.5	60	-82@1MHz	180 nm	82-370	-145.5	RO
[6]	0.7	430	-115.25@200 kHz	130 nm	382-412	-185	LC
[7]	0.6	146	-86.38@1 MHz	65 nm	250-800	-153	RO
[5]	0.87	480	-110@200 kHz	130 nm	386-408	-175.8	LC
[3]	1	430	-102.1@200 kHz	180 nm	400-405	-171.9	LC
[4]	1	600	-95@100 kHz	130 nm	380-440	-169	LC
This work @ 50 mV	0.05	20	- 88@200 kHz	130 nm	405	-171	LC
This work @ 200mV	0.2V	118	-111@200 kHz		349	-185	

IV. CONCLUSION

An ultra-low-voltage oscillator for on-body connected devices was designed and implemented in CMOS RF 130 nm process. The phase-noise and power consumption were measured for different low values of V_{DD} , validating the application of the circuit in ultra-low-power transceivers. The results show that the LC oscillator powered with ultra-low V_{DD} presented here, takes full advantage of both low phase noise and reduced power consumption, which are important requirements for portable and autonomous connected devices in the IoT scenario.

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REFERENCES

- [1] S. Movassaghi, M. Abolhasan, J. Lipman, D. Smith and A. Jamalipour, "Wireless body area networks: A survey," *IEEE Communications Surveys & Tutorials*, vol. 16, no. 3, pp. 1658-1686, Third Quarter 2014.
- [2] R. Chavez-Santiago et al., "Propagation models for IEEE 802.15.6 standardization of implant communication in body area networks," *IEEE Communications Magazine*, vol. 51, no. 8, pp. 80-87, August 2013, doi: 10.1109/MCOM.2013.6576343.
- [3] J. Yang and E. Skafidas, "A Low Power MICS Band Phase-Locked Loop for High Resolution Retinal Prosthesis," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 4, pp. 513-525, Aug. 2013, doi: 10.1109/TBCAS.2012.2220545.
- [4] K. W. Li, K. N. Leung and L. L. K. Leung, "Sub-mW LC Dual-Input Injection-Locked Oscillator for Autonomous WBSNs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 3, pp. 546-553, March 2013, doi: 10.1109/TVLSI.2012.2189029.
- [5] M. Nenadovic, N. Fiebig, G. Fischer, D. Kissinger and J. Wessel, "A 0.48 mW fully integrated MICS band VCO in SiGe BiCMOS technology for medical implant communication," *2018 IEEE Radio and Wireless Symposium (RWS)*, Anaheim, CA, USA, 2018, pp. 1-3, doi: 10.1109/RWS.2018.8304929.
- [6] J. Bae, S. Radhapuram, I. Jo, T. Kihara and T. Matsuoka, "A low-voltage design of digitally-controlled oscillator based on the gm/ID methodology," *2015 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Sendai, Japan, 2015, pp. 187-189, doi: 10.1109/RFIT.2015.7377929.
- [7] Z. Saheb, E. El-Masry and J. Bousquet, "Ultra-low voltage and low power ring oscillator for wireless sensor network using CMOS varactor," *2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, Vancouver, BC, Canada, 2016, pp. 1-5, doi: 10.1109/CCECE.2016.7726620.
- [8] Li Tianwang, Jiang Jinguang, Ye Bo and Han Xingcheng, "Ultra low voltage, wide tuning range voltage controlled ring oscillator," 2011 9th IEEE International Conference on ASIC, Xiamen, China, 2011, pp. 824-827, doi: 10.1109/ASICON.2011.6157332.
- [9] M. B. Machado, M. C. Schneider and C. Galup-Montoro, "On the Minimum Supply Voltage for MOSFET Oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 2, pp. 347-357, Feb. 2014, doi: 10.1109/TCSI.2013.2278344.
- [10] Machado, M.B., Schneider, M.C. & Galup-Montoro, C. Fully integrated inductive ring oscillators operating at VDD below $2kT/q$. *Analog Integr Circ Sig Process* 82, 5–15 (2015). <https://doi.org/10.1007/s10470-014-0440-8>
- [11] M. C. Schneider and C. Galup-Montoro, "CMOS Analog Design Using All-Region MOSFET Modeling," *Cambridge University Press*, 2010.
- [12] H. Wang, S. H. Hesari, S. Shamsir and S. K. Islam, "MICS Band Digital Voltage-Controlled Oscillator (DVCO) for Low-Power Biomedical Data Transmission," *2019 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRS)*, Boulder, CO, USA, 2019, pp. 1-2, doi: 10.23919/USNC-URSI-NRS.2019.8712888.