EXTRACTION OF ELECTRICAL PARAMETERS OF FLOATING GATE DEVICES FOR CIRCUIT ANALYSIS, SIMULATION, AND DESIGN

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ABSTRACT

We propose a structured methodology to extract the electrical parameters of floating gate devices. The characterization of a FG structure requires only two parameters in addition to the conventional MOSFET parameters. This additional set of parameters represents the charge on the FG and the total capacitive coupling of the FG with the control gate. We have characterized the FG device through a comparison of its characteristics with those of a reference transistor. Then we used analytical and simulation MOSFET models in conjunction with the extracted parameters to show the validity of our approach. Our methodology can be applied for the characterization of both flash memories and multiple-input FG devices. Both analytical and simulation models are shown to be in good agreement with experimental results in a 0.35µm CMOS technology.

1. INTRODUCTION

Floating gate (FG) cells find use in non-volatile memories, analog and digital circuits. They consist of an electrode surrounded by an insulator, with no direct electrical connection to any other conductor [1]. The FG electrode acts as the gate of a MOSFET, which serves as the sensor transistor. The potential on the FG can be modified either by capacitive coupling with other conductors or by changing the charge stored on the FG.

The accurate characterization of FG devices is a very challenging task since it requires indirect measurement of some parameters like the capacitive coupling coefficients and the charge stored on the FG. One of the main difficulties to characterize FG parameters stems from the nonlinear nature of the capacitive coupling coefficients, which are often assumed to be constant to simplify device characterization.

For flash memories, there exist several different methodologies to extract the FG device parameters. In a simplified procedure [2], the capacitive coupling ratios can be determined from DC measurements in both the memory cell and in a "dummy cell". In this paper we will follow a similar approach.

The basic idea behind the characterization of the FG device is to consider that the FG device is simply a MOSFET with some capacitive couplings. Therefore, we can take advantage of existent MOSFET models to derive representations and extraction procedures for FG devices.

The analytical MOSFET model to be used here is the one-equation all-region *Advanced Compact MOSFET* (ACM) model proposed in [3]-[4]. We have compared measurements in both the FG device and in a "dummy cell" to extract the coupling coefficient and the equivalent DC voltage developed at the FG (the "dummy cell" is a reference NMOS transistor with the same channel geometry as the FG device). Using this small set of parameters we were able to simulate at both the analytical and transistor levels to demonstrate the accuracy of the extraction procedure.

The direct *dc* simulation of FG devices is not possible because there is no *dc* path from FG to ground [5]. The usual approach to the static simulation of a FG cell is to use a macromodel represented by one or more controlled voltage sources between the FG and ground [6]. The controlled voltage sources represent the dependence of the FG voltage on the transistor's terminals and the charge stored on the FG.

An alternative to the use of a macromodel for *dc* simulation is transient simulation in which the FG is pre-charged at the beginning of the simulation. This method can be used effectively for *dc*, *ac* and transient analysis by using an appropriate set of input signals, i.e. ramp for *dc*, sine for *ac*, etc.

Highlights of our proposed approach are:

1. A methodology for the extraction of parameters of FG devices.
2. The association of the model of a FG device with existent simulation/analytical models of the MOSFET.
3. The modification of a known device macromodel of FG devices to include the extracted parameters.
4. An alternative *ac* and *dc* simulation method of a FG device using transient analysis.

The overall goal is to obtain a small set of parameters that can be shared by models of FG devices. The parameters to be measured are a total coupling coefficient α_{CG} and an equivalent voltage on the FG V_{EQ} or, alternatively, the equivalent subthreshold factor n^{CG} and the equivalent threshold voltage V_T^{CG}. These parameters should be obtained from simple DC transfer characteristics such as I_D vs. V_G plots, for both the "dummy cell" and the FGMOS device with no special setup.

The paper is organized as follows. In Section 2, we describe the floating device. In Section 3, we introduce the analytical and simulation models and the parameter extraction methodology. In Section 4, we show how the analytical and simulation models can be associated through a small set of parameters obtained from the extraction methodology. In Section 5, we summarize the main results of this work.

2. FLOATING GATE DEVICES

In Figure 1, we show a) the symbol representing a *multiple input FG MOS* (MI-FGMOS) transistor, b) its layout, c) its capacitive equivalent model, d) a macromodel suitable for dc simulation and e) a switched structure appropriate for transient simulation. Another coupling terminal (V_w) can be added to the layout when the transistor's FG is laid out on top of an n-well diffusion, as shown in Figure 1b; this input through the well can serve two different purposes: to isolate noise coupling from the substrate and/or to add an additional controlling voltage that can be used either for calibration or for signal modulation.

The FG is isolated from the *controlling gates* (CG) by a capacitive device C_{CG} as shown in Figure 1e, which is formed between two polysilicon layers ($C_{CG}=C_1+C_2+..+C_N$ if the controlling gates are tied together). The FG is coupled to the substrate and to the transistor terminals by several capacitors, which, for the purpose of analysis of the coupling between the controlling gate and the floating gate, form an equivalent capacitor C_{FG} composed of a combination of linear and non-linear capacitors. The dominant component of capacitor C_{FG} is either $C_{fg\text{-}b}$, the one formed between the FG and the bulk, or C_w between the FG and the isolation well. In [7] we give a thorough definition of the parasitic capacitances.

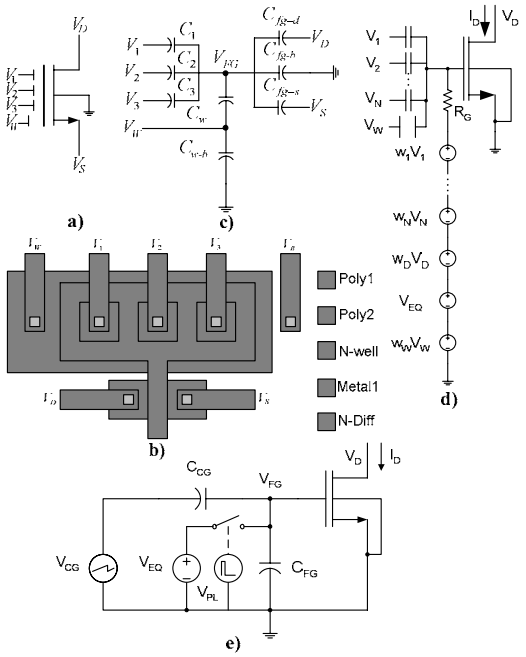

Figure 1. MI-FGMOS transistor. a) Symbolic representation. b) Layout representation. c) Equivalent capacitive circuit. d) Macromodel. e) Switched structure.

To obtain the fundamental design parameters, we assume the capacitive voltage divider representing the FG cell to be linear over the measurement range. Then, we find that

$$V_{FG} = V_{EQ} + \alpha_{CG} V_{CG} \quad ; \quad \alpha_{CG} = \frac{C_{CG}}{C_{FG} + C_{CG}} \tag{1}$$

where α_{CG} is the coupling coefficient associated with the control gate and V_{EQ} is an equivalent voltage at the FG obtained for the voltage at the controlling gate (V_{CG}) extrapolated to zero. V_{EQ} depends on both the charge stored on the FG and the *dc* voltages applied to the MOSFET terminals.

Assuming that (1) is valid for FG voltages close to the threshold voltage, we can define the equivalent threshold voltage factor referred to the accessible controlling gate and the equivalent subthreshold as

$$V_T^{CG} = 1/\alpha_{CG}\left(V_T - V_{EQ}\right); \quad n^{CG} = n/\alpha_{CG} \tag{2}$$

where V_T is the MOSFET threshold voltage and n is the subthreshold parameter. The threshold voltage and the slope factor, both referred to the substrate, are the two parameters to be extracted required to analyze the FG cell using the ACM model.

3. FLOATING GATE MODELING

In this paper, we propose the use of the ACM model for analytical representation of the FG device, a macromodel suitable for DC simulation, a model suitable for transient simulation, and a set of extracted parameters that will help us to associate these models.

3.1 One-equation all-region ACM model

In the current-based ACM model, all the operating regions are represented by one equation, all the MOSFET static and dynamic characteristics are written as functions of two normalized currents, namely the forward and reverse currents [3]-[4]. We have characterized the MOSFET and the FG device in saturation; thus, the reverse current can be neglected. Therefore, we assume the transistor current I_D to be equal to the forward current

$$I_D = I_F - I_R \cong I_F \tag{3}$$

The inversion level or normalized current i_f at the source is the forward current I_F, normalized with respect to the normalization (specific) current I_S.

$$i_f = \frac{I_D}{I_S} = \frac{I\left(V_G, V_S\right)}{I_S}; \quad I_S = \mu n C_{ox}' \frac{\phi_t^2}{2} \frac{W}{L} \tag{4}$$

where V_G and V_S are the voltages at the gate and at the source, respectively. The remaining parameters are technology and design dependent and their definition can be found in [3]-[4].

3.2 Measurement results

For all the measurements we will refer to MI-FGMOS devices with all the inputs driven by a common driving signal. From I_D vs. V_{GS} plots for both a reference NMOS transistor ("dummy cell") and a reference MI-FGMOS device we present the methodology to extract a small set of meaningful parameters to be used for both hand calculations and simulations. The extraction procedure is shown using the TSMC 0.35µm technology available through MOSIS (T13Q 2P4M run). The transistors dimensions are W=1.8µm and L=0.8µm. For all measurements V_{DS}=0.8V. The MI-FGMOS has three capacitive inputs, each of them with an area of 3.2µm x 3.2µm which corresponds to C_i~8.8fF. The drawn area of the n-well is 12.8µm x 5.2µm.

3.2.1 Slope factor (*n*) measurement

To obtain the value of the slope factor *n*, we plotted the I_D vs. V_{GS} curve in weak inversion (WI) as shown in Figure 2. We measured *n* according to the expression

$$1/n = \phi_t \, d\ln(I_D)/dV_{GS} \tag{5}$$

For the NMOS transistor, *n*=1.46 and for MI-FGMOS, n_{CG}=2.46. The coupling coefficient can be estimated from the ratio of the slope factors, according to (2), resulting in $\alpha_{CG}\approx 0.6$.

3.2.2 Normalization current (I_S) measurement

A very appropriate method to measure the normalization current I_S is through g_{ms} (source transconductance) and with good precision through g_{mg} (gate-transconductance) measurements [3]-[4]. For the sake of clarity, the method based on g_{ms} is repeated here. The expression for g_{ms} in saturation is given by

$$g_{ms}\phi_t / I_D = 2/\left(\sqrt{1+i_f}+1\right) \tag{6}$$

where $g_{ms}\phi_t/I_D = -(\Delta I_D/I_D)/(\Delta V_S/\phi_t)$ is the percent variation of I_D relative to $\Delta V_S/\phi_t$.

In WI, the transconductance-to-current ratio is given by

$$g_{ms}/I_D = 1/\phi_t\big|_{i_f \ll 1} \tag{7}$$

while, for i_f=8

$$g_{ms}/I_D = 1/2\phi_t\big|_{i_f \sim 8} \tag{8}$$

Note that the g_m/I_D at i_f=8 is ½ its value in WI. The procedure to determine the normalization current from the I_D/ϕ_t g_{mg} vs. I_D curve is shown in Figure 3; the current at which the current-to-transconductance ratio is twice the WI value, is approximately 2μA, which corresponds to 8*I_S, then $I_S\approx$250μA for both NMOS and FGMOS. The FG device and reference transistor have identical channels, thus, the normalization current should be the same for both devices.

3.2.3 Measurement of the capacitive coupling coefficient (α_{CG}) and the equivalent voltage (V_{EQ})

Since the NMOS reference transistor and the FGMOS device should display the same current for equal gate and FG voltages respectively, the plot of V_G vs. V_{CG} for the same current gives us $\alpha_{CG}\approx$0.64 as the slope and $V_{EQ}\approx$0.26 as the intersect with the V_G axis. The value of the coupling coefficient measured from Figure 4 is slightly different from the one measured from the subthreshold slope since Figure 4 includes both weak and strong inversion. The measurement of V_{EQ} is fundamental for characterization purposes since it allows quantifying the effects of the charges stored on the FG. The procedure is shown in Figure 4.

3.2.4 Threshold voltage (V_T) measurement

According to the ACM model,

$$\left(V_{GS}-V_T\right)/\left(n\phi_t\right)\big|_{v_{SB}=0} = \sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right) \tag{9}$$

When i_f=3, then $V_{GS}=V_T$. From the I_D vs. V_{GS} curve, we can measure the gate to source voltage such that $I_D=3I_S$ and this will correspond to the value of V_T. This procedure is shown in Figure 5 using a normalized i_f vs. V_{GS} plot. The extracted values are $V_T\approx$0.60V and $V_T^{CG}\approx$0.52V.

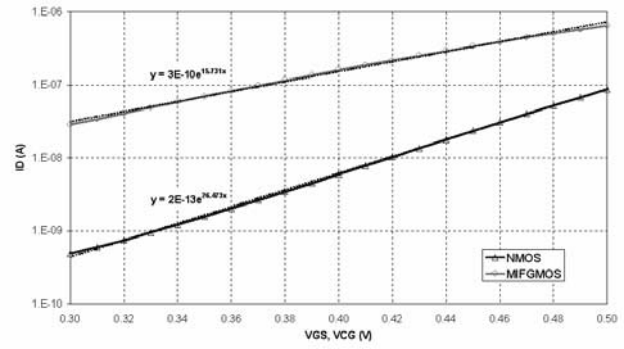

Figure 2. I_D vs. [V_{GS}, V_{CG}] in WI inversion, *n*=1.46 and n^{CG}=2.46.

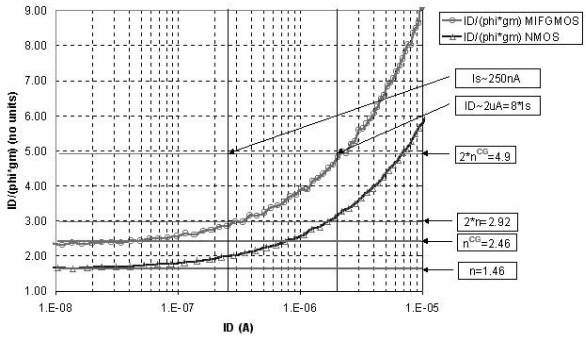

Figure 3. I_D/ϕ_t g_{mg} vs. I_D for NMOS transistor and MI-FGMOS device, $I_S\approx$250nA.

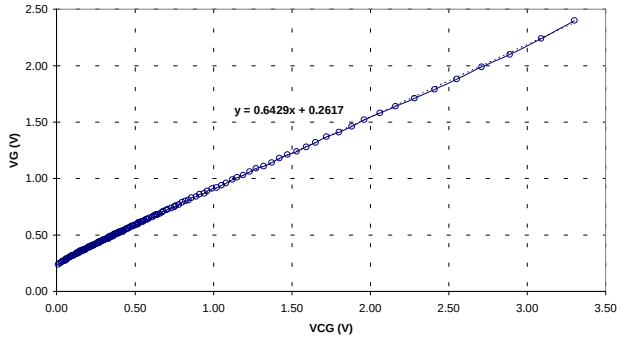

Figure 4. V_G vs. V_{CG}, α_{CG}=0.6429 and V_{EQ}=0.2617.

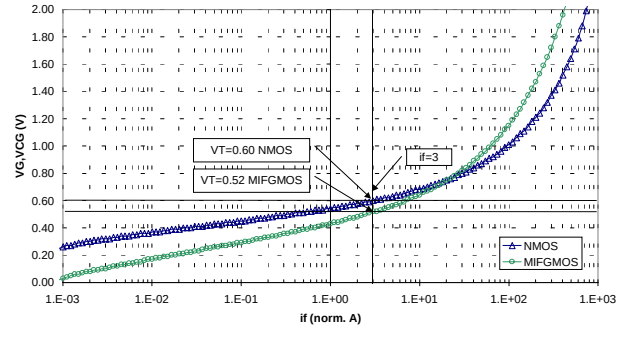

Figure 5. [V_G,V_{CG}] vs. i_f. V_T=0.6V and V_T^{CG}=0.52V.

3.3 Simulation of the FG device.

To overcome the simulator *dc* convergence problem, several macromodels have been proposed. In our work, we have used the technique presented in [6] and modified it to include both the capacitor formed between the FG and the substrate (or n-well) and the effect of the equivalent voltage at the FG. Figure 1d shows the implementation of this extended macromodel. The only parameters required for simulation by the *dc* macromodel are the total coupling coefficient α_{CG} for the voltage controlled voltage sources and the equivalent voltage V_{EQ}. In Figure 1d, $V_1..V_N$ denote the voltages applied to the controlling gates, V_D is the drain voltage, and V_W is the well voltage. Assuming that the input capacitors are equally sized, the coupling coefficient for each input can be expressed by

$$w_m = \alpha_{CG} / N \qquad m = 1,..,N \tag{10}$$

where w_m denotes the mth coupling coefficient, w_D sets the coupling between the FG and the drain and w_w represents the coupling between the FG and the n-well. In our simulations, we assumed both V_D and V_W to be constant; therefore, the equivalent *dc* voltage V_{EQ} can absorb their effects.

An alternative switched structure circuit appropriate for simulation purposes is shown in Figure 1e. This structure can be used for *dc*, *ac* and general transient simulation. To obtain the *dc* transfer characteristic of the FG device, we run a transient analysis. The initial condition on C_{FG} is V_{EQ}, the voltage on the FG for V_{CG}=0. After the switch has opened, the voltage on the control gate sweeps from 0 to VDD. Note that in this simulation C_{FG} should not include the intrinsic capacitances of the MOSFET, which are already provided by the simulator for transient analysis.

4. ASSOCIATION OF MODELS

By extracting a set of basic parameters with the procedure introduced in the previous section, we found the values for the normalization current I_S, the coupling coefficient α_{CG}, the equivalent voltage at the FG V_{EQ}, the equivalent threshold voltage V_T^{CG} and the equivalent subthreshold factor n_{CG}.

We incorporated α_{CG} and V_{EQ} into the macromodel shown in Figure 1d and by using the BSIM3v3 model parameters we ran a *dc* simulation to compare it against the experimental measurements. The results obtained for FGMOS devices are shown in Figure 6. The macromodel simulation results are in good agreement with the experimental results.

For analytical modeling of the FG device, we use equation (9) derived for MOS transistor together with the extracted I_S, V_T^{CG}, and n^{CG}.

$$\left(V_{CG} - V_T^{CG}\right) / \left(n^{CG}\phi_t\right) = \left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right) \tag{11}$$

The results from the analytical ACM model are also shown in Figure 6, where we can observe a close matching of the transfer characteristic plots for a first order approximation model.

Referring again to the switched structure shown in Figure 1e, we also included the results of the transient simulation results in Figure 6. The precision of this simulation relies on the accuracy of the FG to bulk or FG to the n-well capacitor values.

Note that as before, the simulation results are in good agreement with the experimental results.

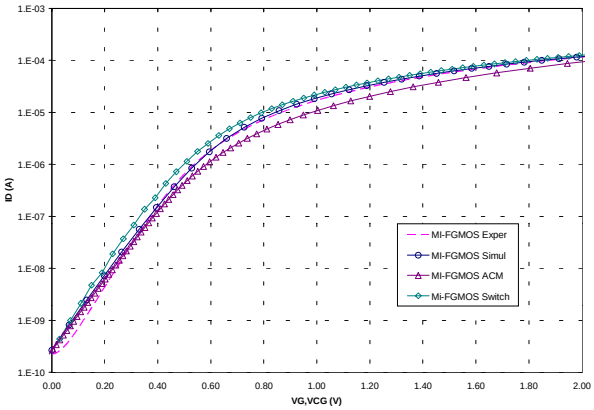

Figure 6. I_D vs. V_{CG} plots for experimental results, macromodel, analytical and transient simulations.

5. SUMMARY

We have proved that, starting from experimental results obtained from a HP-4145B parametric analyzer, we can obtain reliable parameters for simple hand calculations as well as for device simulation using the industry standard BSIM3v3 model.

We demonstrated a simple procedure to extract a meaningful set of parameters, and how these parameters are introduced into the ACM model as well as into a device macromodel for circuit simulation. By using the proposed approach we can design FGMOS VLSI systems being confident that the models will have a good degree of matching for analytical, simulation and experimental results.

The layout of the FG device was extended to include an additional well controlling input. A FG device macromodel [9] was modified to include the well controlling input and the equivalent voltage at the FG. An alternative switched structure was shown to overcome the difficulty of *dc* simulation.

6. REFERENCES

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