Scaling Rules Allow the Reuse of MOS Analog Design

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Abstract

This paper presents a reuse procedure of analog circuits which is based on a scalable model of the MOSFET. A set of very simple expressions allows the calculation of the transistor dimensions and bias of a given circuit in a new generation technology, based on a previous design of the same circuit in an earlier technology.

1. Introduction

In the present-days of omnipresent digital systems there is a growing need for analog designers. This apparent paradox is due to the fact that although analog circuits take up only a limited part of the modern integrated circuit, their design time and cost is very important. The multiplicity of performance specifications, the dependence of circuit behavior on technology variations, the diversity of element sizes and shapes make the analog design problem difficult. The natural difficulties of analog design are worsened by the lack of good device models implemented in circuit simulators and by the fact that modern electrical engineering curricula provide inadequate preparation for analog circuit design. Because there is usually substantial discrepancy between design formulation and simulation results (due to poor modeling), analog designers use very empirical and personal approaches and often "twiddle". In order to reduce design effort, analog standard cell libraries can be used. The problem is that such libraries, which require many man-years of design effort, very rapidly become obsolete due to technology evolution.

In this paper we use a physics-based MOSFET model [1] to develop a methodology for the technology migration of analog circuits. We derive simple formulas that allow us to calculate transistor dimensions and bias for a given circuit in a new generation technology, starting from the same circuit topology designed in an earlier technology. The reuse of designs has several advantages. It can extend the useful life of specific designs and reduce the design effort of a standard cell library in a new technology. Even in the case of a new project, the reuse of an old design can be a useful first step. This approach is particularly appropriate for student designs.

2. MOSFET Model

The model in [1] was developed considering the needs of analog designers. It uses only one basic parameter, the normalization current I_S, that contains the basic information on the device: geometry, technology and temperature.

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \quad (1)$$

In (1), (W/L) is the aspect ratio, μ is the mobility, C'_{ox} is the oxide capacitance per unit area. ϕ_t is the thermal voltage and n is the slope factor, which is slightly greater than one and almost bias-independent [1].

The bias of a saturated MOSFET is characterized by the normalized drain current $i_f = I_D/I_S$ or inversion level [1].

Table I. Basic equations of the new MOSFET model

$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_f}}$ (2)	$G_V = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D} V_E L$ (3)
$f_T = g_m \Big/ 2\pi(\frac{1}{2} C'_{ox} WL)$ (4a)	$f_T = \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f} - 1\right)$ (4b)

The transconductance-to-current ratio of a saturated transistor given by (2) is a universal relationship, which is independent of technology, dimensions and temperature. G_v, the absolute value of the attainable voltage gain of the common-source amplifier can be written as in (3), where V_E is the Early voltage per unit length [2]. Finally, the intrinsic cutoff frequency of a MOSFET in saturation is approximated in [1] by (4a) or, equivalently by (4b).

3. Analog Resizing Rules.

For the resizing rules that follow, we are going to preserve the specifications of dynamic range as well as the gain-bandwidth product (GB). Considering only thermal noise for a purely capacitive load C, the signal-to-noise ratio [2] is

$$SNR = V_{pp}^2 C / 8kT \quad (5)$$

where V_{pp} is the peak-to-peak signal swing, T the absolute temperature and k the Boltzmann constant.

In a single-stage amplifier, GB is proportional to the ratio of the transconductance to the load capacitance [2]

$$GB = g_m / 2\pi C \quad (6)$$

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Therefore, both capacitances and transconductances must be scaled up by K_V^2 for a voltage swing scaled down by K_V. Additionally, as long as the frequency spec (GB) of the amplifier is not changed in the new technology, we maintain the same transition frequency of the transistors as in the original design.

Constant-inversion level scaling

As shown in (2), g_m/I_D is a function of the inversion level i_f. Since n is almost technology-insensitive, scaling at constant inversion level keeps g_m/I_D constant. Since the scaling factor for g_m is K_V^2, the current must also be multiplied by K_V^2. Assuming mobility to be constant then, to keep the transition frequency constant, it follows from (4b) that the channel length must remain the same. The scaling factor for the channel width W is deduced from (1).

Channel length scaling: $L \rightarrow L/K_L$

Channel length scaling is a natural choice to take advantage of the smaller dimensions of a new generation technology. To keep the transition frequency constant, the scaling factor for W must be $K_V^2 K_{ox}^{-1} K_L$, as follows from (4a). Knowing the scaling factors for W and L, it follows from (1) that the normalization current I_S is scaled by $K_V^2 K_L^2$. The reduction in the inversion level associated with channel length scaling can be calculated from (4b).

Finally, the scaling factor for the current I_D is derived from the definition of inversion level $i_f = I_D/I_S$.

Table II. Resizing rules for MOS transistors considering generalized scaling factors

$V_{pp} \rightarrow K_V^{-1} V_{pp}$, $C'_{ox} \rightarrow K_{ox} C'_{ox}$, $L \rightarrow K_L^{-1} L$, $V_E \rightarrow K_E V_E$

Quantity	Constant-inversion level scaling	Channel length scaling	
L	1	K_L^{-1}	
W	$K_V^2 K_{ox}^{-1}$	$K_V^2 K_{ox}^{-1} K_L$	
		WI (*)	SI (**)
i_f	1	K_L^{-2}	K_L^{-4}
I_D	K_V^2	K_V^2	$K_V^2 K_L^{-2}$
G_V	K_E	$K_E K_L^{-1}$	$K_E K_L$

(*) Weak Inversion (WI) (**) Strong Inversion (SI)

4. Example

We first designed a common-source (CS) amplifier , p-channel driver and an ideal current source as the load, for a 1.2 μm technology and 5V power supply. Using both the constant-i_f and channel length scaling rules, we recalculated the dimensions and bias current of the amplifier for a .35μm technology and 2V supply. We have chosen 3 inversion levels for the primary design (Table III). Table IV shows the results of the constant-i_f scaling rules. In this case, the power consumption is increased by K_V and the specs are almost the same as in the primary design. The results in Table V show an improvement with respect to Table IV in regards to power consumption.

Table III. Simulated performance of the CS amplifier in a 1.2u technology

if	W (μm)	L (μm)	I_D (μA)	$\frac{g_m}{I_D}$	G_V (dB)	GB (MHz)	Noise (μV)
1	500	3.2	3.2	19.7	62.6	0.98	11.5
24	160	10	6.0	10.7	67.3	1.03	11.2
400	73	22	21.0	2.7	60.9	0.93	11.6

Table IV. Simulated performance of the CS amplifier in a 0.35u technology, designed using constant inversion level scaling Kv=2.5 Kox=3

if	W (μm)	L (μm)	I_D (μA)	$\frac{g_m}{I_D}$	G_V (dB)	GB (MHz)	Noise (μV)
1	1011	3.2	20.0	20.6	63.7	1.05	4.5
24	323	10	37.5	8.1	64.3	0.80	4.9
400	148	22	131	2.0	52.8	0.70	5.0

Table V. Simulated performance of the CS amplifier in a 0.35u technology, designed using channel length scaling (Kv=2.5 Kox=3 K_L=3.4)

if	W (μm)	L (μm)	I_D (μA)	$\frac{g_m}{I_D}$	G_V (dB)	GB (MHz)	Noise (μV)
0.1	3466	1.0	16.9	25.9	54.8	1.09	4.5
0.8	1109	2.8	14.6	22.1	63.3	0.86	4.9
5.8	506	6.3	22.6	14.5	65.9	0.87	4.8

5. Conclusions

A methodology for reusing analog MOS circuits has been developed. It is supported by a current-based MOSFET model, which has accurate single-piece equations and uses normalized variables and few physical parameters. Simple formulas allow the calculation of transistor dimensions and bias for a given circuit in a current technology, based on the circuit designed in a previous technology.

6. References

[1] A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "An MOS transistor model for analog circuit design", *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510-1519, October 1998.

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