A/D and D/A Converters

Audio, Video
Power Source
Thermocouple
Strain Gage
Bridge
Photodiode

Communication Channels
Wireless, cable, fiber
Disc, optical, and other storage media

Pre-Filtering → MUX → A/D Conversion → Data Acquisition

Post-Filtering → DEMUX → D/A Conversion → Data Distribution

DSP
Microprocessor
High-speed ADC applications
Performance of recently published ADCs: resolution versus speed.
ADC architectures trade-off

- Integrating ADC
- Sigma-Delta ADC
- SAR, Pipelined ADC
- Flash ADC

- Component Matching
- Integrating, Sigma-Delta ADC
- Flash, SAR, Pipelined ADC

- Complexity (Die Size)
- SAR, Pipelined, Sigma-Delta ADC
- Integrating ADC

EEL 410026 – Introdução ao Projeto de CI’s de Sinais Mistos CMOS  J. A. De Lima (EEL/UFSC)
Tradeoff between decision cycles and comparators

FLASH: \[ C = 2^n - 1 \quad t = 1 \]
PIPELINE: \[ C = P \times 2^{n/P} \quad t = P \]
SAR: \[ C = 1 \quad t = n \]

Number of Comparators vs Decision Cycles
Static transfer characteristic

A to D converters

ideal

real
A/D Converter (Nyquist Rate)

- Digital Output
- Analog Input
- Quantization Error
- Quantization interval (±1/2 LSB)

Midstep
Step width (1 LSB=Δ)
3.5 - 4.5

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A/D Nonlinearities

- DNL error is defined as the difference between an actual step width and the ideal value of 1LSB.
• to guarantee no missing codes + monotonic transfer function, DNL should be less than 1LSB (+/- 0.5LSB)
• Integral Non-Linearity is defined as the maximum deviation of the ADC transfer function from the ideal transfer.
Linearity characterization

• A to D converters

INL  Integral Non Linearity
DNL  Differential Non Linearity
(both are expressed in terms of LSB’s)
D to A converter showing a strong Integral Non-Linearity (INL).
Unequal heights of consecutive steps are measured by the Differential Non-Linearity (DNL). In the middle, severe DNL causes non-monotonicity.
Fast Fourier Transform (FFT)
- quantization noise

\[ \Delta = 2^{-N} / \text{(dyn range)} \]

**QUANTIZER concept**

- analog input
- coded output word

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input sine wave

3-bit oversampled sine wave

quantization noise

quantized sine wave
quantization noise
(magn multiplied by 200)
Power density spectrum of quantized sine waves

Fast Fourier Transform (FFT)

Sine wave

Number of samples: $2^{12}$

Quantization noise

Number of periods: 37

$\frac{f_s}{2}$

8 bit

10 bit

12 bit

14 bit

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Assumption:
quantization noise is uniformly distributed

Real SFDR measurement
Spurious Free Dynamic Range is the usable dynamic range of a A/D or D/A converter before spurious noise interferes or distorts the fundamental signal.

SFDR: ratio of the RMS value of the signal (carrier) at the input of the ADC or DAC to the RMS value of the next largest noise or harmonic distortion component (which is referred to as a “spurious” or a “spur”) at its output. SFDR is usually measured in dBc (i.e. with respect to the carrier frequency amplitude).

$\Rightarrow$ SFDR as an indicator of fidelity.

$$\text{SNR}_{\text{Ideal}} = 6.02 \ (N) + 1.76 \quad \text{(only quantization noise!!)}$$

(best-case: assumption that quantization noise is uniformly distributed)
generation of spurious second and third-order products
ENOB (Effective Number of Bits): A measure of overall accuracy under real-world conditions

ENOB Measures the Combined Effects of Multiple Sources of Noise and Distortion
Evaluation of ENOB

![Diagram showing evaluation of ENOB](image)

**THD < 0.001%@1KHz**
overall noise picked up by A/D
Error (Distortion) Sources in ADCs

DC:

i) **integral and differential nonlinearity errors**: irreducible distortion, as ADC output is not continuous, but quantized. Even perfect ADC exhibit some integral and differential nonlinearity.

ii) **noise**:
    a: quantization error - inherent to data conversion process
    b: generated within the converter itself.

iii) **channel-to-channel offset**: difference in the characteristics of analog input channels

AC:

i) **THD**: ratio of all harmonics generated to the original signal frequency.

ii) **channel crosstalk**: signal interference analog input channels.
ENOB Measurement of 16-bit ADC

ENOB of 13.6 and 14.1 bits
\[
\text{ENOB} = \frac{\text{SNR}_{\text{dB}} - 1.8}{6}
\]

because saturation is likely to occur when the signal gets large the SNR, which determines the ENOB, is evaluated by extrapolating the linear part of the plot until F.S.
$$\text{SNR}_{\text{ideal}} = 6.02 \ (N) + 1.76$$

(best-case: assumption that quantization noise is uniformly distributed)

where N is the number of bits of the converter. For N=10, SNR = 62dB.

**ENOB**

$$\text{ENOB} = \frac{\text{SNR}_{\text{dB}} - 1.8}{6}$$

*example: SNR = 53 dB, ENOB = 8.5*
Ex: The input signal has two channels: a strong one (0 dB) @ 6.72 MHz, and a small one (−90 dB) @ 3.8 MHz. The sampling frequency is 16.4 MHz. The big component generates a large third harmonic at 20.16 MHz which gets folded down to 3.76 MHz, just 40 kHz from the small channel. Even if the SFDR is 85 dB the spur almost completely masks the −90 dB signal.
FLASH ADC

• $2^N - 1$ comparators
• typically consume more power than other ADC architectures
• generally limited to 8-bits resolution
• relatively low resolution and expensive
• ideal for applications requiring very large bandwidth
• exceed giga-sample per second (Gsp) conversion rates
• each comparator represents 1 LSB
• output code can be determined in one compare cycle.
<table>
<thead>
<tr>
<th>Thermometer</th>
<th>Gray</th>
<th>Binary</th>
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</thead>
<tbody>
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<td>0 0 0 0 0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0</td>
<td>0 0 1</td>
<td>0 0 1</td>
</tr>
<tr>
<td>1 1 0 0 0 0 0</td>
<td>0 1 1</td>
<td>0 1 0</td>
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<tr>
<td>1 1 1 0 0 0 0</td>
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<td>1 0 0</td>
<td>1 1 1</td>
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<table>
<thead>
<tr>
<th>T</th>
<th>G</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>G3</td>
<td>B3</td>
</tr>
<tr>
<td>T2</td>
<td>G2</td>
<td>B2</td>
</tr>
<tr>
<td>T3</td>
<td>G1</td>
<td>B1</td>
</tr>
</tbody>
</table>
A 10-bit Flash ADC

- \( V_{DD} = 1.8 \text{ V} \)
- 10-bit \( \rightarrow \) 1023 comparators
- \( V_{FS} = 1 \text{ V} \) \( \rightarrow \) 1 LSB = 1 mV
- DNL < 0.5 LSB \( \rightarrow \) \( \sigma_{os} < 0.5 \text{ LSB} \)
- 0.5 mV \( \times 3.5 \sigma \) \( \rightarrow \) \( \sigma = 0.1 \text{ 0.2 mV} \)
- \( 2^{N-1} \) very large comparators
- Large area, large power consumption
- Very sensitive design
- Limited to resolutions of 4-8 bits
Offset vs. Resolution

- \( V_{FS} = 2\text{V} \)
- \( V_{FS} = 1\text{V} \)

- DNL < 0.5 LSB
- Large \( V_{FS} \) relaxes offset tolerance
- Small \( V_{FS} \) benefits conversion speed (settling, linearity of building blocks)
• Typical CMOS comparator

V_{os} derives from:
• Preamp input pair mismatch (V_{th}, W, L)
• PMOS loads and current mirror
• Latch mismatch
• CI / CF imbalance of M_9
• Clock routing
• Parasitics
Latch Regeneration

- exponential regeneration due to positive feedback of $M_7$ and $M_8$
(1) large differential input voltage
(2) small differential input voltage
(3) \( \cong \) zero differential input voltage

\[ \Delta V_{IN}: \text{the differential input voltage at the time of latching}, \]
\[ A = \text{the gain of the preamp at the time of latching}, \]
\[ \tau = \text{regeneration time constant of the latch}, \]
\[ t = \text{the time that has elapsed after the comparator output is latched} \]
The AM685 ECL Comparator (1972)
Interpolation A/D Converters

An interpolator generates an electrical value that is intermediate between two other electrical quantities by using, for voltage inputs: resistive or capacitive dividers and, for current inputs: schemes based on current mirrors.

\[
V_{\text{inter}} = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}.
\]

\[
V_{\text{inter}}(\phi_2) = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2}.
\]

\[
\frac{(W/L)_{1,i}}{(W/L)_1} = \alpha; \quad \text{and} \quad \frac{(W/L)_{2,i}}{(W/L)_2} = 1 - \alpha
\]

\[
I_{\text{inter}} = \alpha \cdot I_1 + (1 - \alpha) \cdot I_2.
\]
Traditional active 2x interpolation architecture.
a) Use of interpolation in flash converters. b) Outputs and interpolated responses.
4-bit interpolating flash A/D Converter

2^n latches
Integrating A/D Converter

- Single, dual and multi-slope ADCs can achieve high resolutions of 16-bits or more are relatively inexpensive and dissipate materially less power.

- input voltage (-VIN) is integrated for a fixed number of clock periods, $2^n$.

- It then "de-integrates" Vmax by changing to $+V_{REF}$ at input and counts the number of clock cycles $k$ until it crosses zero.

- since peak amplitudes of rising and falling ramps are equal $\Rightarrow$

$$V_{in} \frac{2^n T_{ck}}{\tau} = V_{ref} \frac{k \cdot T_{ck}}{\tau}$$

$$k = 2^n \frac{V_{in}}{V_{ref}}$$
Operation of the integrating converter for three different input voltages.
Successive-approximation A/D

- quick conversion time and moderate complexity
- binary-search algorithm

Timing (a) and flow diagram (b) of the successive approximation technique.
The method uses one clock period for the S&H and one clock period for the determination of every bit
⇒ \((n + 1)\) clock intervals for an \(n\)-bit conversion
Pipeline (sub-ranging, half-flash) A/D Converter

- it reduces the number of bits to be converted into smaller groups, which are then run through a lower resolution flash converter.
- 100Msps at 8 to 14-bit resolutions
- compared to a flash converter, this approach reduces the number of comparators and logic complexity
• each stage resolves a few bits quickly and transfers the residue to the following stage so that the residue can be resolved further in the subsequent stages

• on each stage a DAC converts the output of the coarse ADC back to analog and subtracts from the input. The residue is then amplified.

⇒ latency time increases with number of stages \( K \). Delay = (K+1) clock cycles
two-step algorithm: two clock periods, one for converting the MSBs and the other for the LSBs.
Charge-Redistribution Successive Approximation ADC
• Ex: 5-bit charge-redistribution A/D Converter

1. **Sample Mode**: in this first step, all capacitors are charged to $V_{in}$
2. **Hold Mode**: The comparator is activated by opening S2, and then all capacitors are switched to ground \( \Rightarrow V_x = -Vin \). S1 is switched, so that VREF is applied to the capacitor array, during next step (bit cycling)
3. **Bit cycling:** The largest capacitor (16C in the example) is switched to VREF ⇒ \( V_x = -V_{in} + \frac{V_{ref}}{2} \). If VX is negative, then \( V_{in} > \frac{V_{REF}}{2} \) and MSB capacitor (16C) remains connected to VREF, with \( b_1 \) considedr now =1. Otherwise, the MSC capacitor is reconnected to ground and \( b_1 \) is taken as 0. This process is repeated N times, with a smaller capacitor being switched each time, until the conversion is finished.
Flow graph for a successive approximation.
Exercise: Find intermediate node voltages at Vx during the operation of the 5-bit DAC below, when Vin = 1.23V and VREF = 5V. Assume a parasitic capacitance of 8C exists on the node at Vx.
Σ–Δ A/D Converters

- Applications:
  - High-resolution needed applications;
  - Audio, video, medical applications and so forth.
- Nyquist rate $f_N = 2B$
- Oversampling rate $M = \frac{f_s}{f_N} >> 1$

Noise energy spread over a wider frequency range

$$\text{SNR} = 6.02N + 1.76\text{dB}$$
Oversampling

Quantization error modeled as noise

\[ M = \frac{F_s}{f_{3\text{dB}}} : \text{Oversampling Ratio (OSR)} \]
Anti-aliasing Filter

Relaxed requirements with oversampling

Input Signal

Nyquist Sampling

Anti-aliasing Filter

Oversampling
• each factor-of-4 oversampling increases the SNR by 6dB, and each 6dB increase is equivalent to gaining one bit.
• A 1-bit ADC with 24x oversampling achieves a resolution of four bits
• to achieve 16-bit resolution, one must oversample by a factor of $4^{15}$, which is not realizable $\Rightarrow$ noise shaping technique
without noise shaping:

\[ SNR = 6.02N + 1.76 + 10 \log(\text{OSR}) \text{ dB} \]

4x OSR → 1bit resolution

<table>
<thead>
<tr>
<th>13 Bits @ 8 kHz</th>
<th>Voice</th>
<th>1 Bits @ 134 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 Bits @ 300 kHz</td>
<td>ISDN</td>
<td>1 Bits @ 5 THz</td>
</tr>
<tr>
<td>16 Bits @ 40 kHz</td>
<td>Digital HiFi</td>
<td>1 Bits @ 172 THz</td>
</tr>
</tbody>
</table>

1 bit improves ADC linearity but sampling frequency will be huge !!!
Noise Shaped Spectrum

The integrator serves as a highpass filter to the noise.
The result is noise shaping.

Filtering the Shaped Noise

Effect of the digital filter on the shaped noise.
Nyquist Sampler (1 bit)

Power Density

In-Band noise of Nyquist Samplers
In-Band noise Oversamplers
In-Band noise of Noise-Shaped Oversamplers

First order Sigma-Delta Modulator

Oversampler

$f_B$, Frequency, $F_S/2$

Spectrum of a First-Order Sigma-Delta Noise Shaper
with noise shaping (first-order loop):

$$SNR = 6.02N + 1.76 - 5.17 + 9.03\log_2(OSR) \quad dB$$

$$SNR = 6.02N + 1.76 - 5.17 + 30\log_{10}(OSR) \quad dB$$

2x OSR → 1.5bit resolution

13 Bits @ 8 kHz → Voice → 1 Bits @ 233 kHz

13 Bits @ 300 kHz → ISDN → 1 Bits @ 8.36 MHz

16 Bits @ 40 kHz → Digital HiFi → 1 Bits @ 2.56MHz
summary:

Why $\Sigma \Delta$?

- Quantization Noise reduction in baseband.
- High-resolution.
- Anti-aliasing filter relaxing.
- Analog blocks flexibility.
Delta modulation and demodulation

(a) Modulation

Predictor of $x(t)$

(b) Demodulation
• Delta modulation is based on quantizing the signal amplitude change from sample to sample rather its absolute value (rate of change)

• since the integrator output tries to predict the input $x(t)$, the integrator works as a predictor.

• prediction-error term $x(t) - \bar{x}(t)$ is quantized and used to make the next prediction.

• prediction error (delta modulation output) is integrated in the receiver just as it is in the feedback loop $\Rightarrow$ receiver predicts the input signals
\[ \Sigma - \Delta \text{ modulation} \]
**Block Diagram of Sigma-Delta Modulation**

- Analog Signal enters through an integrator, followed by a 1-bit quantizer.
- The signal is then transmitted through a channel to a lowpass filter.
- In the demodulation section, the output of the lowpass filter is integrated, adding noise (N(s)) to form Y(s).
- Y(s) is then passed through another lowpass filter to produce X(s).

Note: Only one integrator.
The bitstream is a one-bit serial signal with a very high bit rate. Its major property is that its average level represents the average input signal level.
• the term Sigma-Delta comes from putting the integrator (sigma) in front of the delta modulator. Σ–Δ modulator produces a bitstream, whose average level represents the input signal level.

• input to the integrator is the difference between the input signal \( x(t) \) and the quantized output value \( y(n) \), converted back to the predicted analog signal, \( \bar{x}(t) \).

• difference \( x(t) - x(t) \) at the integrator input is equal to the quantization error.

• error is summed up in the integrator and then quantized by the 1-bit ADC.
Input and Output of a First-Order Sigma-Delta Modulator
• in each clock cycle, output of the modulator is either plus or minus full scale, according to the results of the 1-bit A/D conversion

• when the sinusoidal $x(t)$ is close to a plus full scale, the output is positive during most clock cycles. Conversely, when $x(t)$ is close to minus full scale, output is mostly negative. In both cases, the local average of the modulator output tracks the analog input.

• When $x(t)$ is near zero, the modulator output varies rapidly between a plus and a minus full scale with approximately zero mean.
• if the analog input is 0V (ac), the integrator will have no tendency to ramp either positive or negative, except in response to the feedback voltage

⇒ FF output will continually oscillate between "high" and "low," as the feedback system goes back and forth, trying to maintain the integrator output at 0V.
• averaging 4 samples gives 2 bits of resolution  
• averaging 8 samples gives 3 bits of resolution
First-Order Sigma-Delta ADC
Signals within a First Order Analogue Modulator

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• loop integrates the error between the sampled signal and the input signal
• signal is low-passed and noise is high-passed
⇒ the signal is left unchanged as long as its bandwidth doesn’t exceed the filter’s cutoff frequency, but the Σ–Δ loop pushes the noise into higher frequencies

Signal Transfer Function: (when $N(s) = 0$)
$$Y(s) = \left[ X(s) - Y(s) \right] \frac{1}{s}$$

Noise Transfer Function: (when $X(s) = 0$)
$$Y(s) = -Y(s) \frac{1}{s} + N(s)$$

$$\frac{Y(s)}{X(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{1}{s + 1} : \text{lowpass filter}$$

$$\frac{Y(s)}{N(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{s}{s + 1} : \text{highpass filter}$$
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First order \(\Sigma\Delta\) loop

Block Diagram of First-Order Sigma-Delta A/D converter

Digital Decimation Process
\[ SNR = \frac{3\pi}{2} A_x^2 (2L+1)(2B-1)^2 \left( \frac{OVR}{\pi} \right)^{2L+1} \]

- \( L \): loop order
- \( B \): no. of bits in discriminator
- \( A_x = 2^B - 1 \)

Note: Higher order Noise Shaper has less baseband noise

Multi-Order Sigma-Delta Noise Shapers
First-order $\Delta\Sigma$ modulator block diagram.

Second-order $\Delta\Sigma$ modulator block diagram.

Third-order $\Delta\Sigma$ modulator block diagram.

Fourth-order $\Delta\Sigma$ modulator block diagram.
(a) First order sigma-delta
(b) Second order sigma-delta
(c) Third order sigma-delta

NOTE: Frequency band of interest (in-band): 0 - 5 kHz
Rest of frequency band will be removed by digital decimation filters

Spectra of Three Sigma-Delta Noise Shapers
Spectrum of 2nd-order modulator

Ref: Schreirer and Temes
Ref: Kester, M. - Analog Devices, MT - 022 Tutorial
OL (overload level) : defined as the maximum input signal amplitude for which A/D still operates correctly
PSD of a 2nd-Order Sigma-Delta Modulator (detail)

SNR1 = 81.2 dB @ OSR=128
Rbit1 = 13.19 bits @ OSR=128
Second-Order and Third-Order Sigma-Delta Noise Shapers
• 2\textsuperscript{nd}-order $\Sigma\Delta$ modulator

• Continuous-Time (CT) Integrators
• 2\textsuperscript{nd}-order \(\Sigma–\Delta\) modulator

• Discrete-Time (CT) Integrators
Differential 2nd order △△ modulator
High-level view of delta-sigma modulator
Decimation

- decimation is used in a Σ–Δ ADC to
  
i) downsampling (eliminate redundant data at the output); re-sample the signal at Nyquist rate.
  
ii) attenuate noise above baseband

- Nyquist theorem: sample rate only needs to be 2x the input-signal bandwidth to reliably reconstruct the original signal

- However, the input signal was grossly oversampled to reduce the quantization noise

⇒ there is redundant data that can be eliminated without introducing distortion to the conversion result.
Essentially, decimation is both an averaging filter function and a rate reduction function performed simultaneously.

Decimation reduces the original sampling rate to a lower rate, the opposite of interpolation.

⇒ output sampling rate by ignoring all but every Mth sample
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BLOCK DIAGRAM AND SPECTRAL REPRESENTATION OF THE DECIMATION PROCESS
• decimation comb filter

• programmable decimation ratio

• the digital filter is generally designed so that zeros occur at the mains frequencies of 50 Hz/60 Hz.
Frequency response of a sinc filter with $N = 32$. 
• $\Sigma\Delta$ - ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter.

“If the number of "1"s in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input”

• This method of averaging only works for dc or very slowly changing input signals.

• $2^N$ clock cycles must be counted in order to achieve $N$-bit effective resolution, thereby severely limiting the effective sampling rate.
Sinc filter realized with a counter.
\( \Sigma \Delta \) A/D stream accumulated and decimated to represent an n-bit value of the input.
Sample Rate Reduction == >> More Resolution

16 : 1 decimation
average

\[ \frac{7}{16} = 0.4375 = 0111 \]

1 multi-bit output

speed is exchanged for resolution

Simple Example of Decimation Process
Sinc³ digital decimation filter
// declaration
// Decimation filter with Sinc filter followed by
// Differentiator and Decimation
//
module decimation(
    DSH clk i,  // DSH-rate clock (bit clock)
    WordClk i,  // Output Word-rate clock
    Reset i,  // Active-hi reset
    DSM i,  // Input from Modulator
    DWord ro);  // 16-bit Output Word

input DSH clk i;  // DSH-rate clock (bit clock)
input WordClk i;  // Output Word-rate clock
input Reset i;  // Active-hi reset
input DSM i;  // Input from Modulator
output [15:0] DWord ro;  // 16-bit Output Word

// Internal Wires
//
// I's-comp version of DWord
//
wire [15:0] DWord_icomp_w;

// Sinc Filter
assign DWord 2comp w = (DSH i==1'b0) ? 24'd0 : 24'd1;

// Accumulator (integrator)

always @ (posedge DSM clk i or posedge Reset i)
if (Reset i) begin
    // initialize acc registers on Reset_i
    Ac0l r <= 24'd0;
    Ac02 r <= 24'd0;
    Ac03 r <= 24'd0;
end
else begin
    // perform accumulation process
    Ac0l r <= Ac0l r + DWord 2comp w;
    Ac02 r <= Ac02 r + Ac0l r;
    Ac03 r <= Ac03 r + Ac02 r;
end

// Differentiator and Decimation
//
always @ (posedge WordClk i or posedge Reset i)
if (Reset i) begin
    Ac1 r <= 24'd0;
    Diff1 q r <= 24'd0;
    Diff2 q r <= 24'd0;
    Diff3 r <= 24'd0;
end
else begin
    Diff1 r <= Diff1 r - Diff2 q r;
    Diff2 r <= Diff1 r - Diff3 r;
    Diff3 r <= Diff2 r;
    DWord ro <= Diff3 r[13:0];
end
endmodule
Output spectra with ideal and finite gain ($A_0 = 100$) op-amp.
• Both output transistors operate in push-pull mode

• bitstream is amplified to the high level of the power supply and is available at the output with low impedance