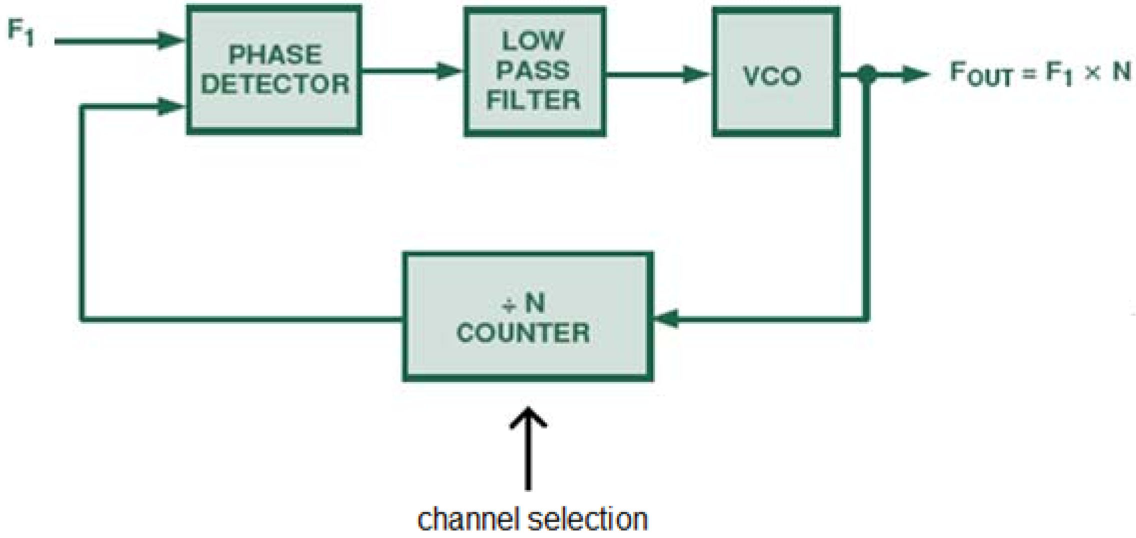
PRESCALERS

Frequency Synthesizers

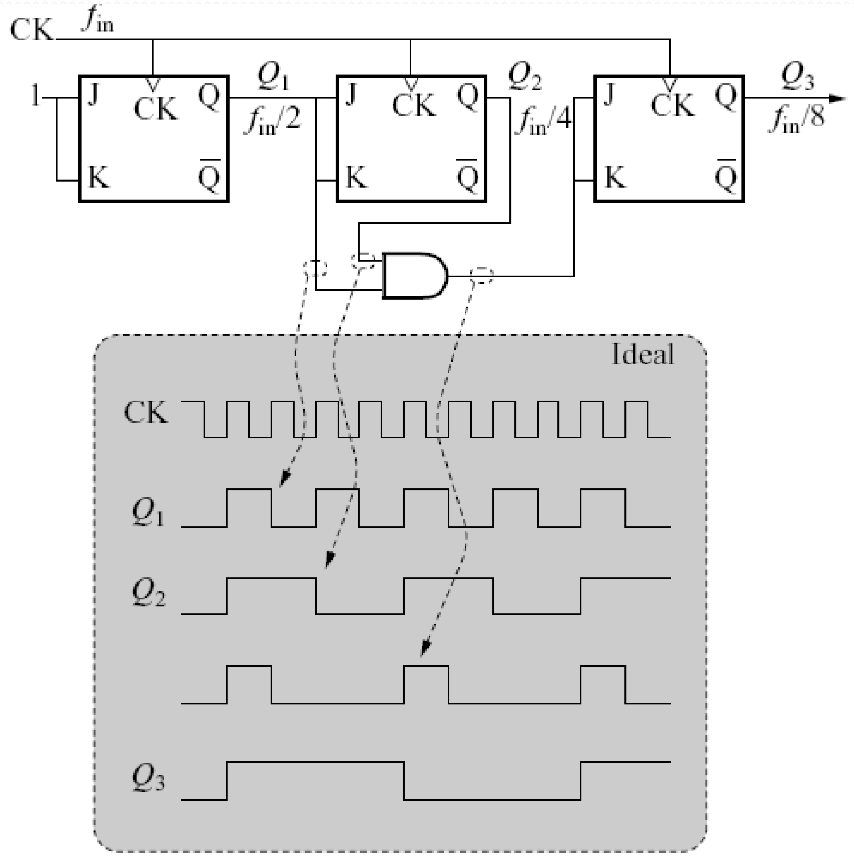


Using a reference counter in a PLL synthesizer

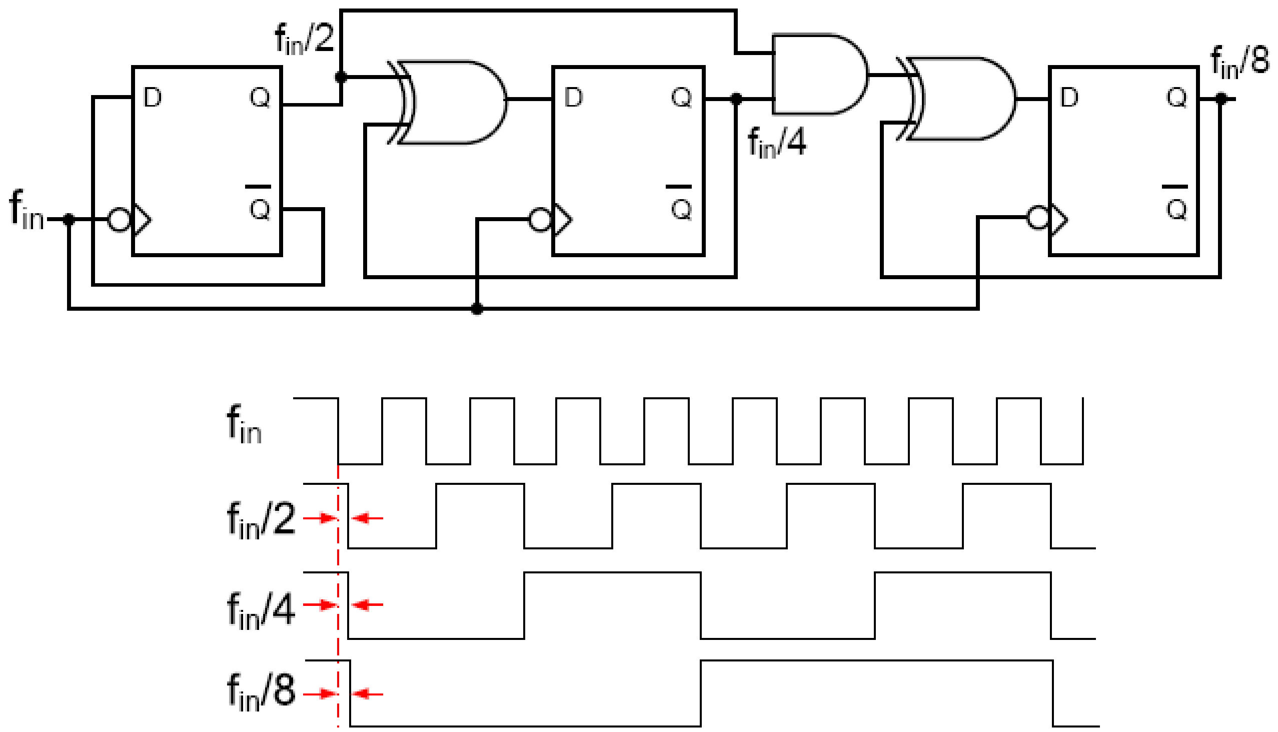
resolution: F_1

Synchronous vs. asynchronous counters (high-frequency)

Synchronous counters
- consume large power
- represent large CLOAD to oscillator
- race problems

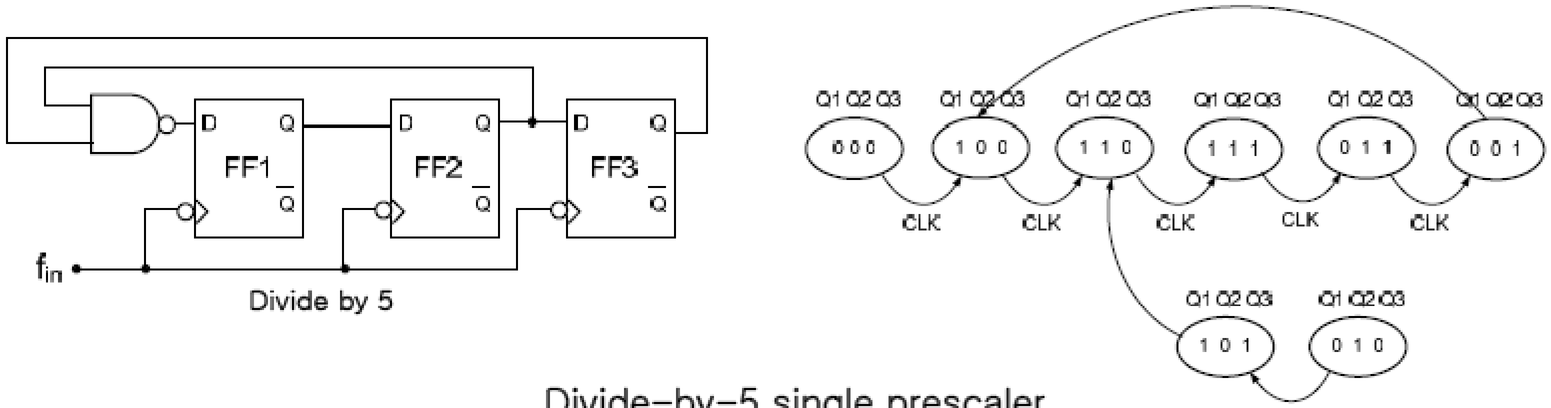


Ex: if Q2 is slower to go to 0 than Q1 to go to 1, the output of the AND gate experiences glitches.

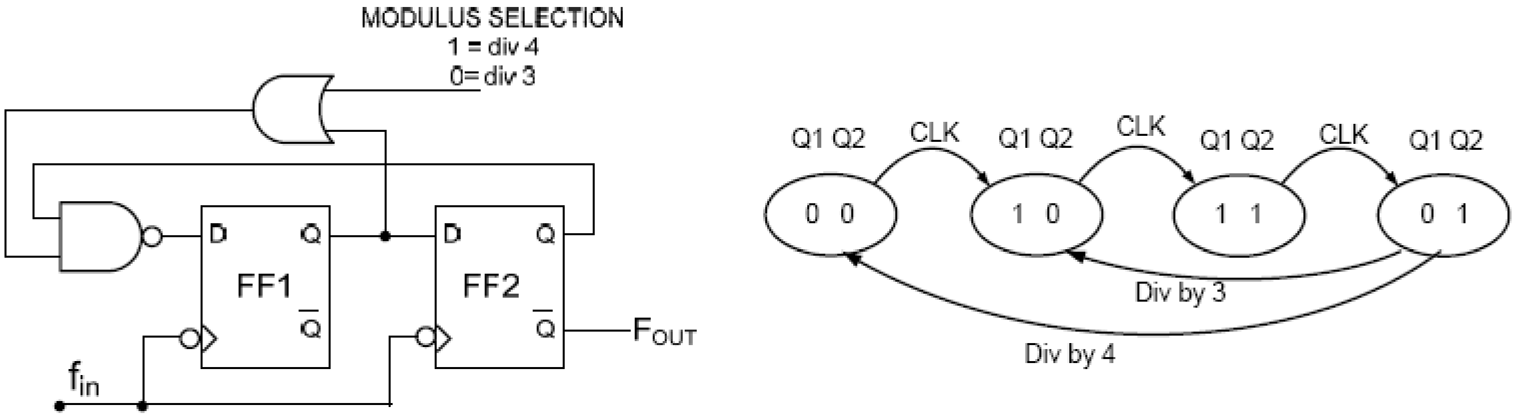


Synchronous counter

• delay almost constant between the input clock and the output at the divided frequency (NOT proportional to no. of flip-flops)

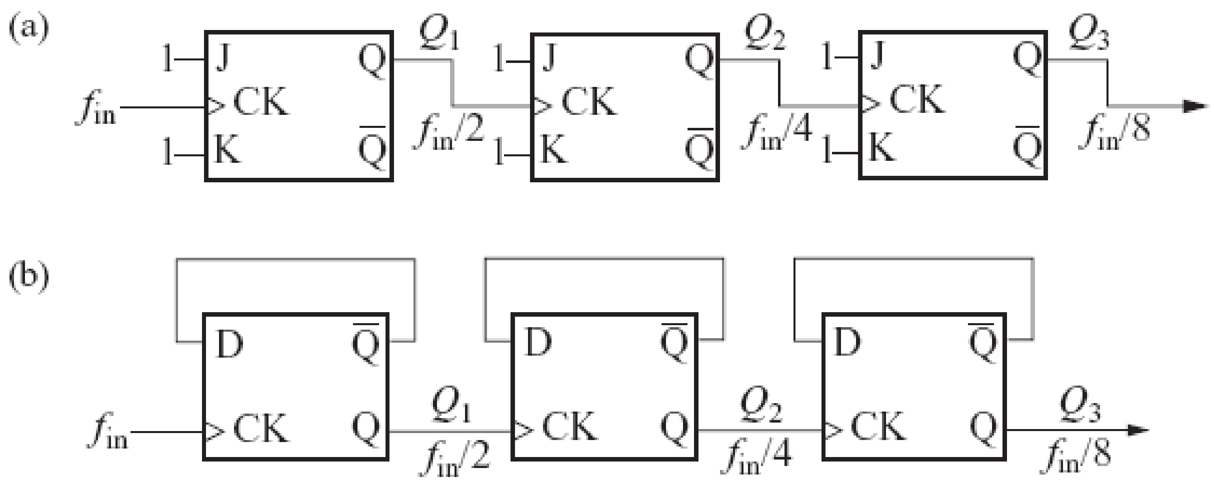


Divide–by–5 single prescaler



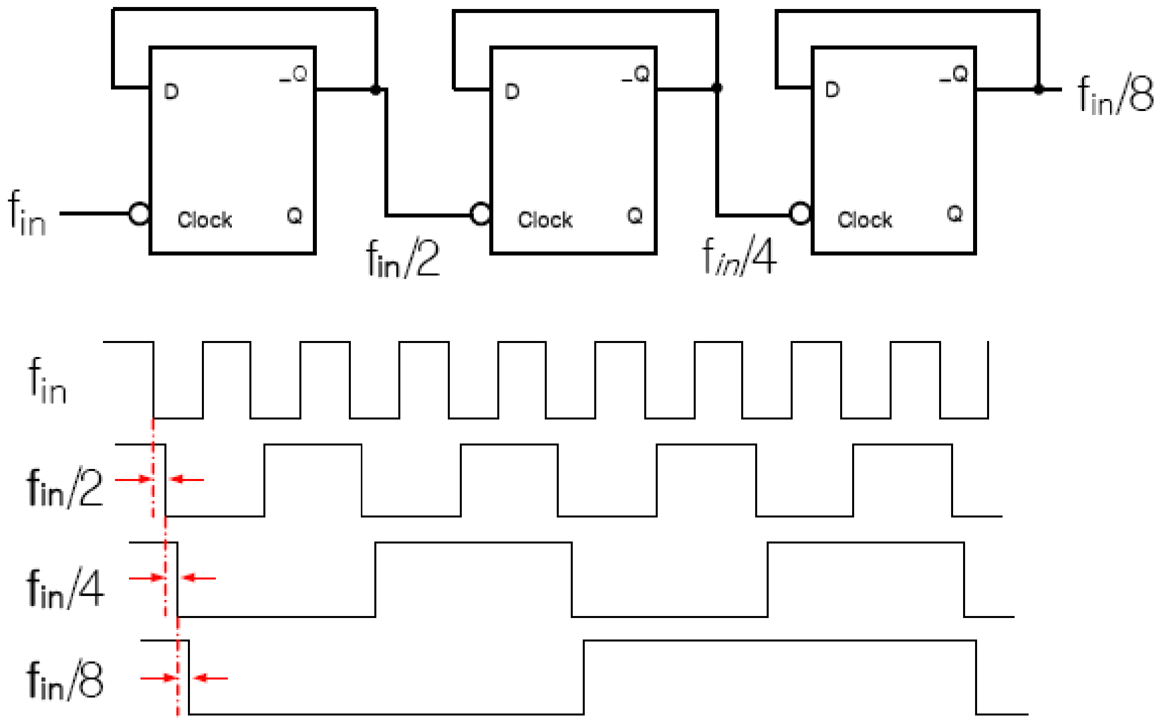
Dual 3/4 prescaler and state diagram

asynchronous counters ⇒ preferred option for high-frequency



Asynchronous counters: (a) cascade of toggle flip-flops and (b) cascade of modulo-2 Johnson counters

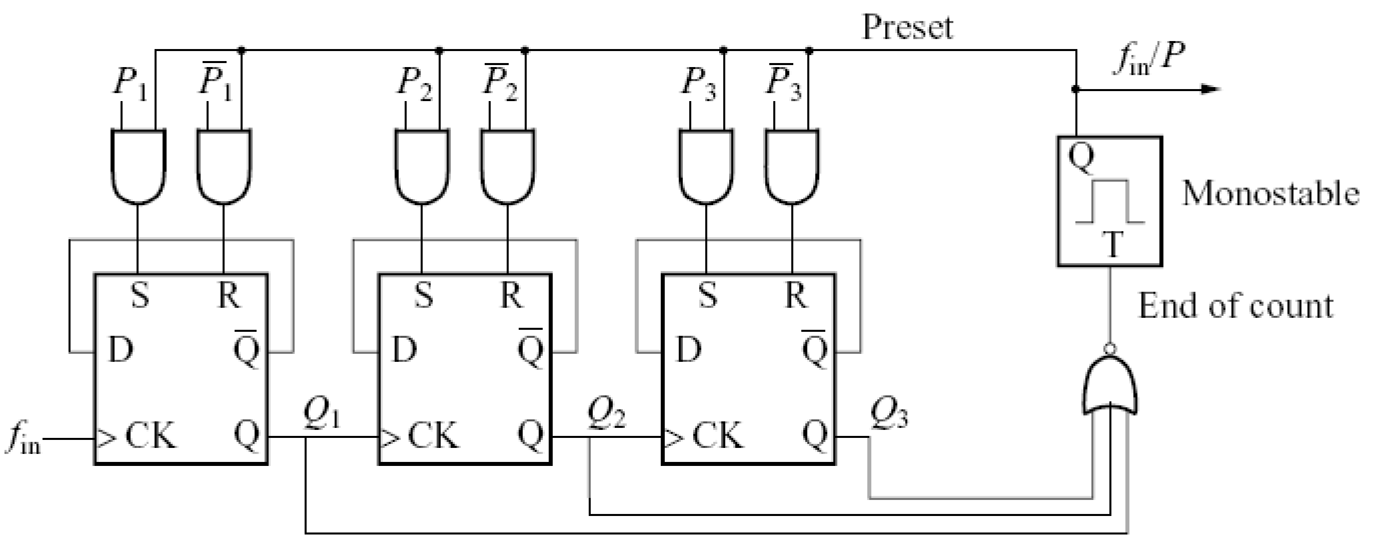
- forward/backward counting
- power consumption is reduced, as each stage operates at half frequency of previous stage



Asynchronous ripple counter

• delay is however added between the input clock and the output at the divided frequency (**proportional** to no. of flip-flops)

Programmable dividers



Presettable modulo-P asynchronous counter (modulus-8 with backwards counting from Q3Q2Q1 =111 to 000)

Basic principle: to preset counter to a initial state P and detect final state F by means of an 'end-of-count' EOC logic ⇒ the counter counts down between P and F

- limitation is max fin as correct operation is guaranteed if EOC signal presets the counter before the next clock edge arrives

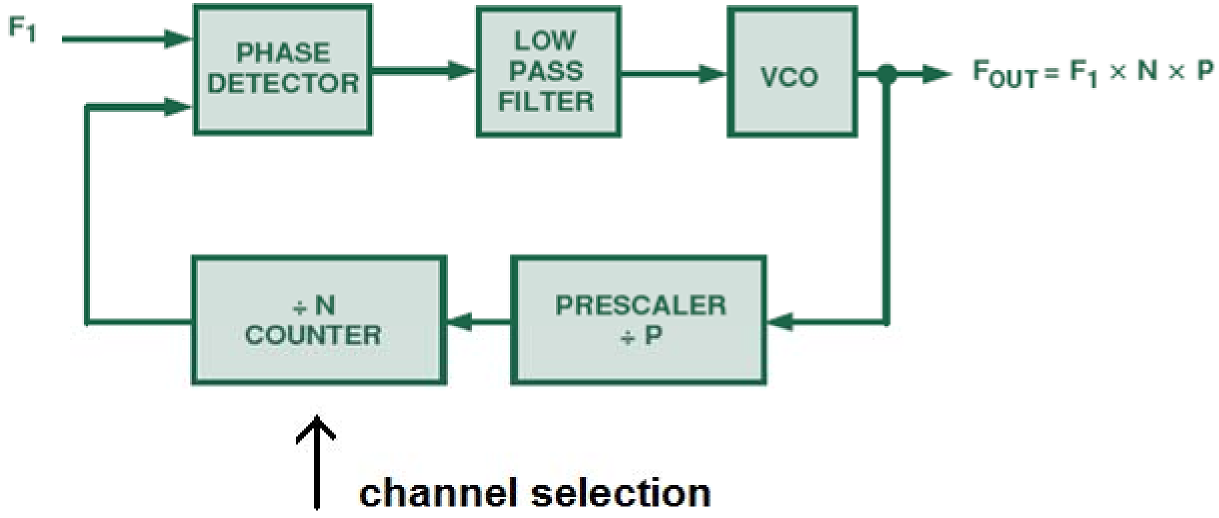
i) High-frequency operation is attained when logic function is kept simple

i) simplest dividers divide by fixed numbers

⇒ programmable divider could have a fixed-modulus high-speed divider as first stage

• If a pre-settable modulus-P divider follows a modulus-N prescaler, overall frequency division ratio is NxP.

• the input frequency has to be lowered exactly by P to keep same resolution
⇒ implies narrowing the PLL loop bandwidth, which may be undesirable!



Basic prescaler

resolution degraded: P x F_1

Pulse Swallowing Technique

• If *S input pulses are swallowed* the output period becomes longer by S reference periods

$\Rightarrow$ overall frequency division-ratio is $M = (NP + S)$, *which can be varied in unity steps* by changing S

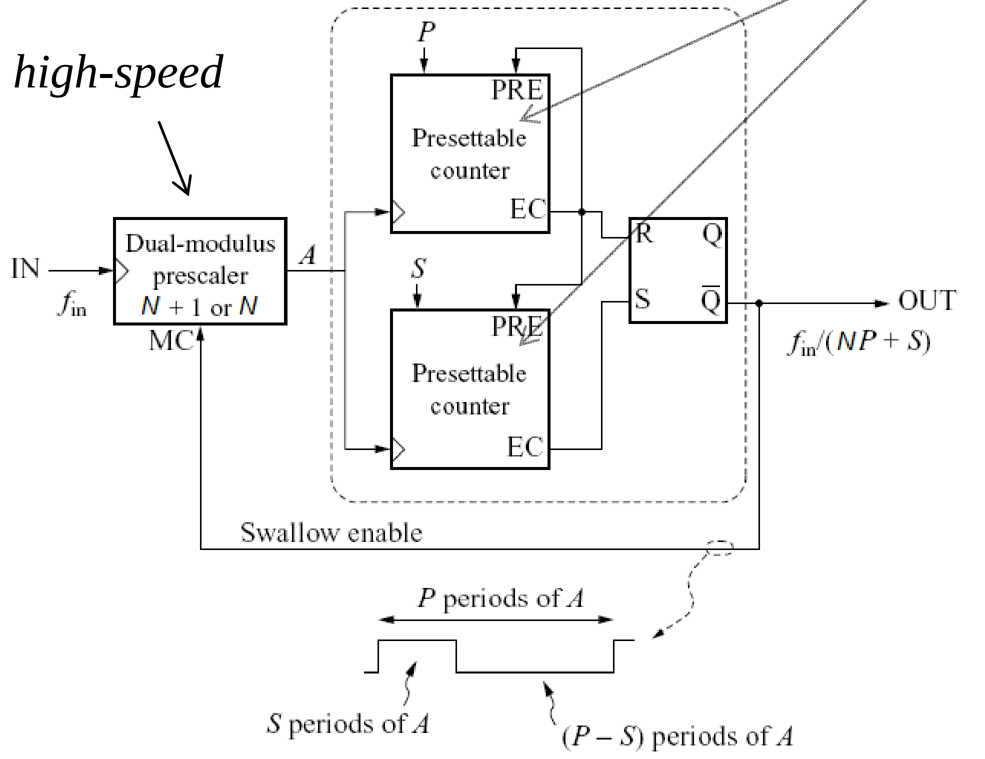
$M_1 = (NP + S)$

$M_2 = (NP + S + 1)$

$\Rightarrow \Delta M = M_2 - M_1 = 1$ *(same resolution without prescaling!)*

asynchronous counter

high-speed



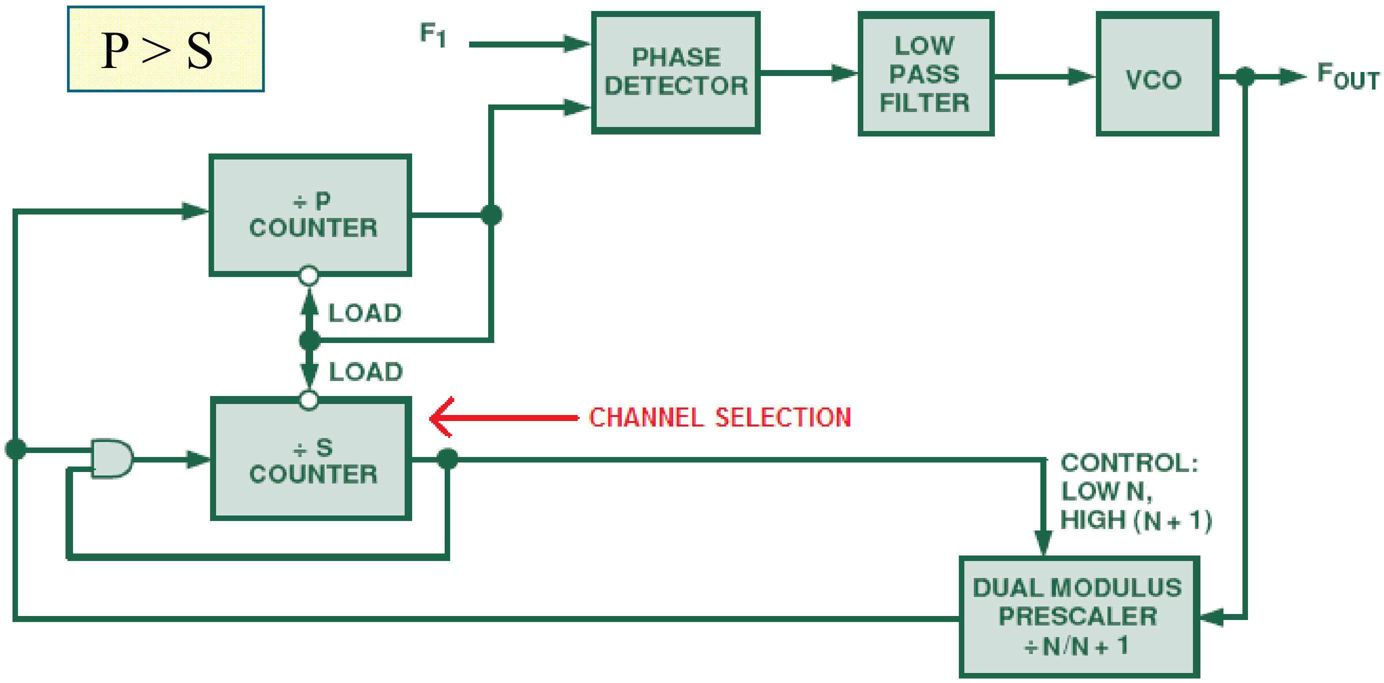
A= (N+1) **A= N**

Programmable divider based on pulse swallowing.

- at beginning of counting, N+1 factor is selected in dual-modulus prescaler (OUT = 1)
- P and S count in parallel, with P > S
- when S overflows, set = 1 and OUT → 0
- N factor is selected in dual-modulus prescaler
- it remains like that until P overflows and OUT → 1
- cycle is restarted.

total counts of Fout is a full F1 cycle:

S x (N+1) + (P-S)N
SN + S + PN – SN
PN + S = M



frequency synthesizer with pulse swallowing technique

total counts of Fout is a full F1 cycle:

S x (N+1) + (P-S)N

SN + S + PN – SN

PN + S = M

Ex 1 (using pulsing swallowing):

• frequency synthesizer in 2400–2480 MHz ISM band

• 1 MHz channel spacing ⇒ division factor ($M = NP + S$) between 2400–2480

Design steps:

i) choice of the modulus *N (dual-modulus prescaler), P (program counter)* and *S (swallow counter), with P > S*

ii) assume that <u>only S can vary</u> to simplify channel-select logic.

iii) make either N or N + 1 *a power of* two

iv) choose S as low as possible so that P > S is a minimum

Assuming initially S varies between 1 and 81 (to cover 81 possible division ratios) then P > 81:

$$N < \frac{M - S}{P} = \frac{2399}{81} = 29.6$$

Choosing N = 16 $\Rightarrow$ $P = \frac{M - S}{N} = \frac{2399}{16} = 149$ and $P > S$

Design values for pulse swallower

N	P	S	M	$P > S$
16	149	16	2400	TRUE
16	149	96	2480	TRUE
32	75	0	2400	TRUE
32	75	80	2480	FALSE
32	76	48	2480	TRUE
22	109	2	2400	TRUE
22	109	82	2480	TRUE
9	256	96	2400	TRUE
9	256	176	2480	TRUE

$M = (P \times N) + S$

$M_{MIN} = (Pmin \times N) + Smin$
$= ((N + 1) \times N) + 1$
$= N^2 + N + 1$

$M_{MAX} = (Pmax \times N) + Smax$
Pmax and *Smax* are determined by the size of P and S counters.

M_{MIN}-M_{MAX}: range over which it is possible to change N in discrete integer steps.

Ex2: assume that prescaler is programmed to N/N+1 = 32/33

S counter: 6 bits means S can be $2^6 - 1 = 63$

P counter: 13 bits means P can be $2^{13} - 1 = 8191$

$M_{MIN} = N^2 + N + 1 = 1057$

$M_{MAX} = (Pmax \times N) + Smax$

$= (8191 \times 32) + 63 = 262175$

If F_1 = 10KHz and P = 6000; S =40

F_{OUT_MIN} = 1.057GHz

F_{OUT_MAX} = 2.62GHz

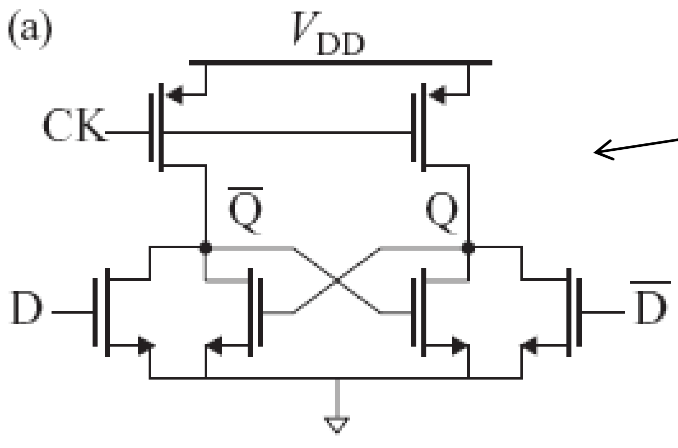
$F_{OUT} = F_1 (PN + S)$ = 10KHz (6000x32+40)=1.92040GHz

$F_{OUT1} = F_1 (PN + S+1)$= 10KHz (6000x32+41)=1.92041GHz

ΔF_{OUT} = 10KHz

(Differential) CMOS Current Mode Logic - (D)CML

• The main building block of the before-described counters is the D-type level-triggered latch

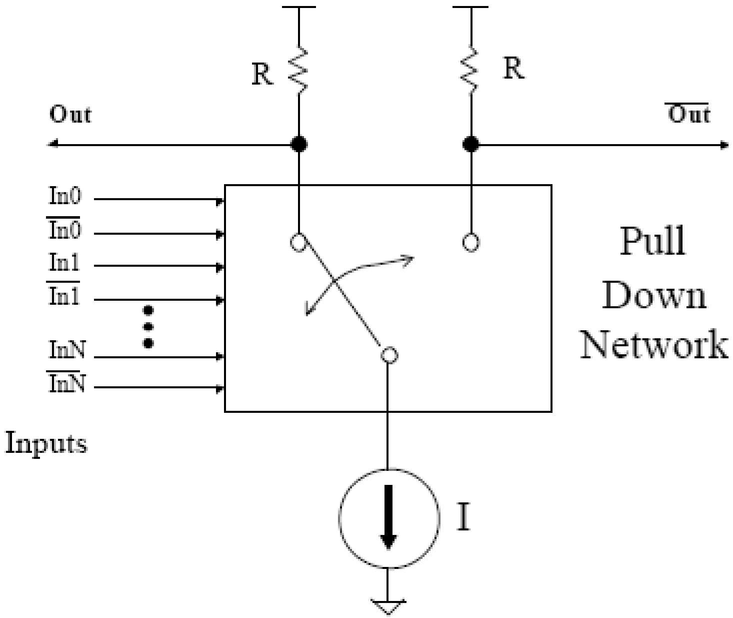


D-type latch: (a) static CMOS

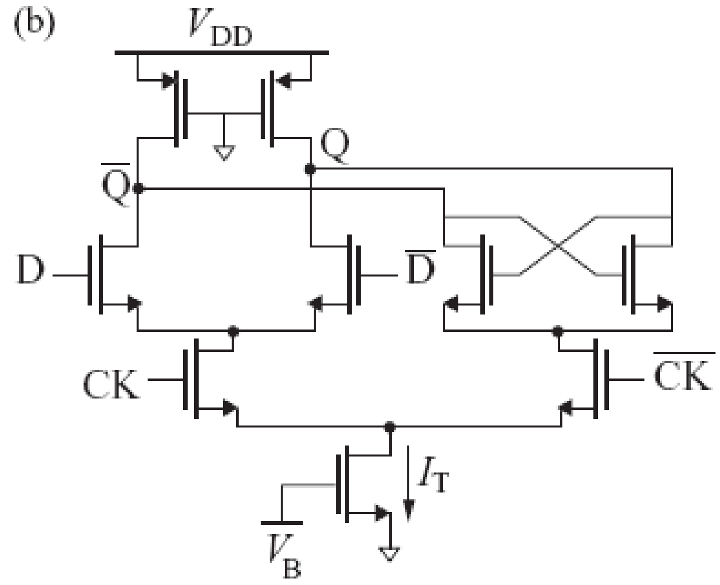
Conventional CMOS

• CK swing has to be wide enough ($V_{TH} + V_{GO}$) to turn on pMOS. Since CK has a finite slope, this implies a certain delay before the latch is able to sense at CK transition

⇒ Differential CML for high-speed processing



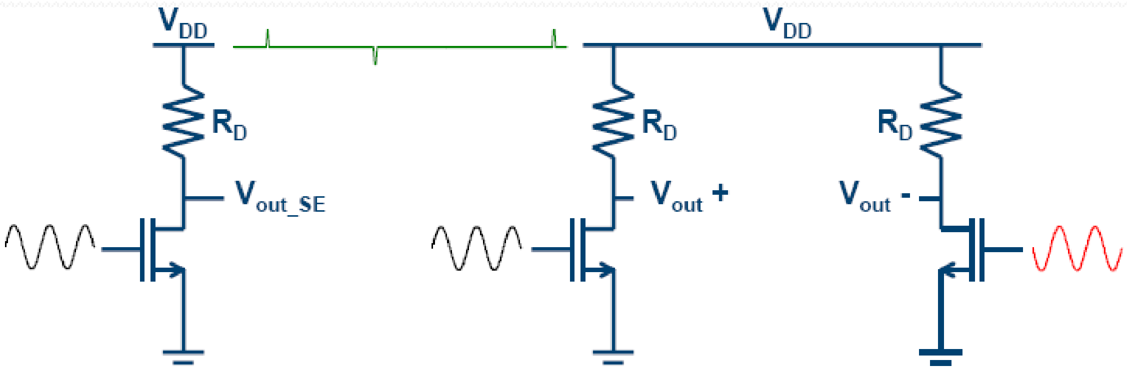
Basic CML gate

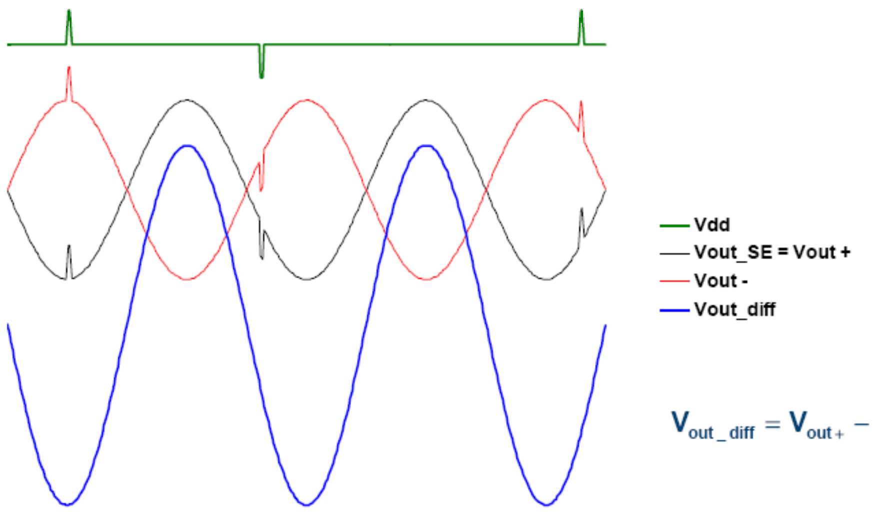


D-type latch: (b) static CML

- CML is based on the use of differential stages
- tail current is switched between two branches by CK
- a regenerative pair holds the data when CK is low
- loads can be triode-operating or diode-connected PMOS.

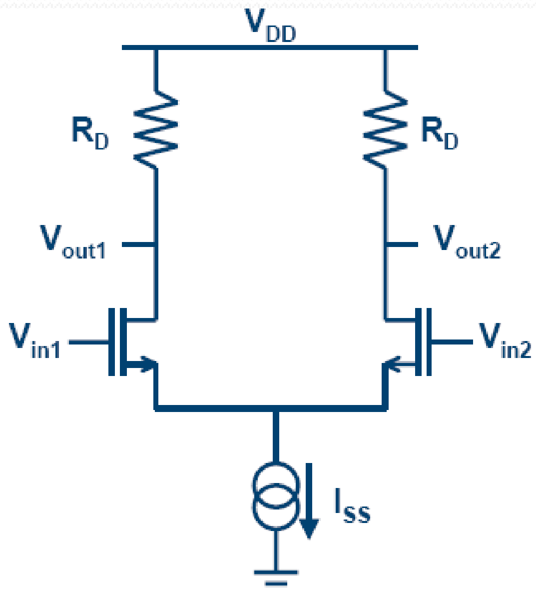
Single-Ended vs Differential

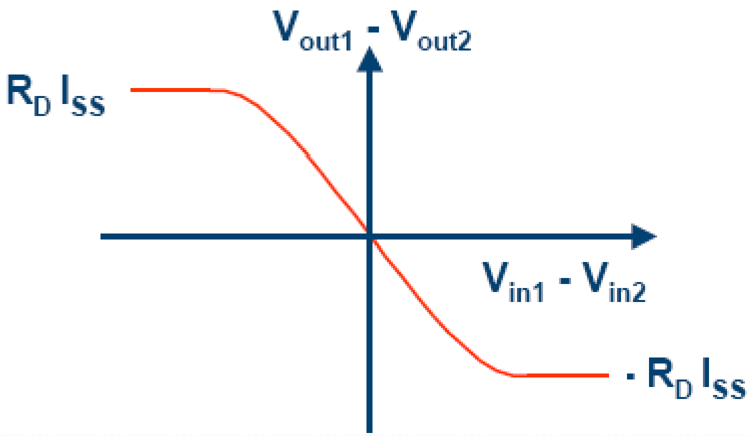


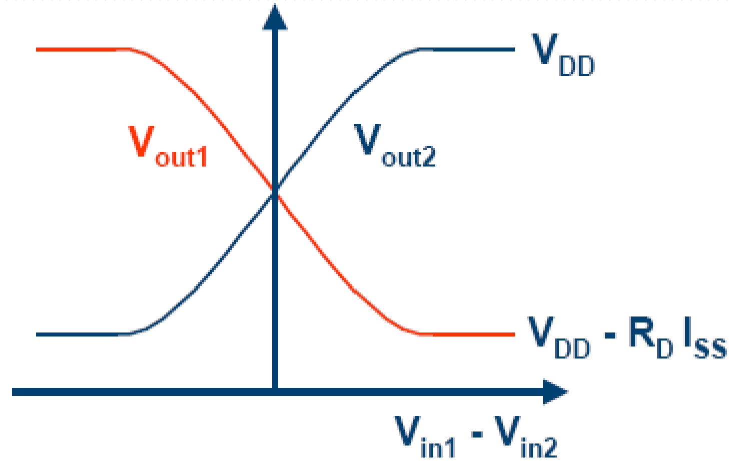


$$V_{out\_diff} = V_{out+} - V_{out-}$$

Common-Mode disturbances disappear in the differential output







- small ΔV_{in} already develops full V_{OUT}

CML x CMOS

Pros:

i) reduced voltage swing (V_{GO} against $V_{GO} + V_{TH}$ of CMOS stages) ⇒ less delay before input sensing ⇒ higher speed

ii) current-steering operation: current drained from supply less variable

iii) differential circuits are immune to coupled disturbances; they reject disturbances coming from substrate and power supply due to other blocks

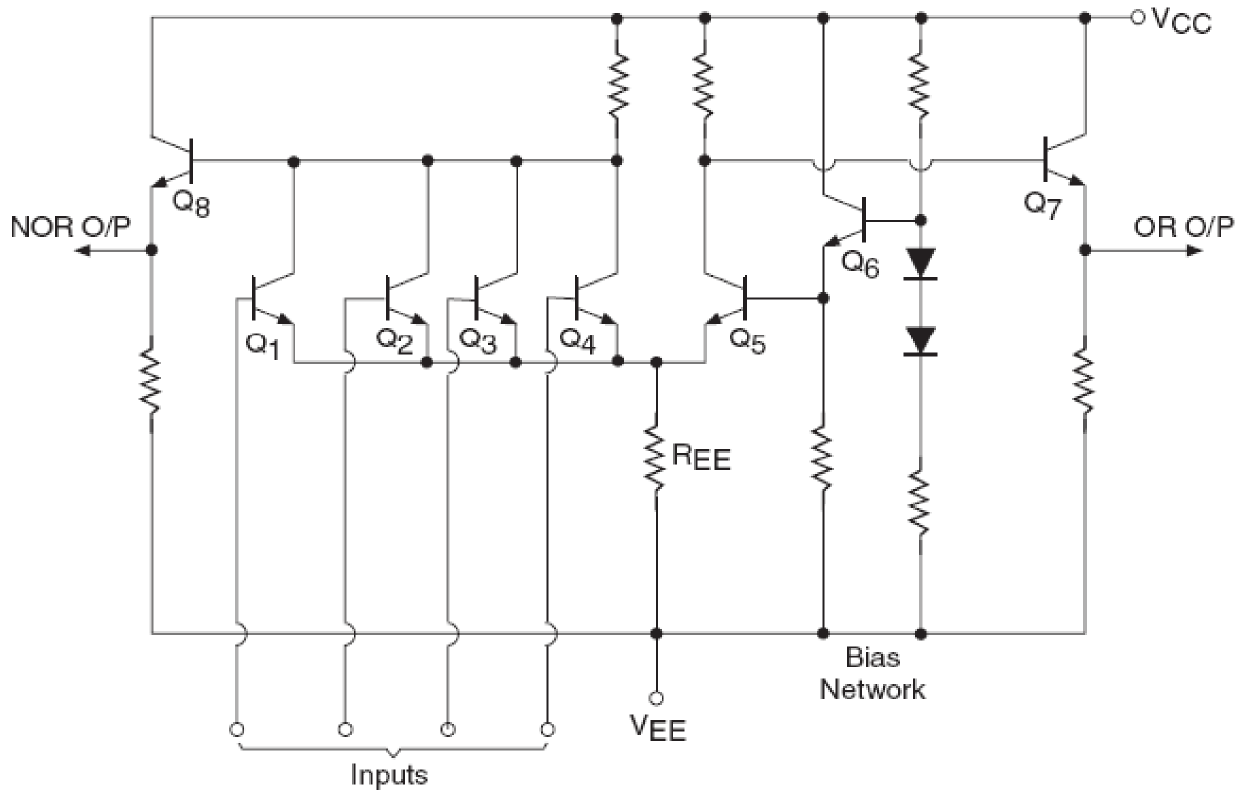
Cons:

i) larger area

ii) 2 “wires” per signal

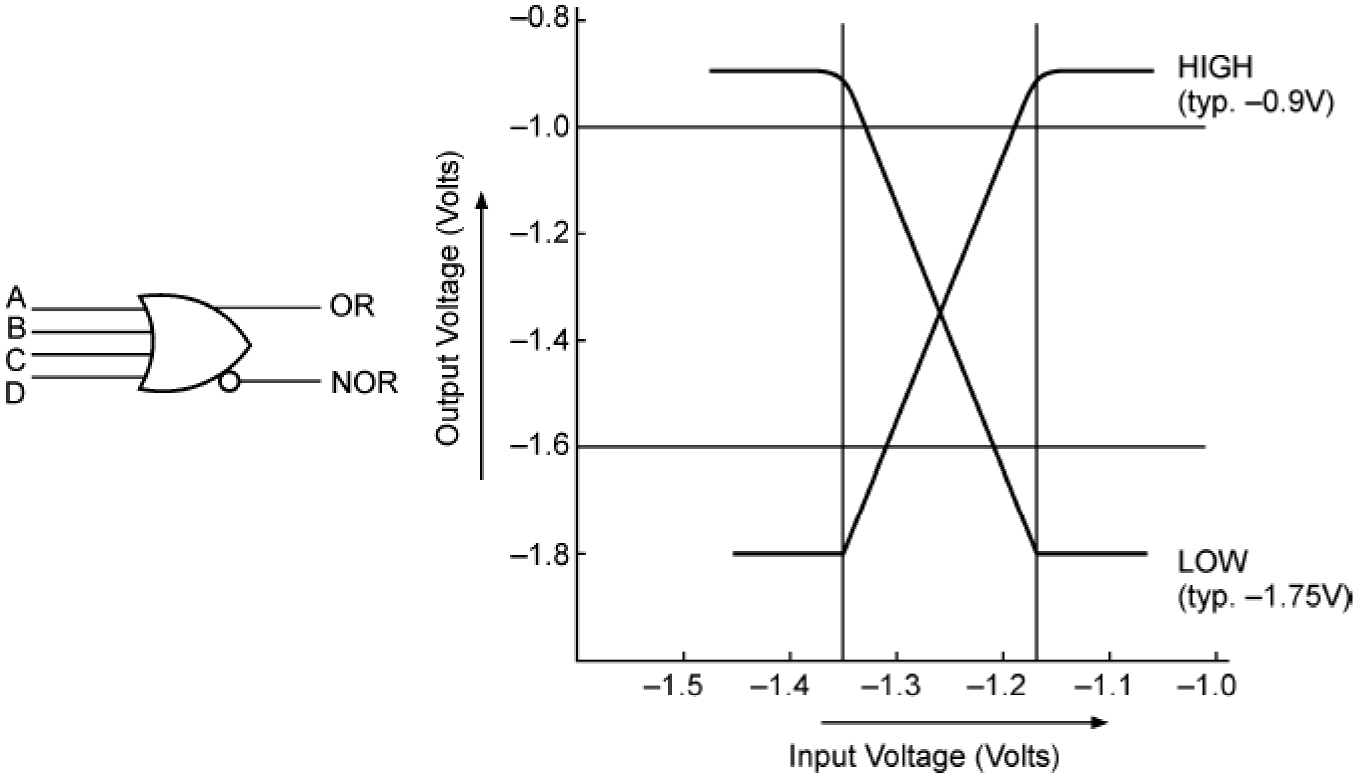
iii) higher consumption

- Emitter-Coupled Logic (origin)



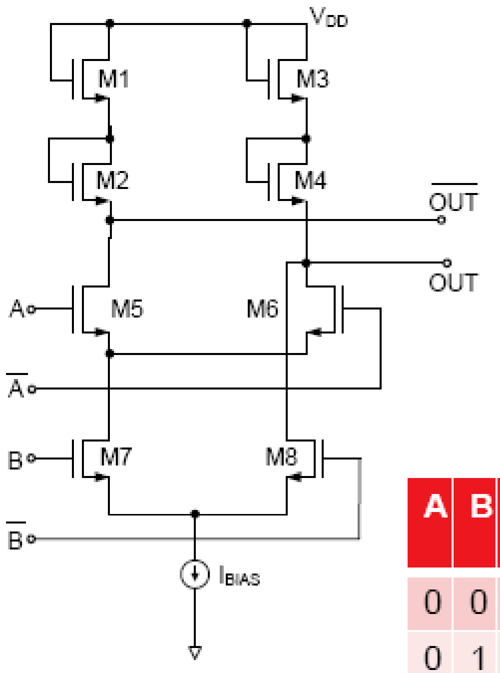
OR/NOR in ECL.

- Emitter-Coupled Logic



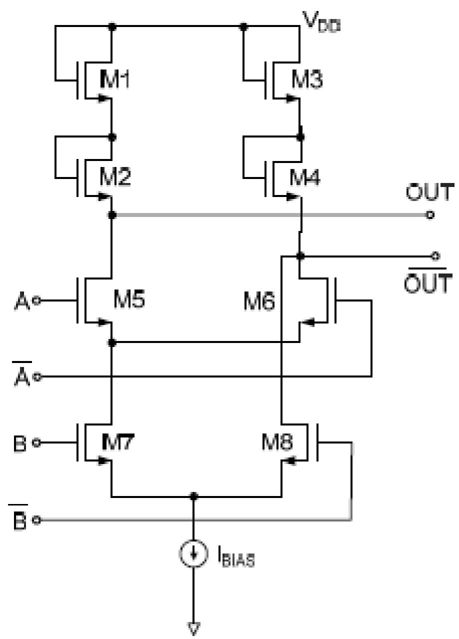
ECL input/output characteristics.

CML AND / NAND gates



AND

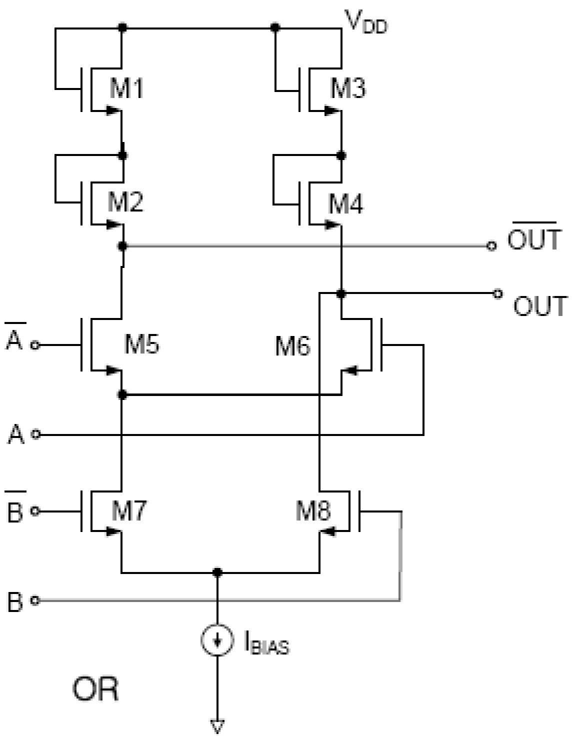
A	B	out	out-not
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

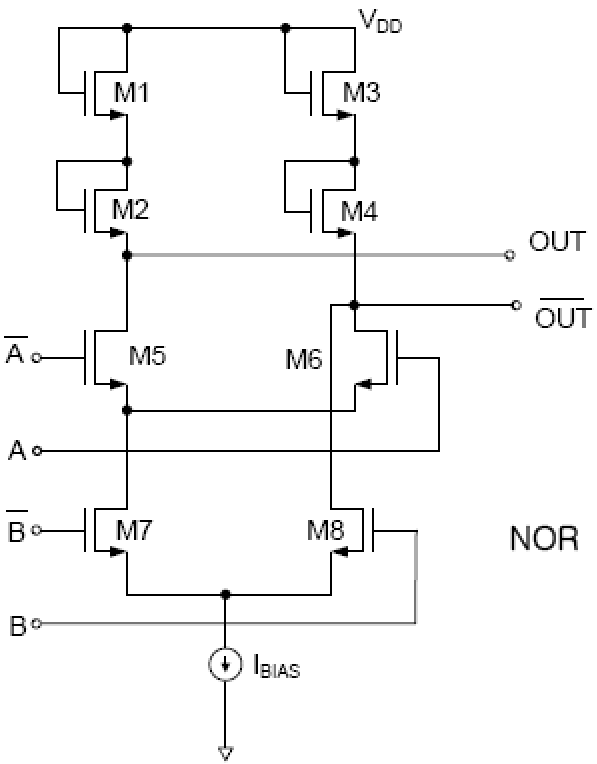


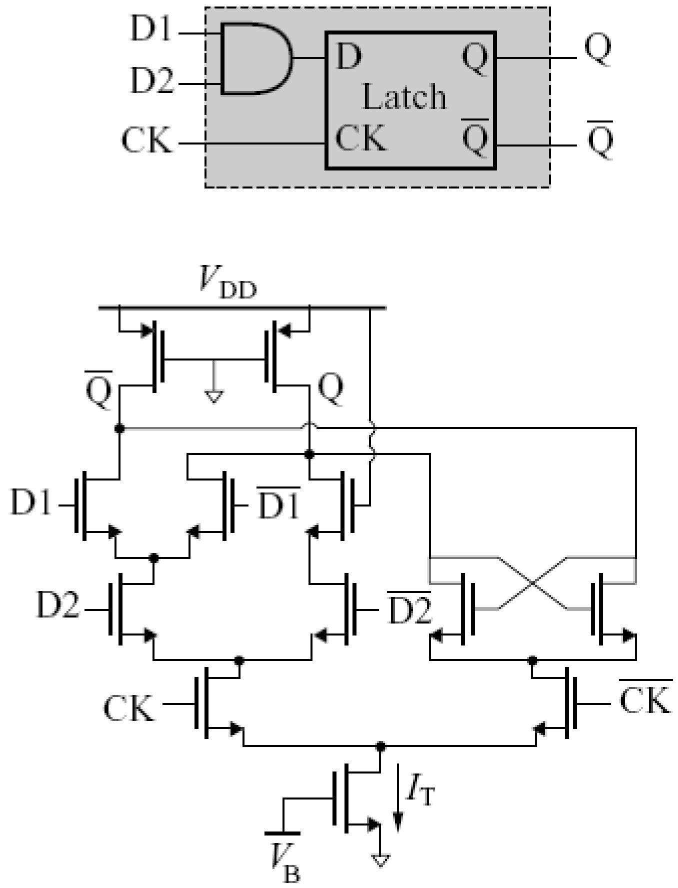
NAND

A	B	out	out-not
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

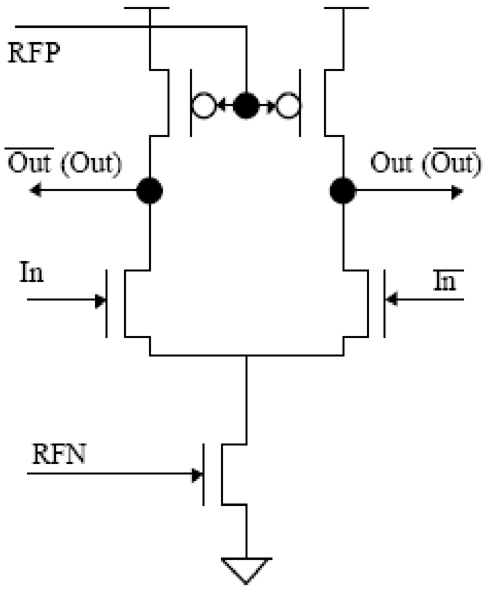
CML OR / NOR gates



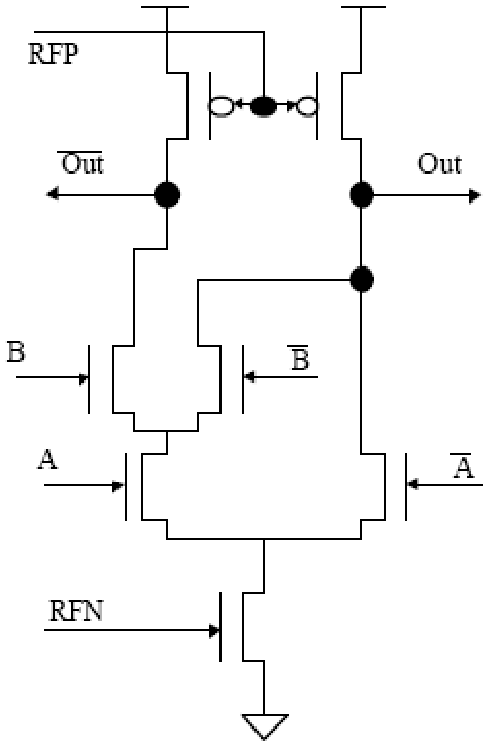




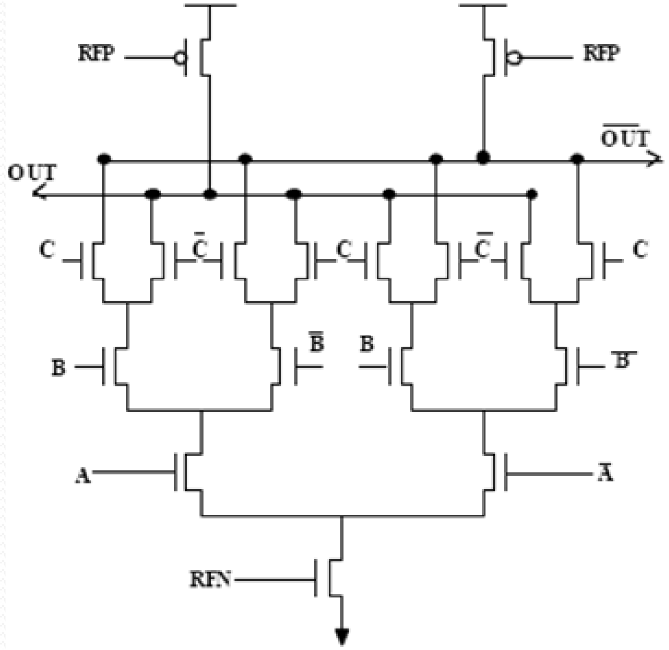
Merged AND gate and D-type latch in CML logic



Buffer/Inverter



AND/NAND/OR/NOR



XOR3