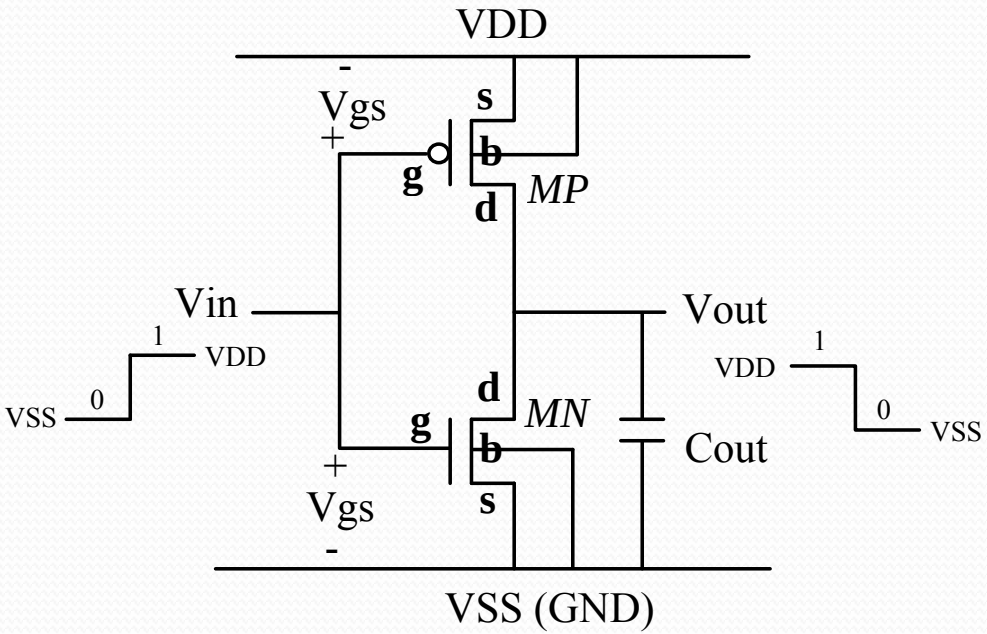
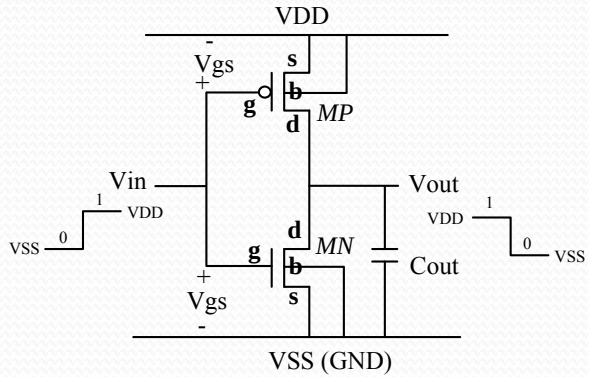
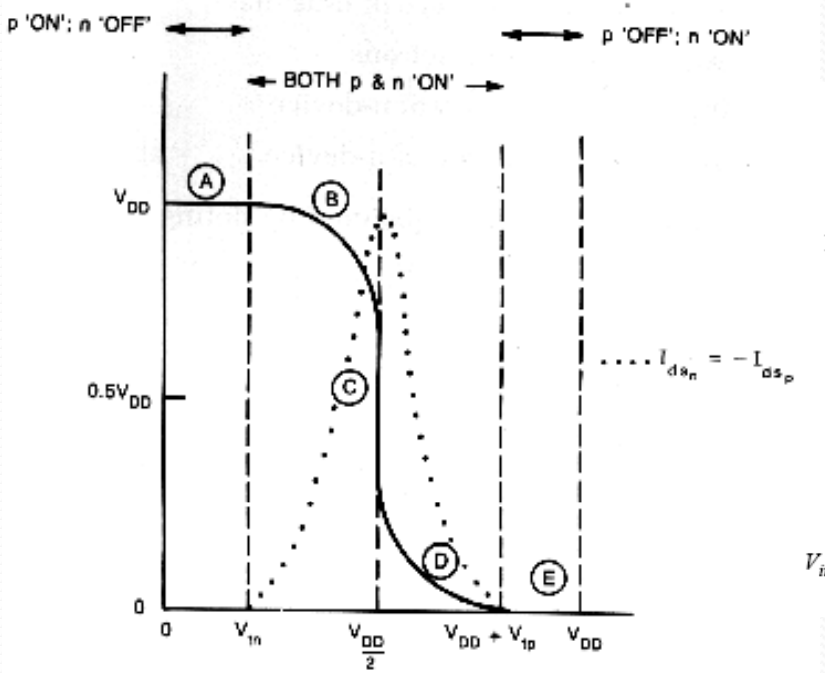
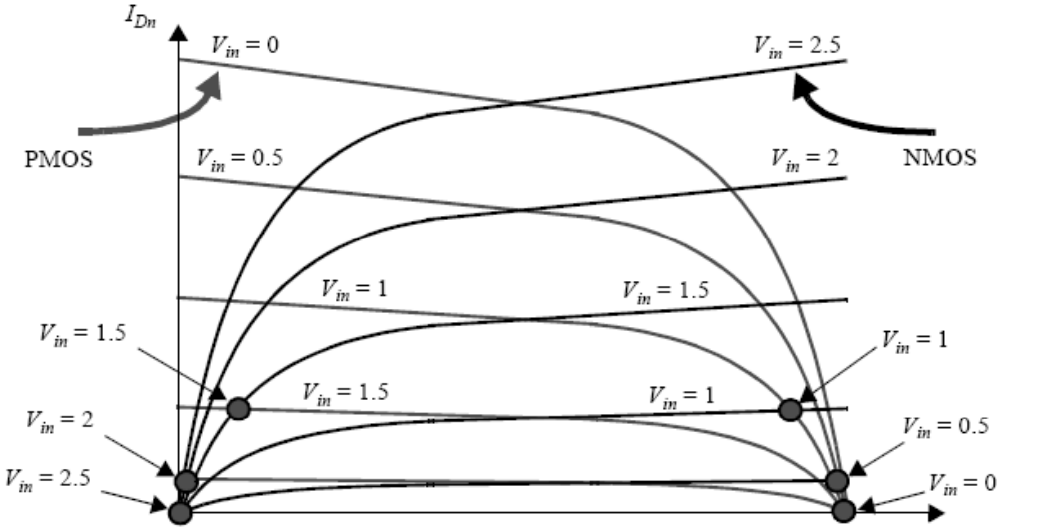
CMOS LOGIC GATES

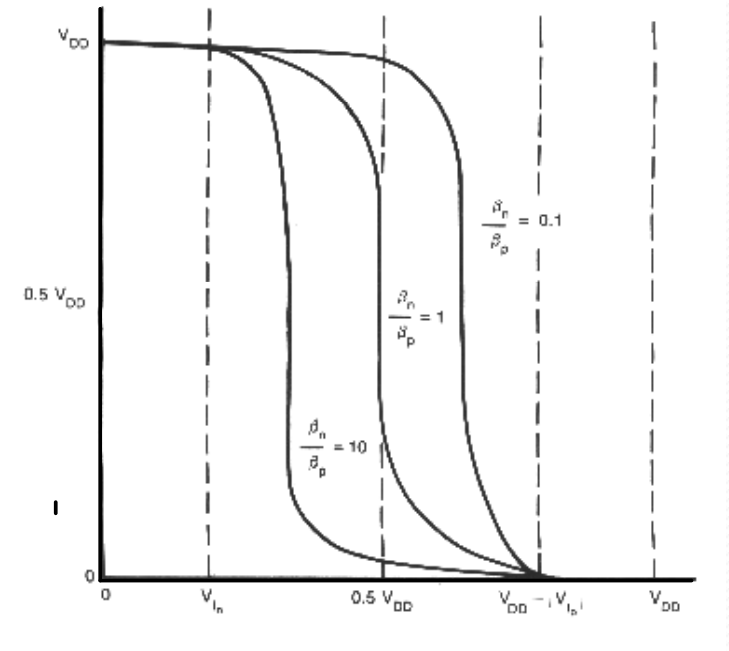
- CMOS inverter

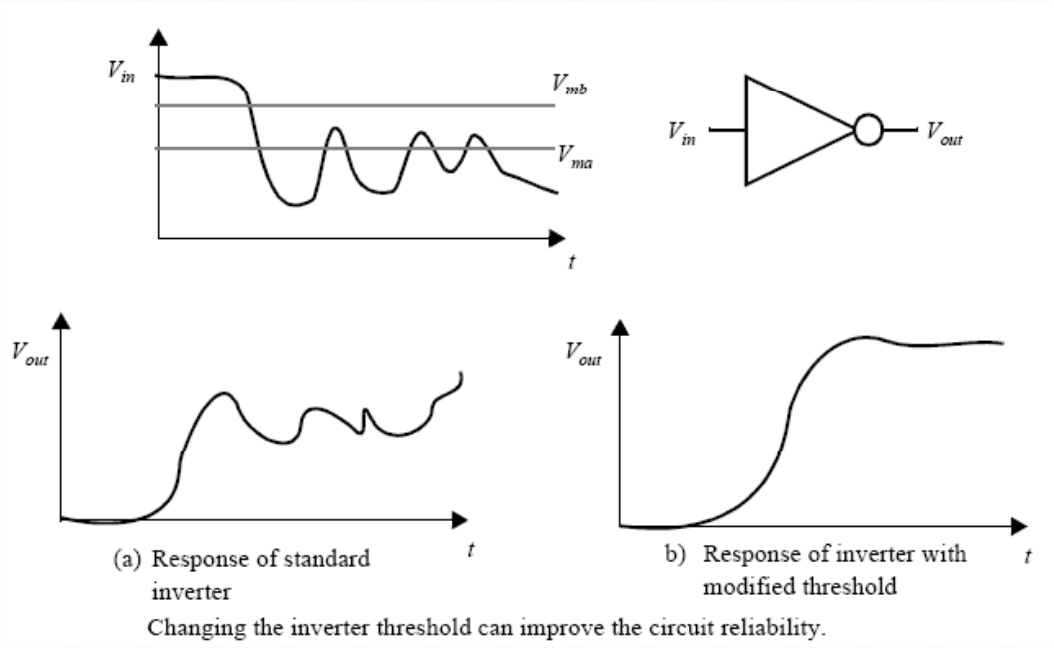



VDD
Vgs
s
b
g
d
MP
Vin
1
VDD
VSS
0
Vout
VDD
1
0
VSS
d
g
MN
b
Cout
Vgs
s
VSS (GND)


p 'ON'; n 'OFF'
p 'OFF'; n 'ON'
BOTH p & n 'ON'
A
B
C
D
E
V_{DD}
$0.5V_{DD}$
0
$I_{ds_n} = -I_{ds_p}$
0
V_{tn}
$\frac{V_{DD}}{2}$
$V_{DD} + V_{tp}$
V_{DD}


I_{Dn}
$V_{in} = 0$
$V_{in} = 2.5$
PMOS
NMOS
$V_{in} = 0.5$
$V_{in} = 2$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 2$
$V_{in} = 0.5$
$V_{in} = 2.5$
$V_{in} = 0$





(a) Response of standard inverter

b) Response of inverter with modified threshold

Changing the inverter threshold can improve the circuit reliability.

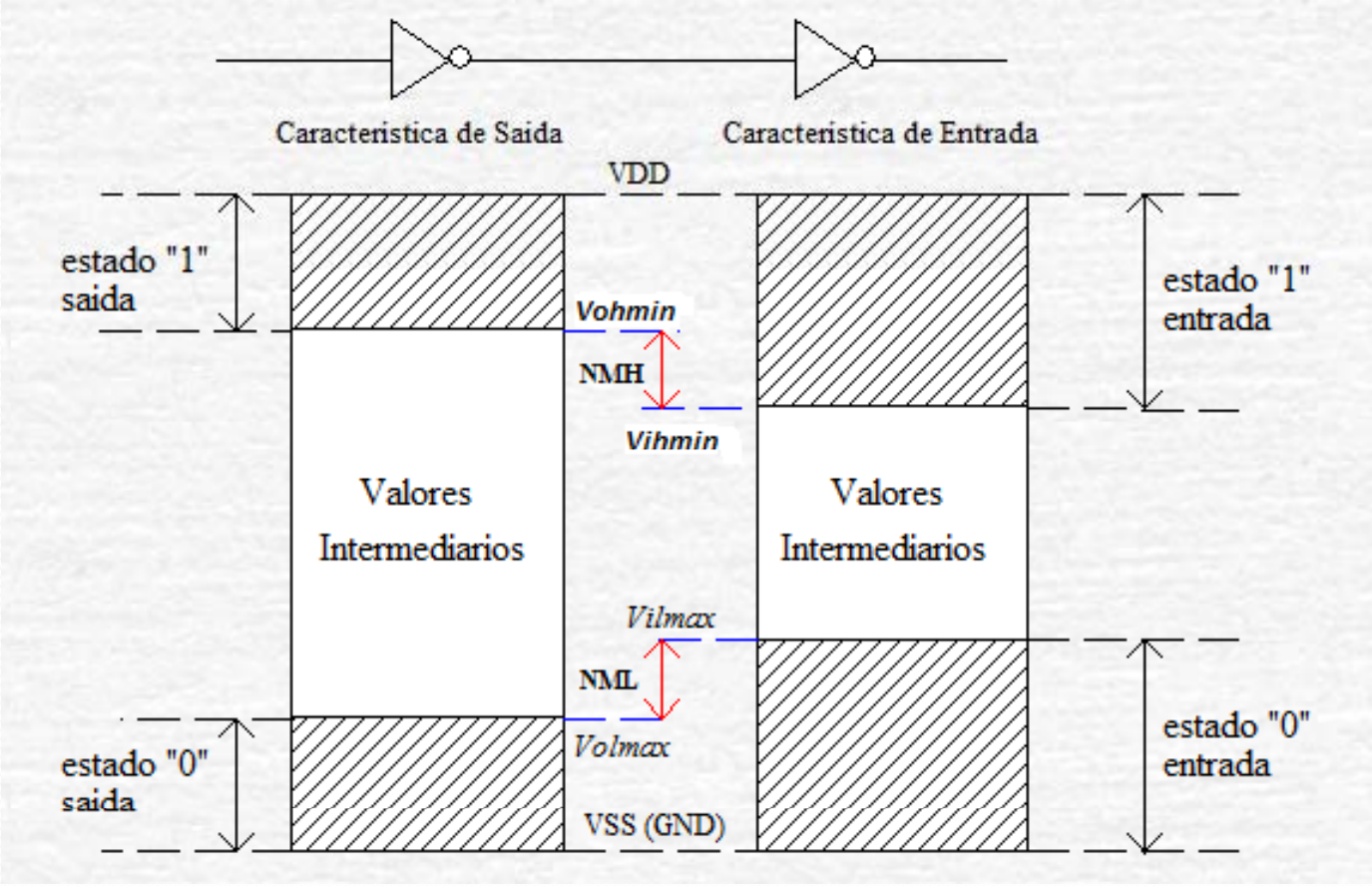
Inverter Noise Margin

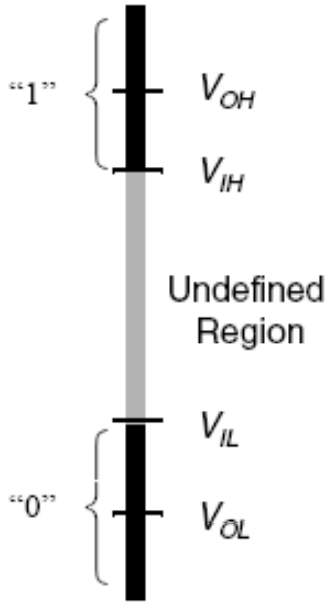
• Determines the maximum noise voltage at input of inverter – or logic gate - that does not affect the logic state at output.

• This margin – or noise immunity – is defined in terms of parameters NM_L (*Low Noise-Margin*) and NM_H (*High Noise-Margin*).

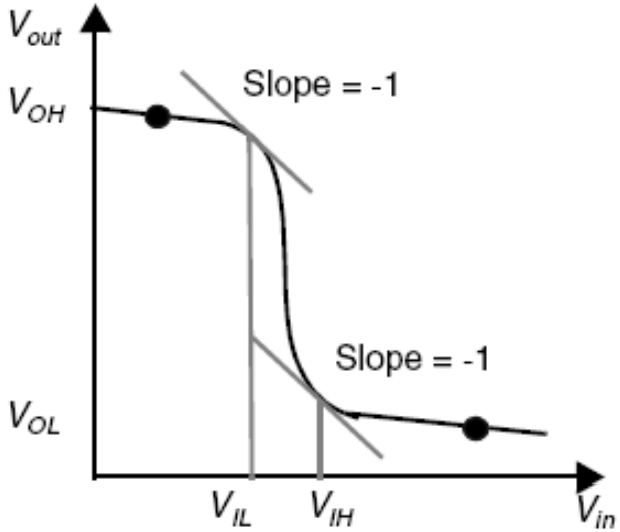
$$NM_L = |V_{OLmax} - V_{ILmax}|$$

$$NM_H = |V_{OHmin} - V_{IHmin}|$$


Caracteristica de Saida
Caracteristica de Entrada
VDD
estado "1"
saida
Vohmin
NMH
Vihmin
Valores
Intermediarios
Valores
Intermediarios
estado "1"
entrada
Vilmax
NML
Volmax
estado "0"
saida
VSS (GND)
estado "0"
entrada



(a) Relationship between voltage and logic levels



(b) Definition of V_{IH} and V_{IL}

At condition $\beta_n = \beta_p$ one has:

$$NM_H = (3V_{DD} - 5V_{THP} - 3V_{THN}) / 8$$

$$NM_L = (3V_{DD} + 3V_{THP} + 5V_{THN}) / 8$$

$\Rightarrow$ Noise margins

a. Decrease with the magnitude of threshold voltage
b. decrease with VDD

Ex: for $V_{THN} = - V_{THP} = 0.2\ V_{DD}$,

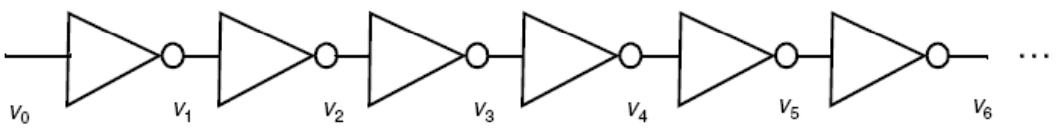
$$NM_L = NM_H = (3 + 1 - 0.6)\ V_{DD} / 8 = 0.425\ V_{DD}$$

If $V_{DD} = 2.5V \rightarrow NM_L = NM_H = 1.06V$

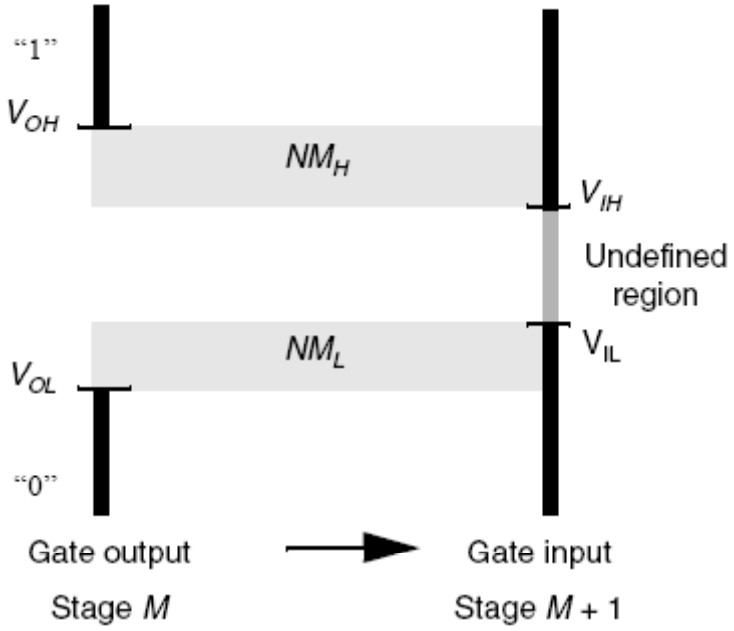
$V_{DD} = 1.5V \rightarrow NM_L = NM_H = 0.63V$

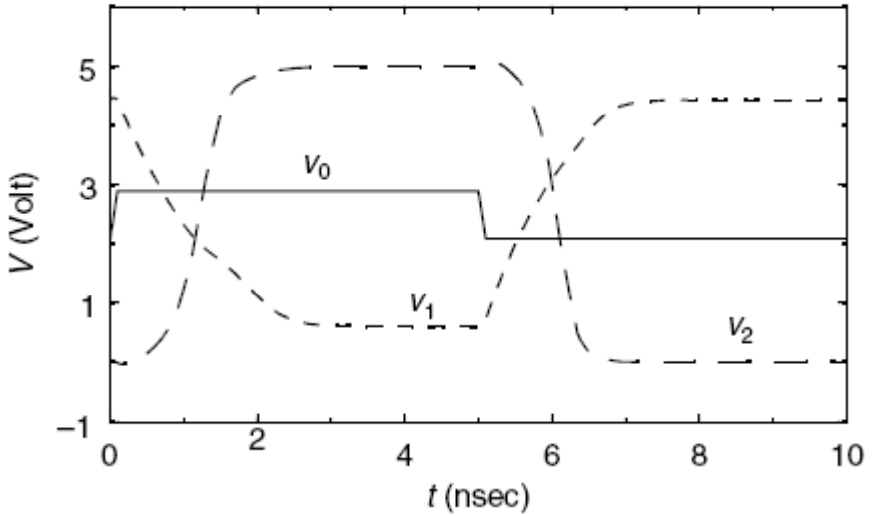
$\Rightarrow$The inverter may be subject to swithcing noise at its input and present a false output transistion

The regenerative property of inverter chain:

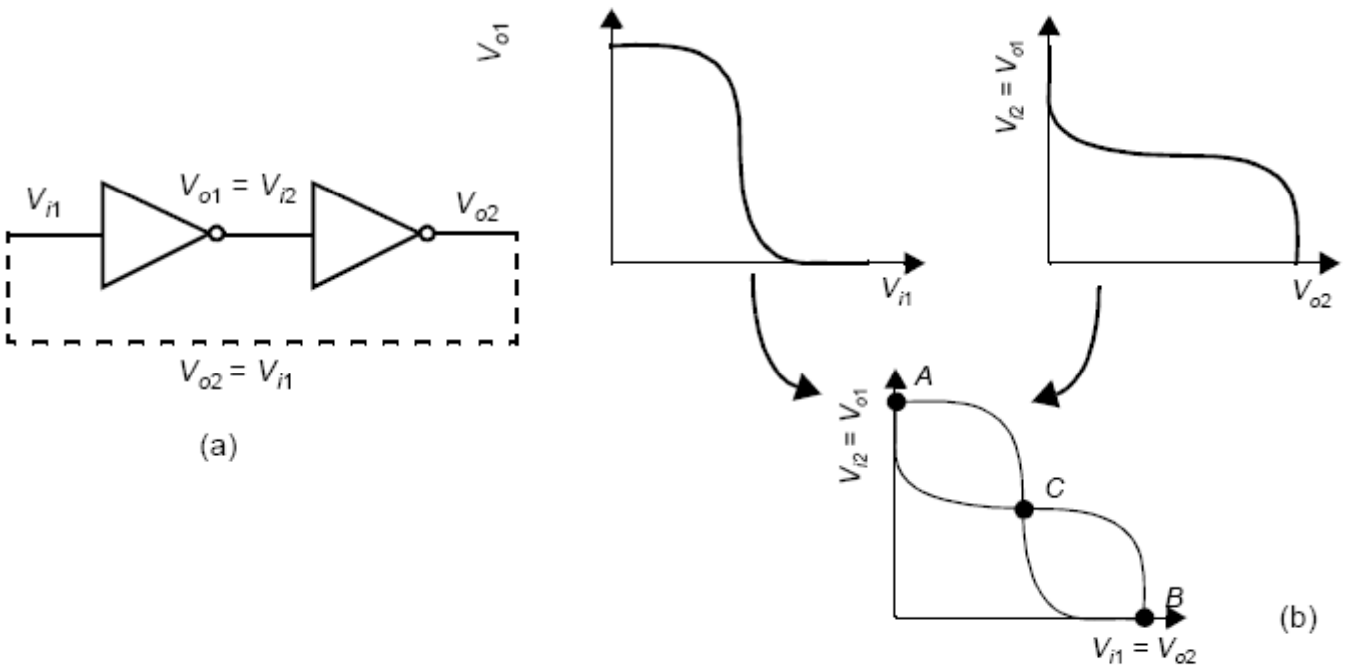


A chain of inverters

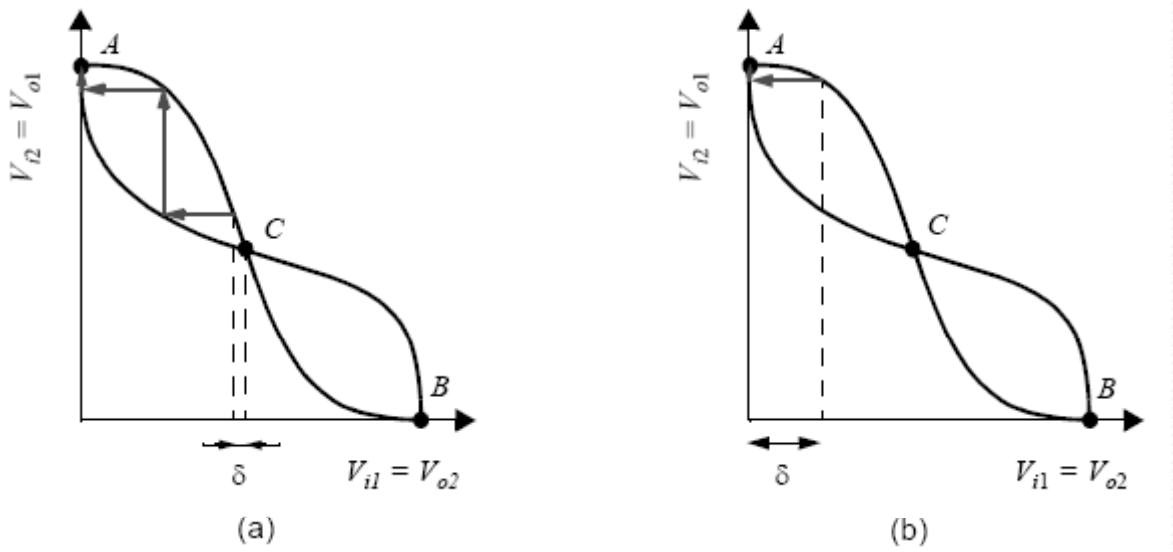




Simulated response of chain of MOS inverters



Two cascaded inverters (a) and their VTCs (b)

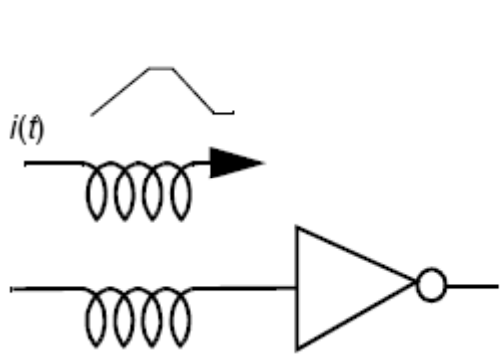


Metastability.

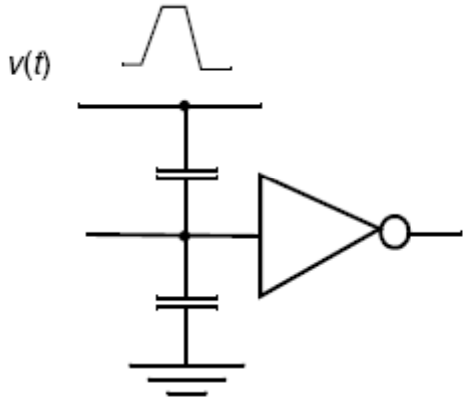
Noise sources in digital circuits:

• Most noise in a digital system is internally generated, and the noise value is proportional to the signal swing (i.e., to VDD!)

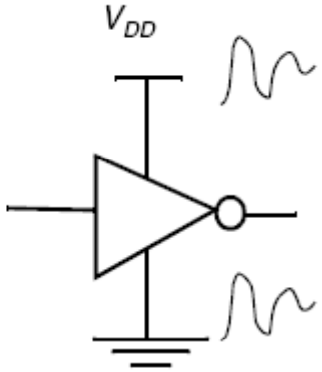
Ex: capacitive and inductive cross talk and internally-generated power supply noise



Inductive coupling



Capacitive coupling



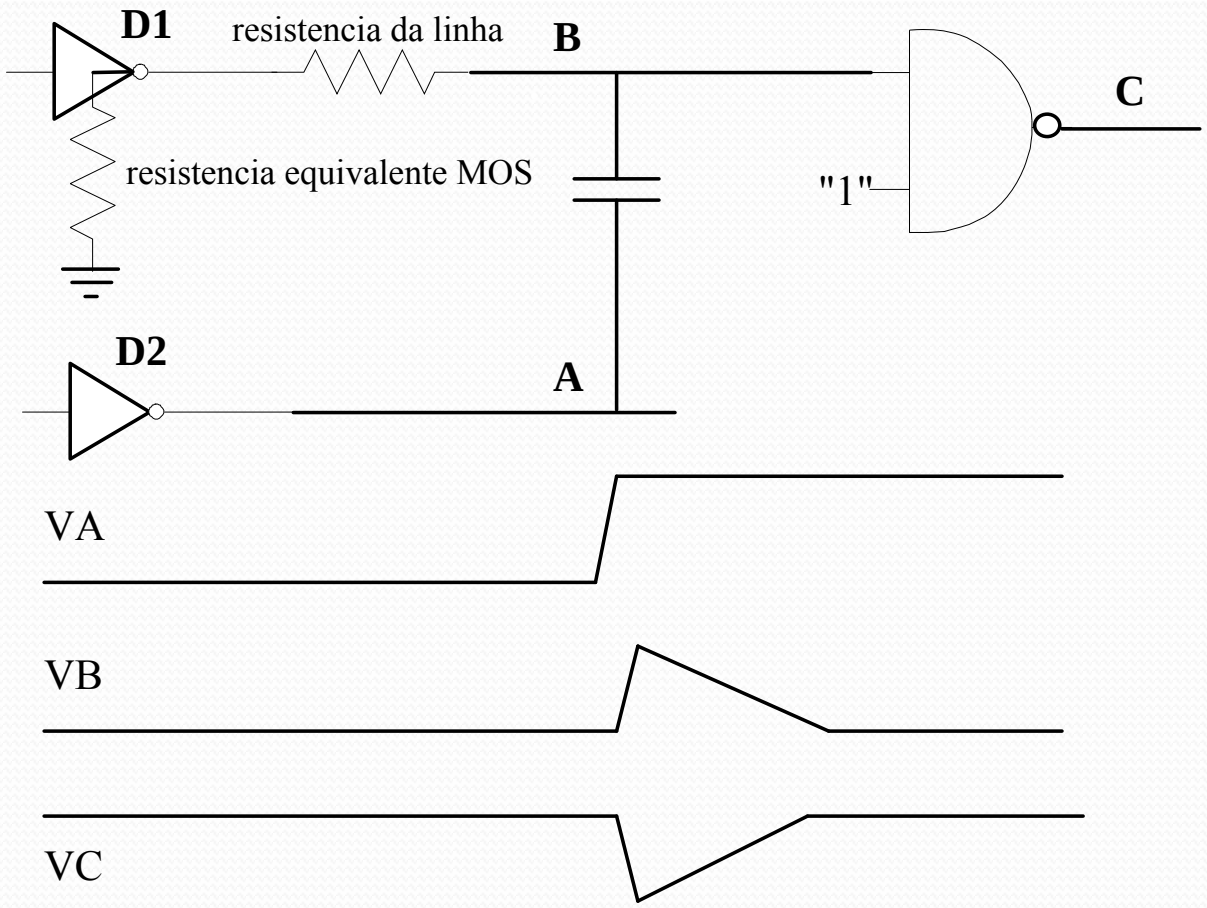
Power and ground noise

- Switching noise from capacitive coupling

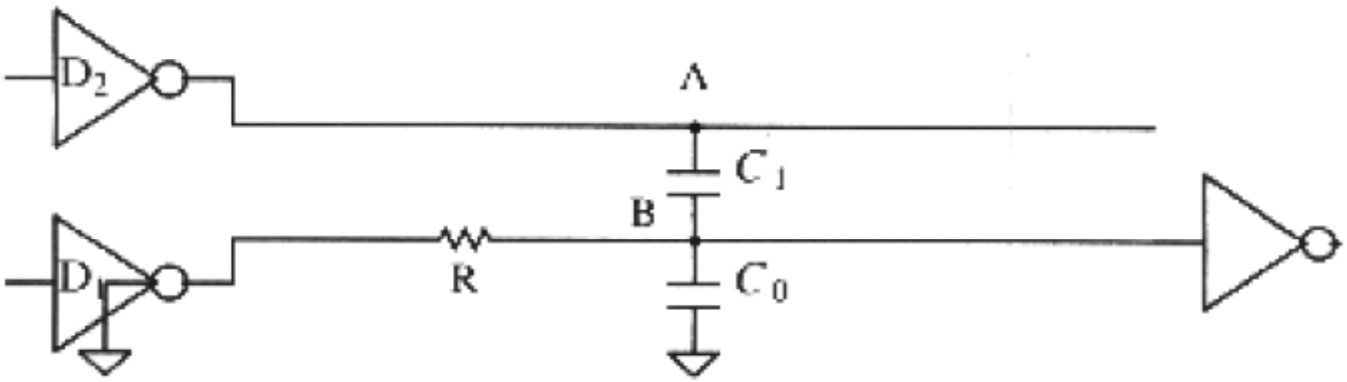
  i) through interconnecting lines
  ii) introduced by power bus

Ref: “CMOS Digital Circuit Technology”, Shoji M., Prentice-Hall.

i) noise coupling through interconnections



metal-metal



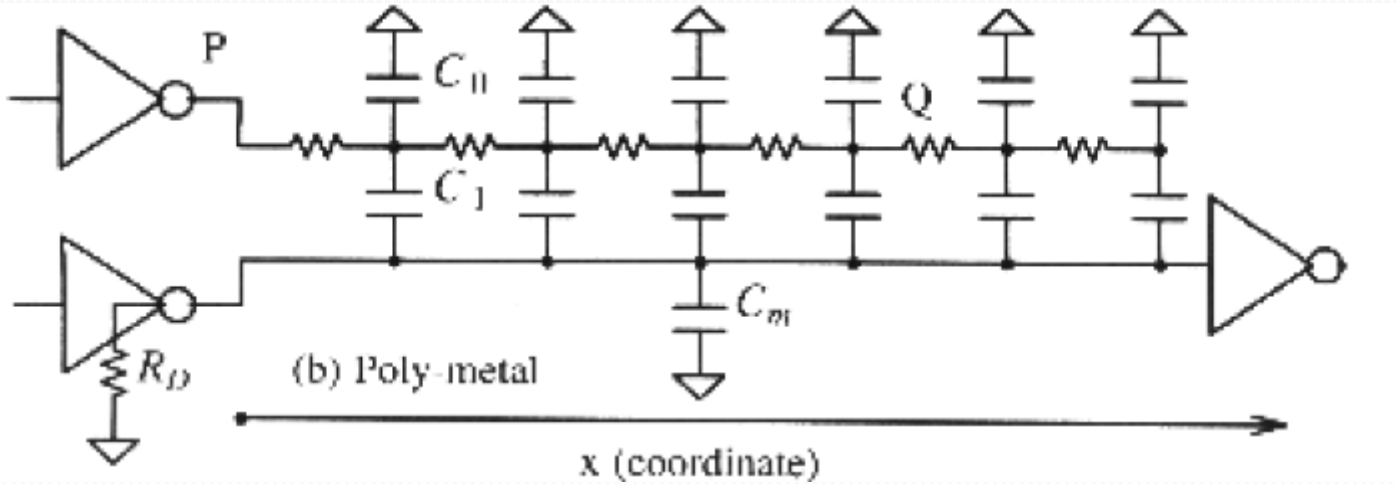
(a) Metal-metal induced noise

$$V_B(t) = \frac{C_1}{C_0 + C_1} V_{DD} \exp\left(-\frac{1}{R(C_0 + C_1)} \right)$$

Worst-case: superposition of lines: C1 = C0 e $V_{Bpeak} = 1/2V_{DD}$

Assuming C1 + C0 = 2pF (1cm) and R = 5KΩ, spike duration is ≅ 10ns!

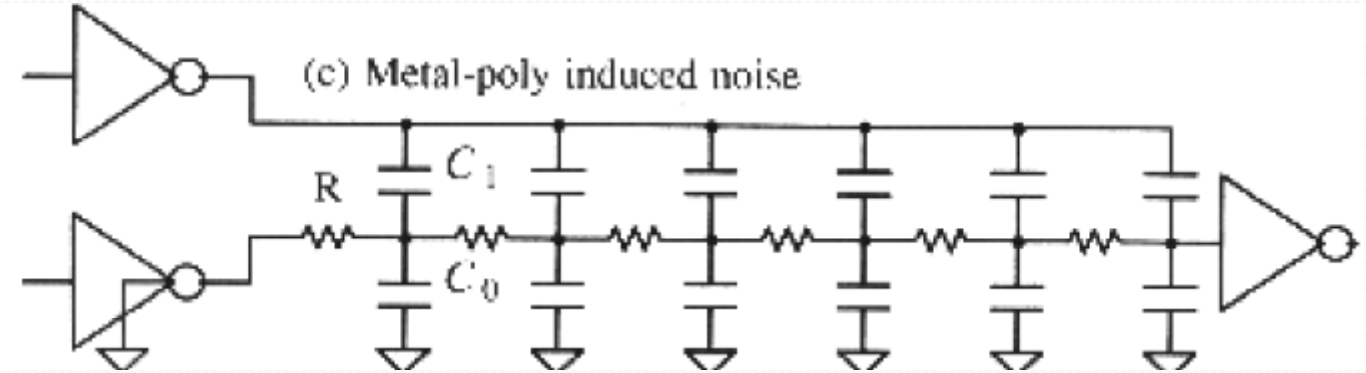
poly-metal



$$\text{peak} = \frac{C_1}{C_0 + C_1}\left[\frac{(C_0 + C_1)L}{Cm}\frac{R_D}{R.L}\right]^{0.5}$$

if C1 + C0 = 2pF, (C0+C1)L/Cm = 1 and RD/(R.L) = 1/7
$\Rightarrow$ spike amplitude $\cong$ 0.1VDD

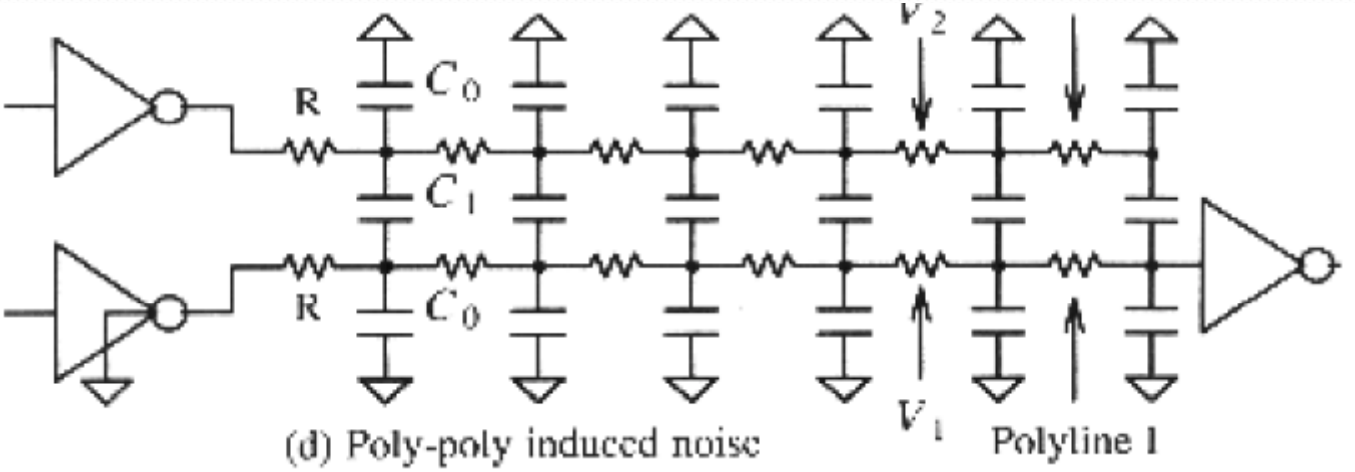
metal-poly



$$t_{spike} = 1.1R\left(C_0 + C_1\right)x^2$$

If R = 4Ω/□, t_{spike} = 2.7ns for x = 2mm (narrow pulse)

poly-poly



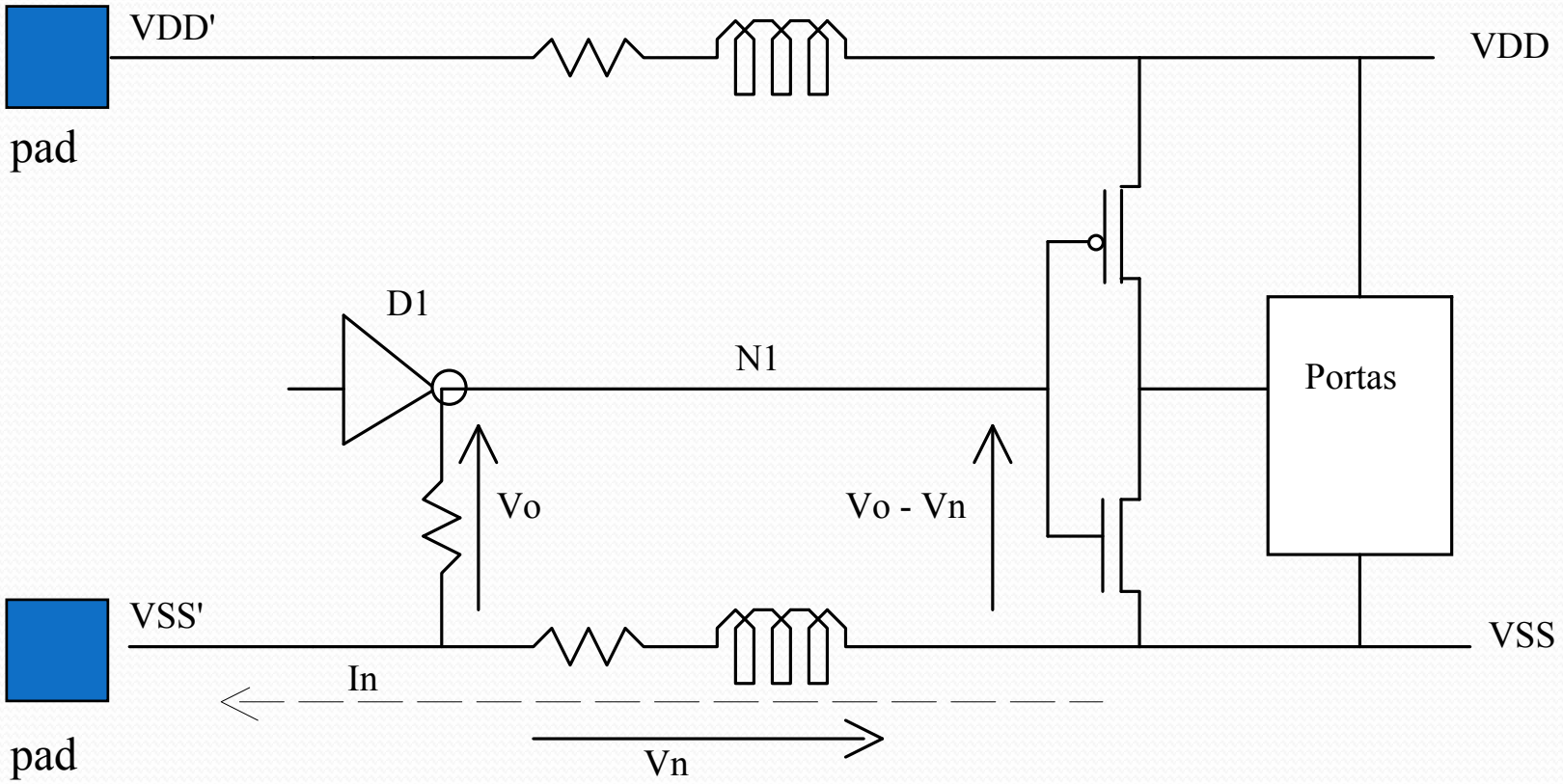
Spike amplitude ; $0.05V_{DD}$ (not important!)

ii) Noise through Power Bus (VDD e GND)

• signal flow in the digital system is controlled by a clock, so that all transitions become synchronized.

• in every transition at a CMOS gate, there´s a current flowing from V_{DD} e GND, besides the transient component due to load capacitance charge/discharge.

⇒ Great number of simultaneous transitions all over the digital circuit leads to meaningful current spikes I_{DD} and I_{GND}


VDD'
pad
VDD
D1
N1
Portas
Vo
Vo - Vn
VSS'
VSS
In
pad
Vn

• changes in V_{DD} e GND voltages due to distribuited resistance (R) and inductance indutância (L) in power buses

$$\Delta V_{res} = R \times I$$

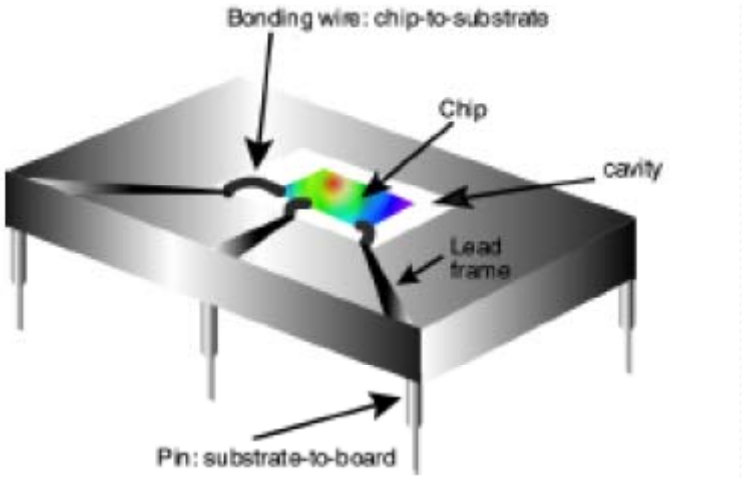
$$\Delta V_{ind} = L \, (dI/dt)_{max}$$

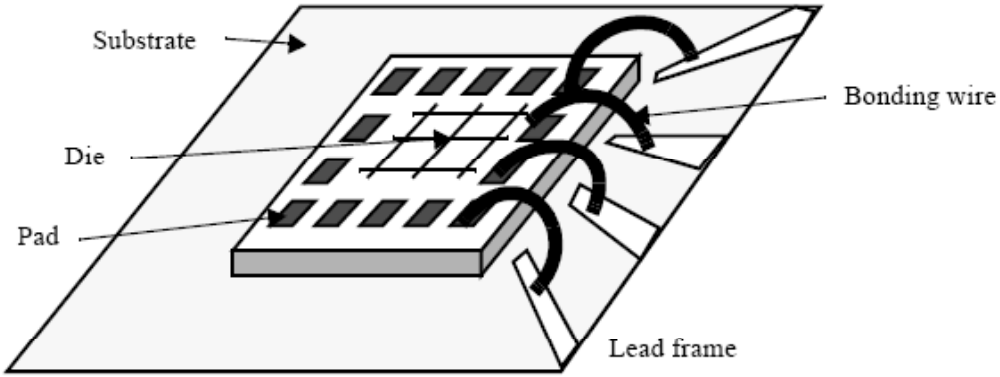
• As $(dI/dt)_{max} = k \, (1/T_{swt})$, where T_{swt} is the switching time of a logic gate and *k* is a constant, function of the waveform

$$\Rightarrow \Delta V_{ind} / \Delta V_{res} = k \, (L / R) \, (T_{swt}/I)$$

where L/R is the power line time constant (on-chip metallization + Bond wirings + packaging + PCB tracks)

- interconnect in IC packaging

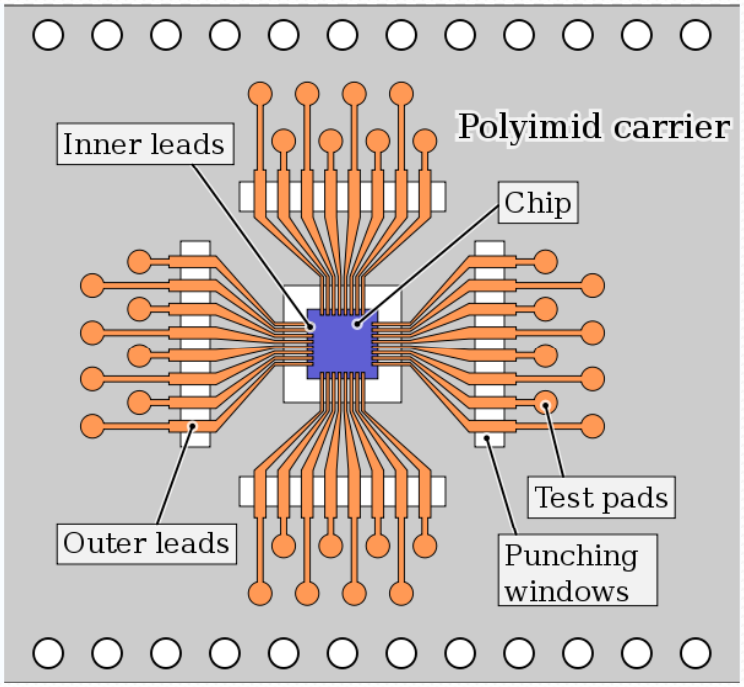


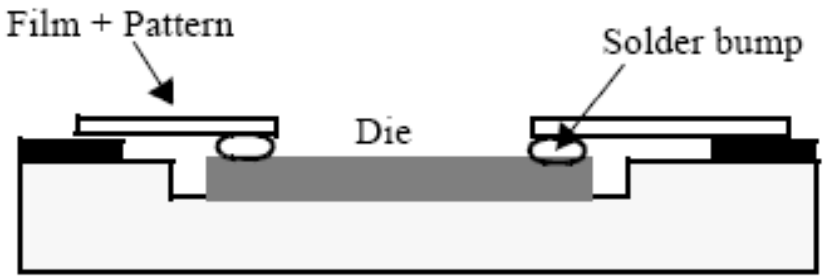


Bonding wires have inferior electrical properties:

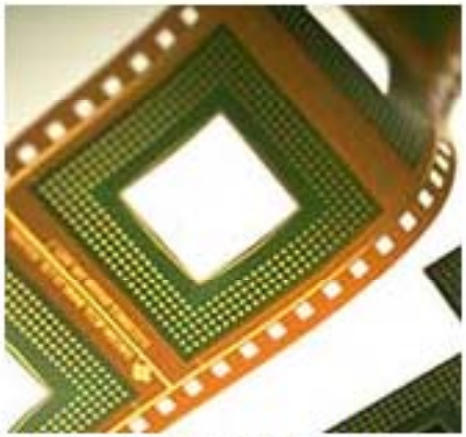
- high individual inductance (+5 nH) and mutual inductance with neighboring signals.
- Typically 1 nH/mm, while the inductance per package pin 7 - 40 nH (per pin)

Tape-automated bonding (TAB) places bare ICs onto PCB by attaching them to a polyamide film (ex: LCD display driver circuits)

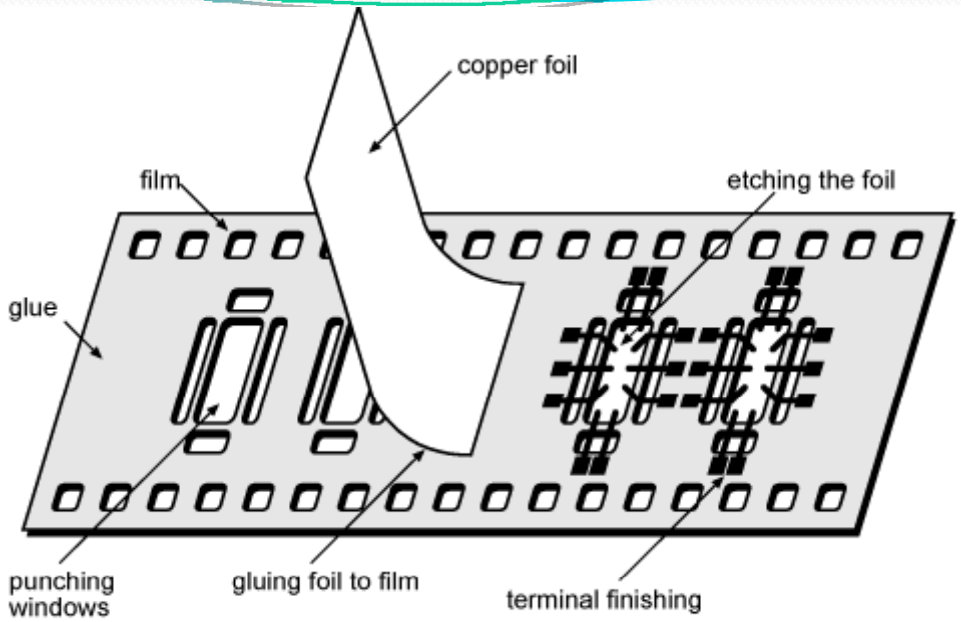


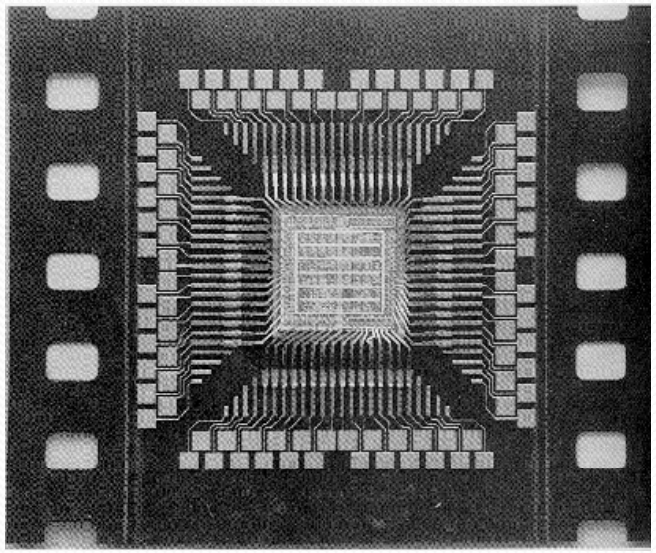


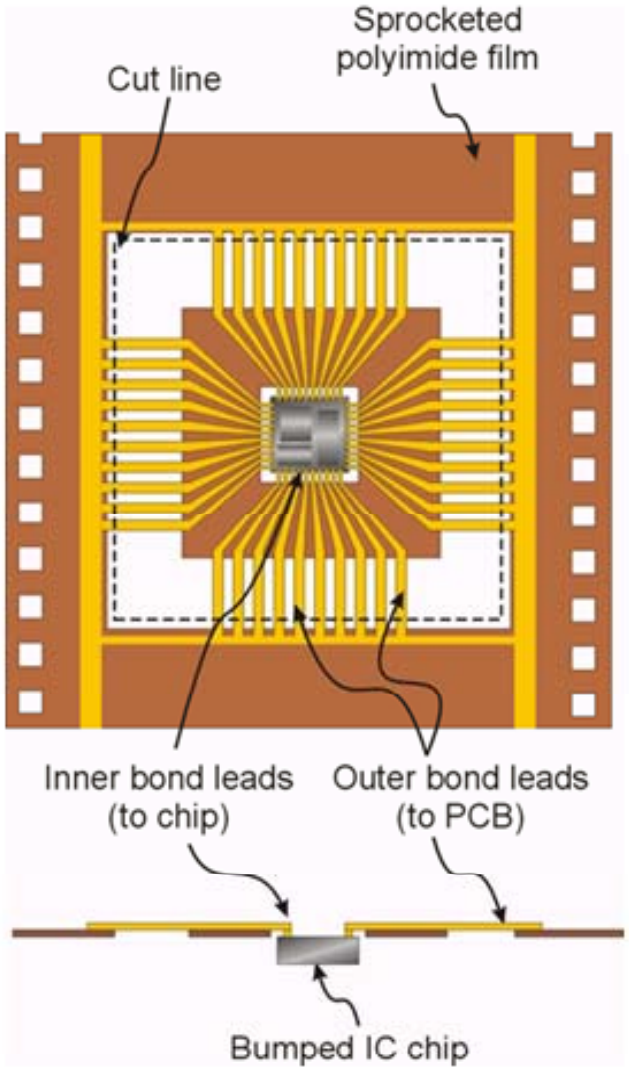
Die attachment using solder bumps



TAB (Tape Automated Bonding)

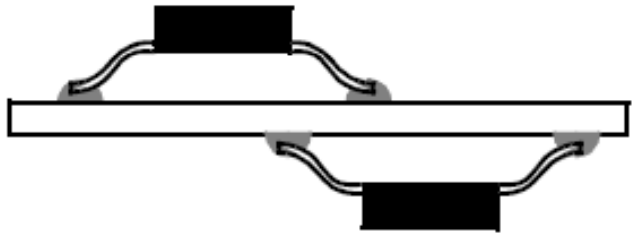


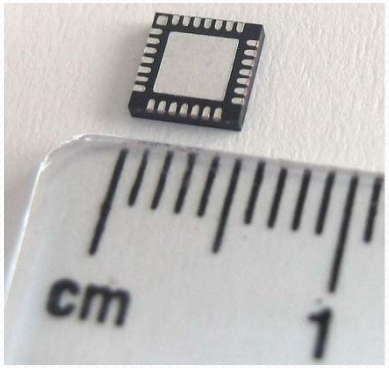


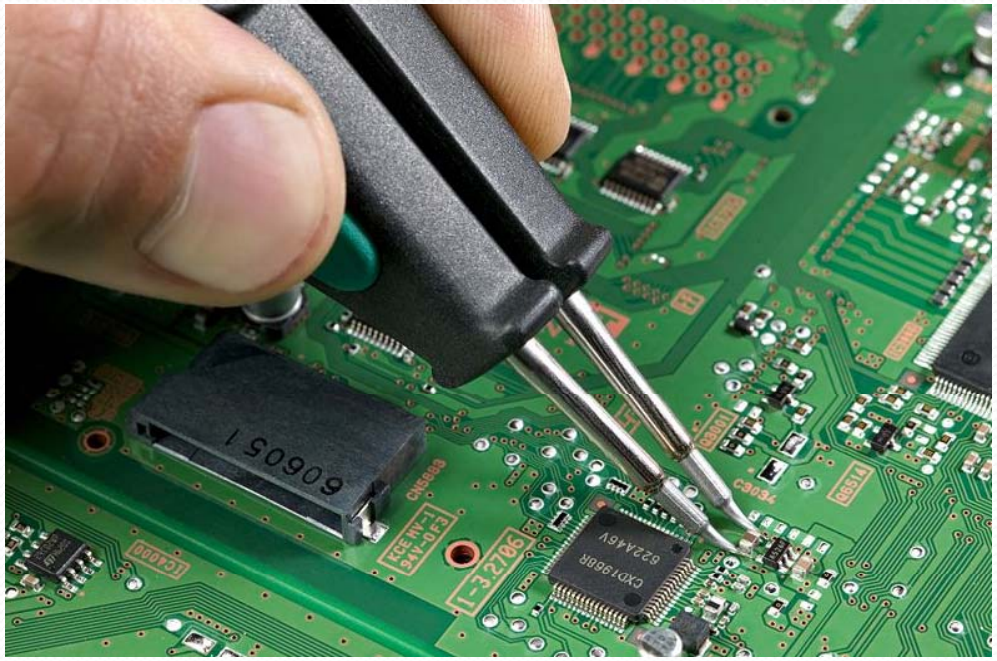


Tape Automated Bonding

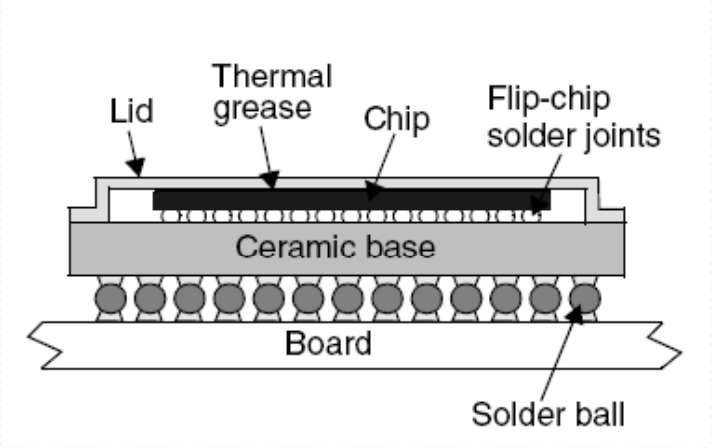
- Surface Mounting Devices (SMD)

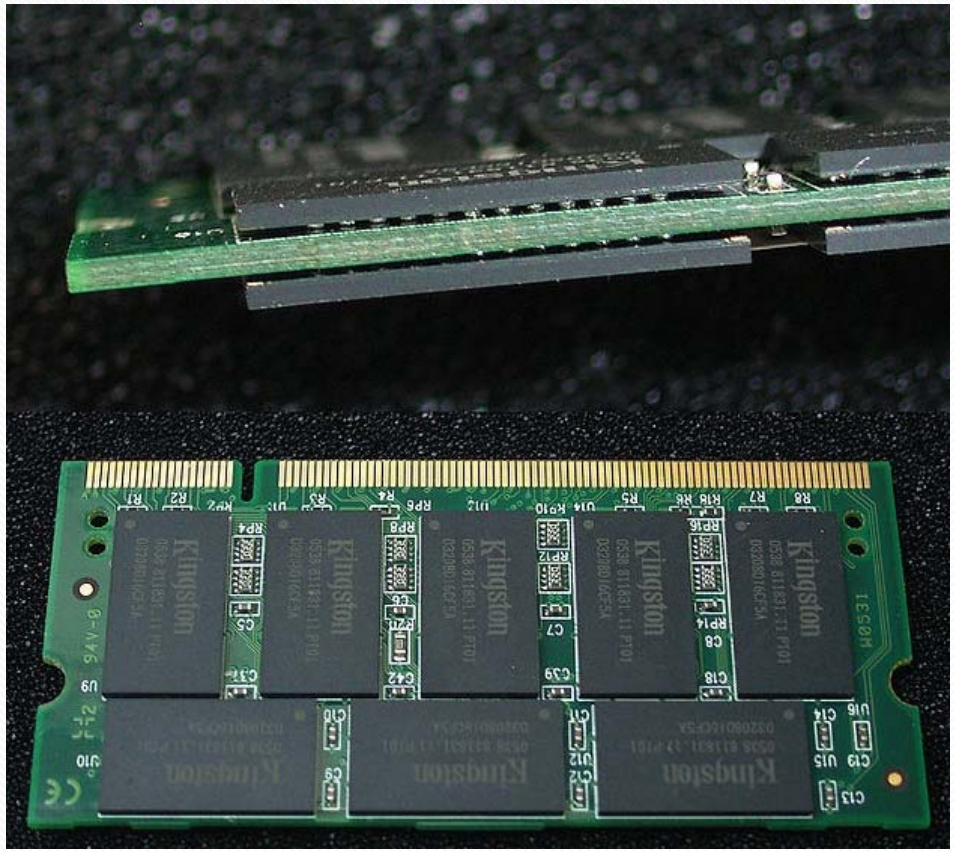






- Ball Grid Array (BGA)



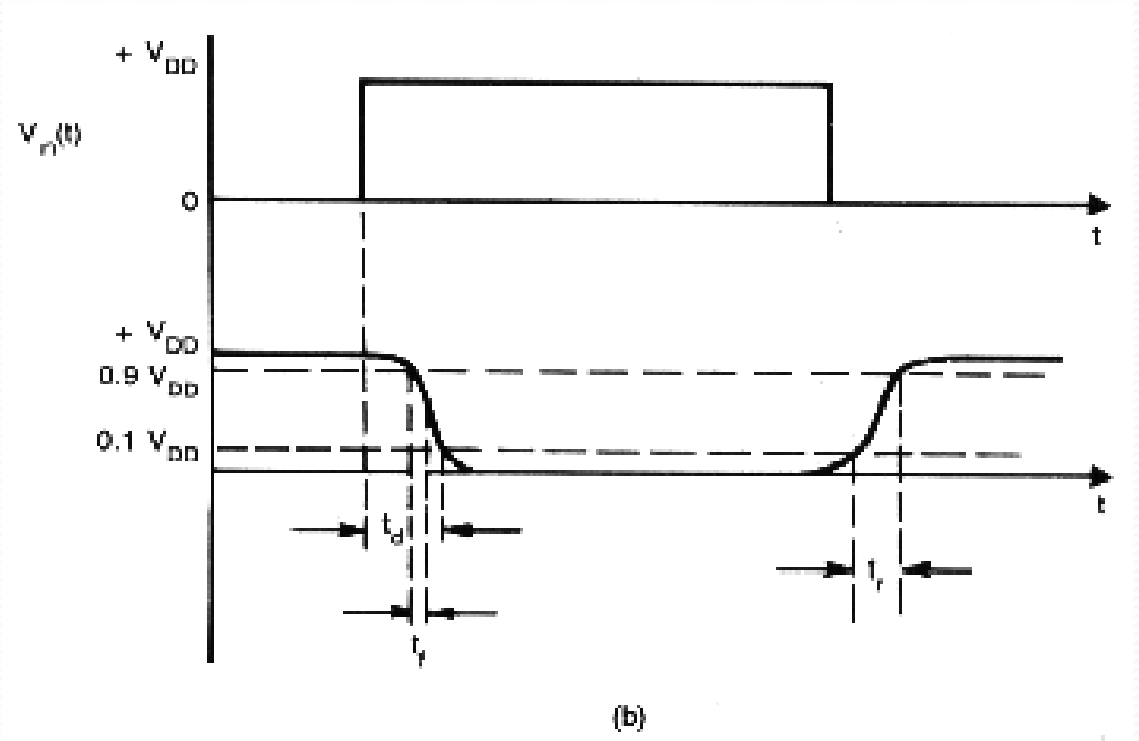


Typical capacitance and inductance values of package and bonding styles

Package Type	Capacitance (pF)	Inductance (nH)
68-pin plastic DIP	4	35
68-pin ceramic DIP	7	20
256-pin grid array	1–5	2–15
Wire bond	0.5–1	1–2
Solder bump	0.1–0.5	0.01–0.1

Condutors	L (nH/cm)	R (Ω/cm)	L/R (ns)
Aluminum Wire (1 mil)	7.37	0.58	12.80
V_{DD} Line (100µm)	7.42	2.82	2.63
V_{DD} Line (40µm)	9.21	7.06	1.30
V_{DD} Line (20µm)	10.59	14.12	0.75
V_{DD} Line (5µm)	13.36	56.4	0.24

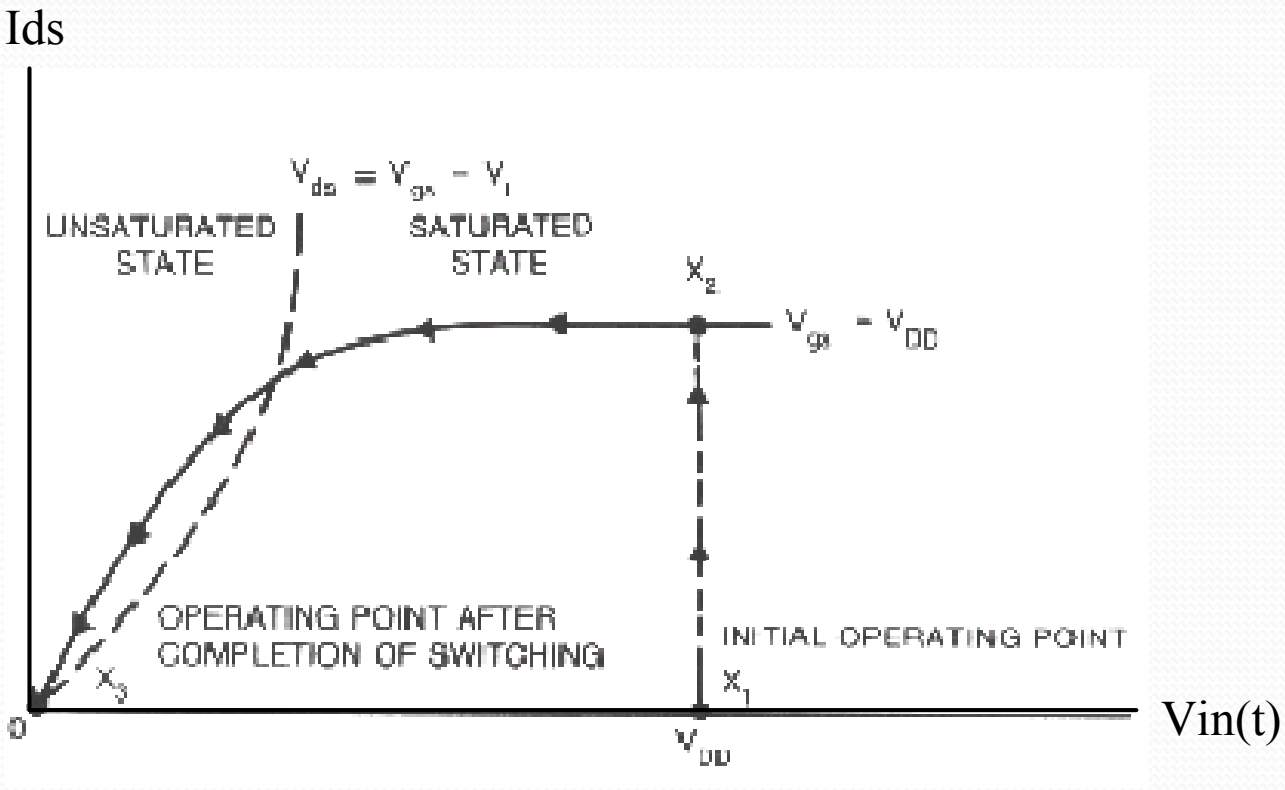
Inverter Switching Caracteristics



(b)

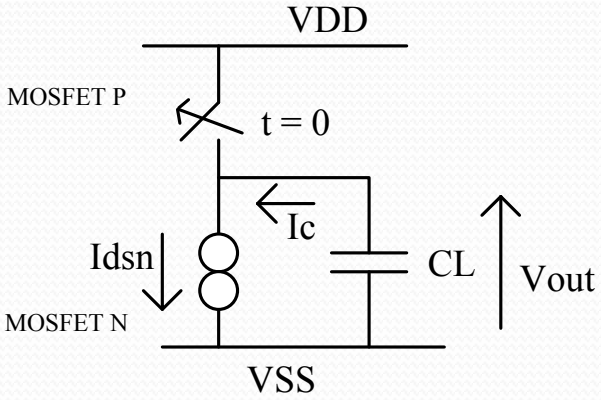
i) rising time: swing from 10% to 90% of final value
ii) fall time: swing from 90% to 10% of final value
iii) delay time: 50% of input transition to 50% of output transition

CMOS Inverter Fall Time

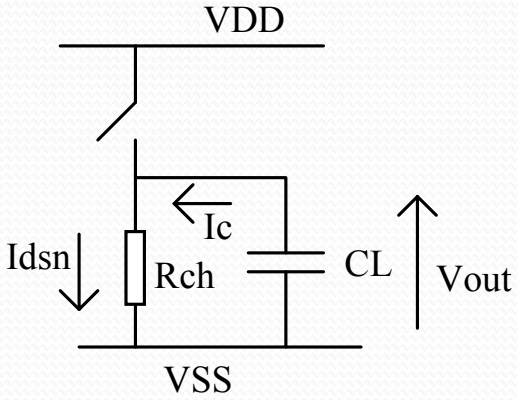


Assuming $V_{THN} = 0.2\ V_{DD}$, $\Rightarrow t_f = 4\ C_L / (\beta_n\ V_{DD})$

Transição Negativa à Saida

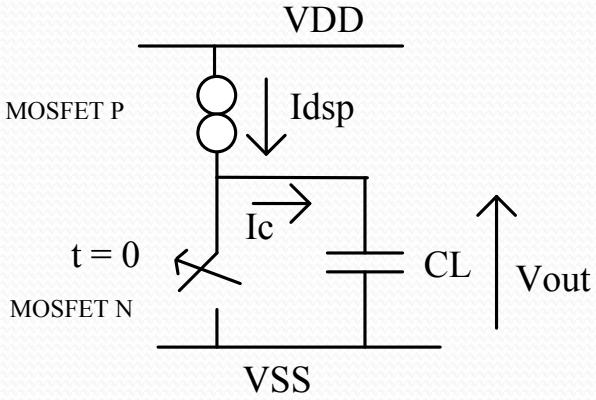


Saturação: Vout > VDD - Vthn

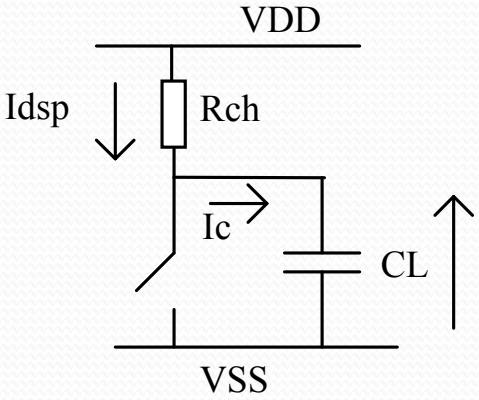


Linear: 0 < Vout < VDD - Vthn

Transição Positiva à Saida



Saturação: Vout < - VDD + Vthp



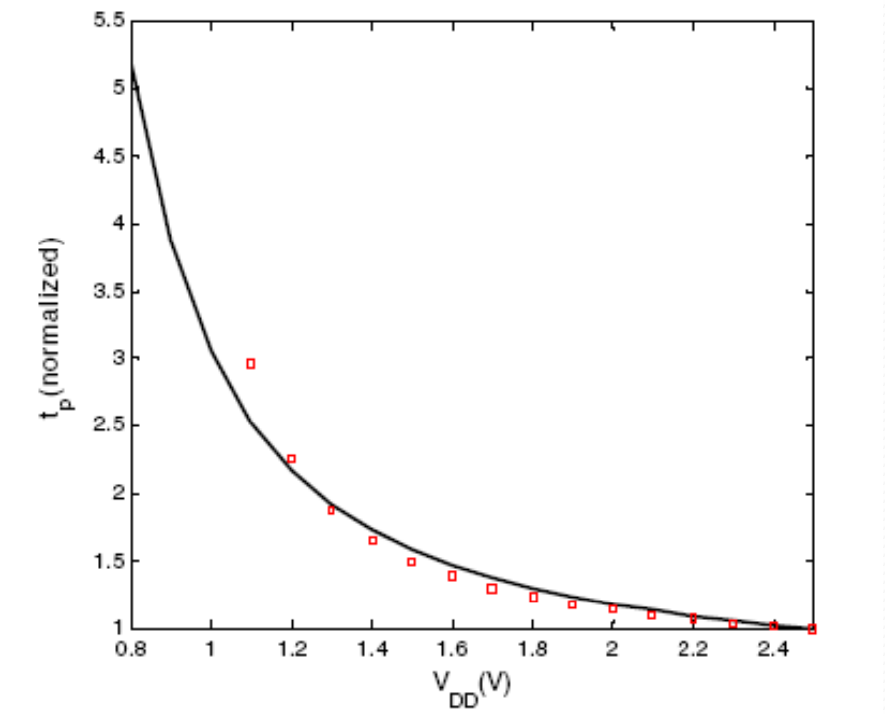
Linear: - VDD + Vthp < Vout < 0

CMOS Inverter Rise Time

- CMOS inverter simmetry $\Rightarrow$ similar approximation can be used to evaluate the rise time

for $V_{THP} = -0.2\, V_{DD}$, $\Rightarrow t_r = 4\, C_L / (\beta_p\, V_{DD})$

Imposing $\beta_n = \beta_p$, or, $\mu_n (W/L)_n = \mu_p (W/L)_p$,
$\Rightarrow t_f = t_r$



Propagation delay of CMOS inverter as a function of supply voltage

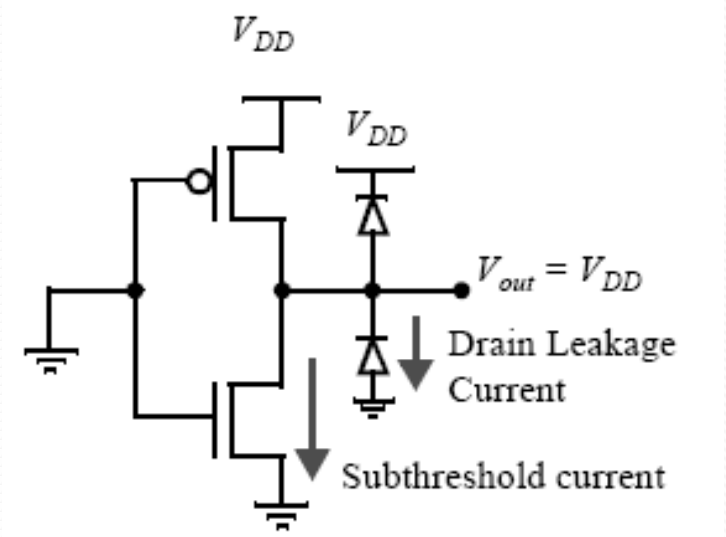
[normalized with respect to the delay at 2.5 V]

Power Consumption

$$P_{total} = P_S + P_D \text{ (static + dynamic)}$$

Static Power Dissipation

- leakage current (Ij) in reversely-biased substrate junctions
- subthreshold current (Ist)

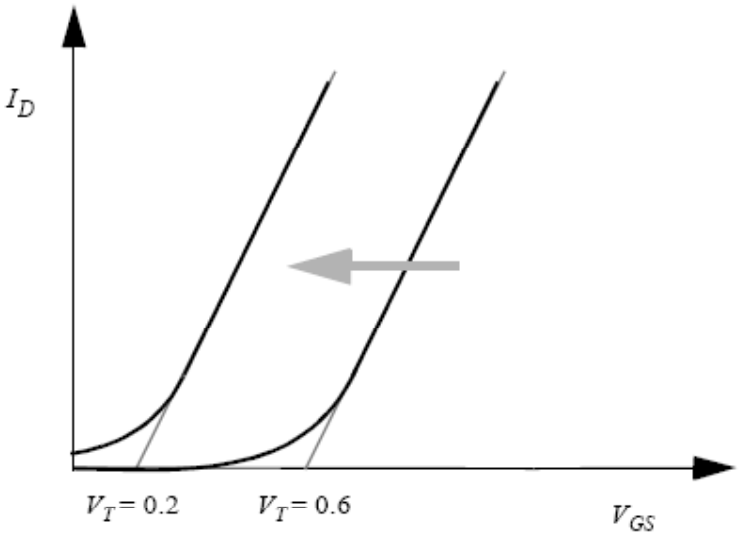


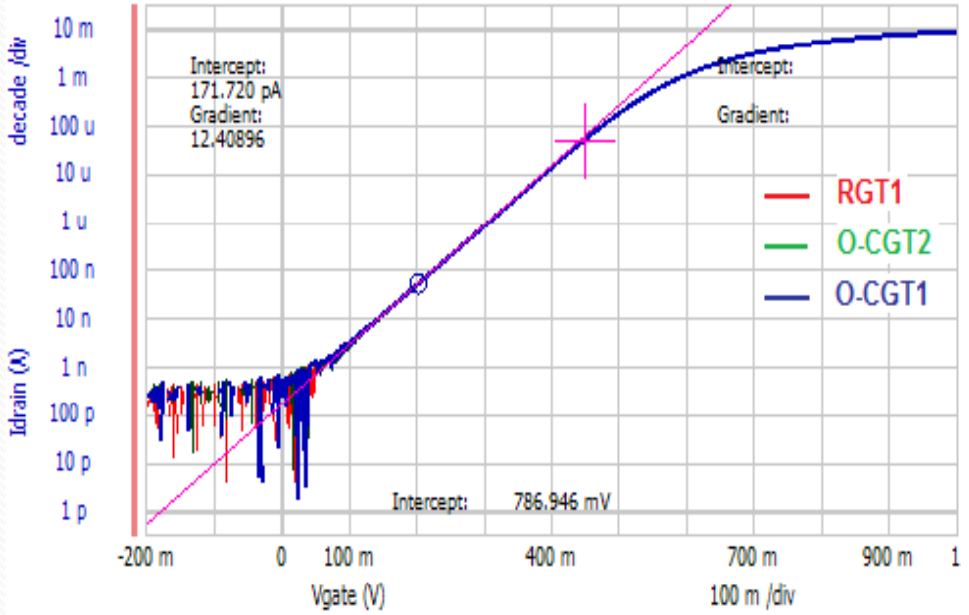
$$P_S = \sum_{1}^{n} (I_j + I_{st})\, V_{DD}$$

- Ij doubles at every 10ºC-variation

Ex: 1nA@25ºC ⇒ 1μA@125ºC

I_{ST} characteristic





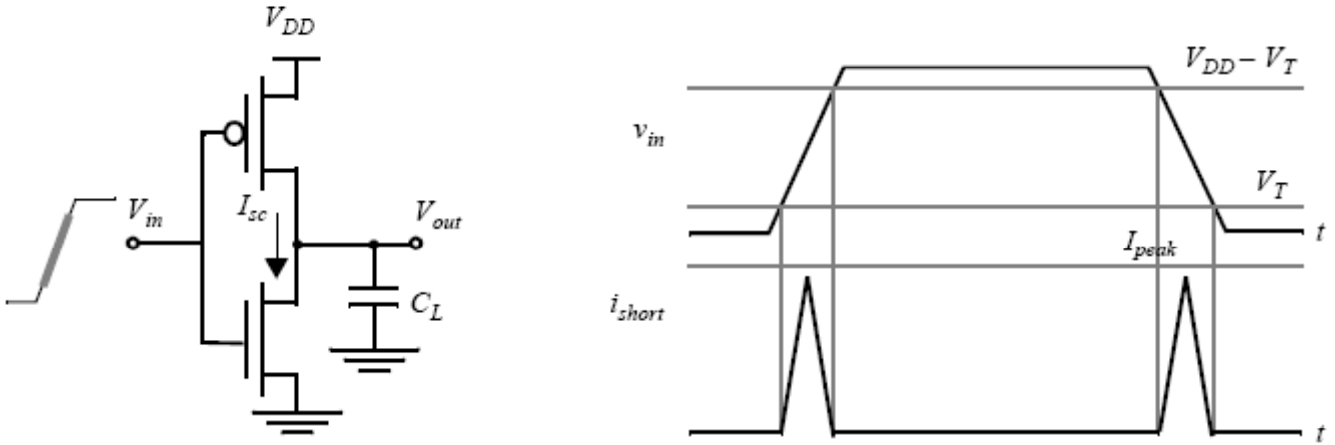
S = 88mV/dec (weak inversion slope)

If $\Delta VTH = 300mV \Rightarrow$ IST is increased by a factor of 2567!!!
$\Delta VTH = 400mV \Rightarrow$ IST is increased by a factor of 35112!!!

Dynamic Power Dissipation

• during transitions 0 → 1 or 1 → 0, both transistors are turned on for a short time

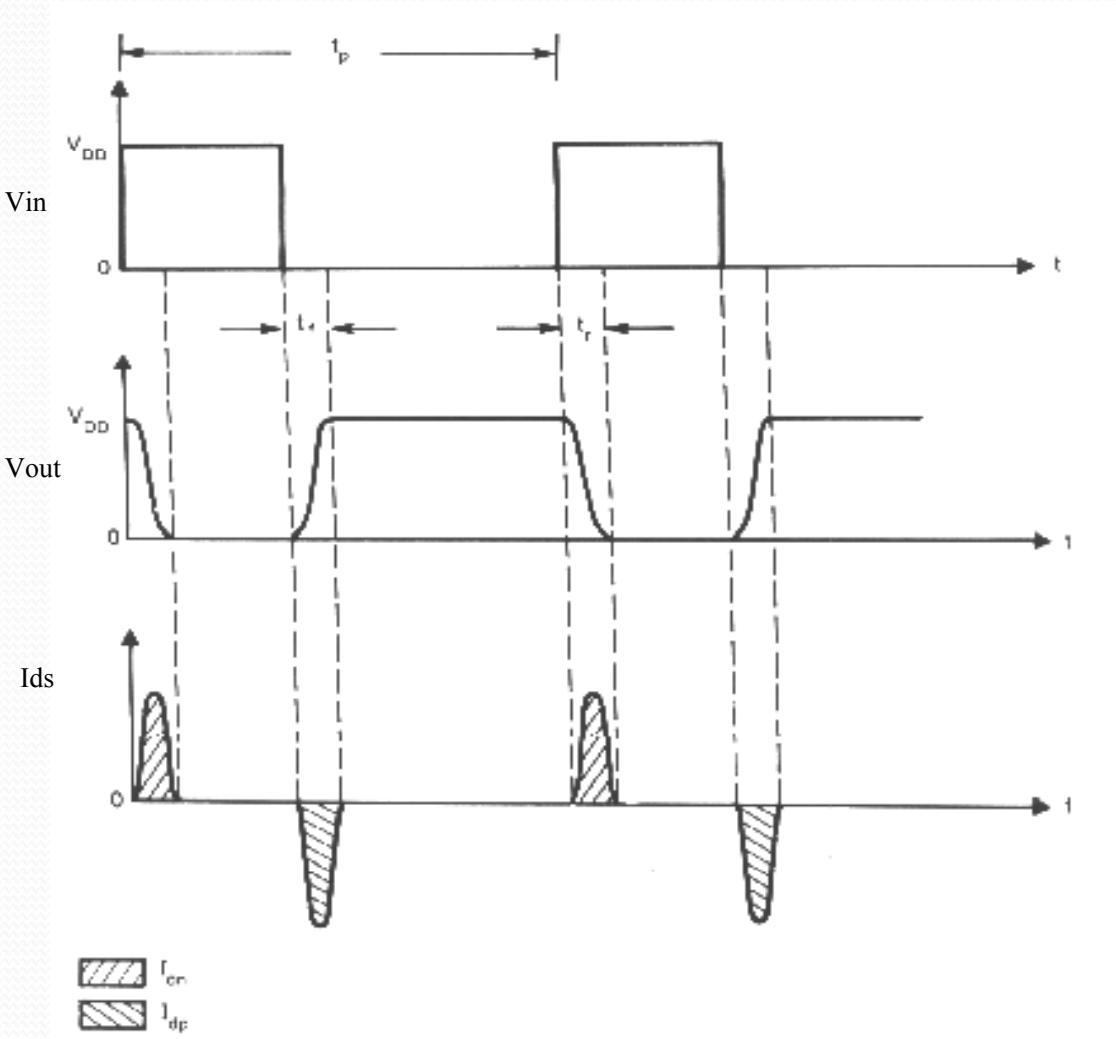
⇒ DC path between V_{DD} e V_{SS} !!!



Short-circuit currents during transients.

$$P_{sc} = t_{cs} I_{peak} V_{DD} f_{sw}$$

$$t_{cs} \cong \frac{t_{r(f)}}{0.8}$$


Vin
Vout
Ids
t_p
V_{DD}
0
t
t_f
t_r
I_{cc}
I_{dp}

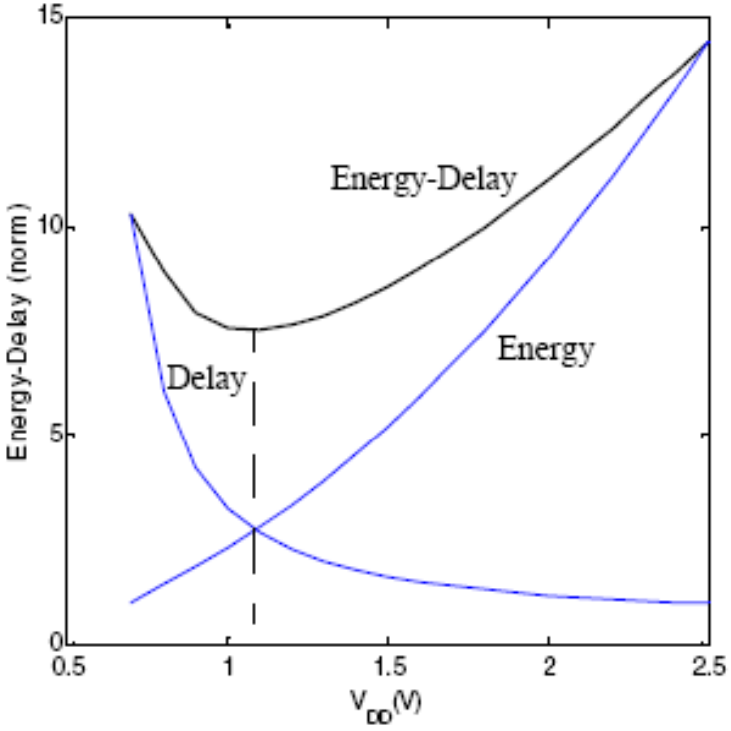
• dynamic power can be estimated by assuming transients much shorts than switching period $T_p = 1/f_p$ of a square wave V_{in}

$$P_D = (1/T_p) \int_0^{T_p/2} I_{DSn}(t)\, V_{out}\, dt + (1/T_p) \int_{T_p/2}^{T_p} I_{DSp}(t)\, (V_{DD} - V_{out})\, dt$$

For a voltage-step at input and $I_{DS}(t) = C_L\, (dV_{out} / dt)$,

$$P_D = (C_L/T_p) \int_0^{V_{DD}} V_{out}\, dV_{out} + (C_L/T_p) \int_{V_{DD}}^{0} (V_{DD} - V_{out})\, dV_{out}$$

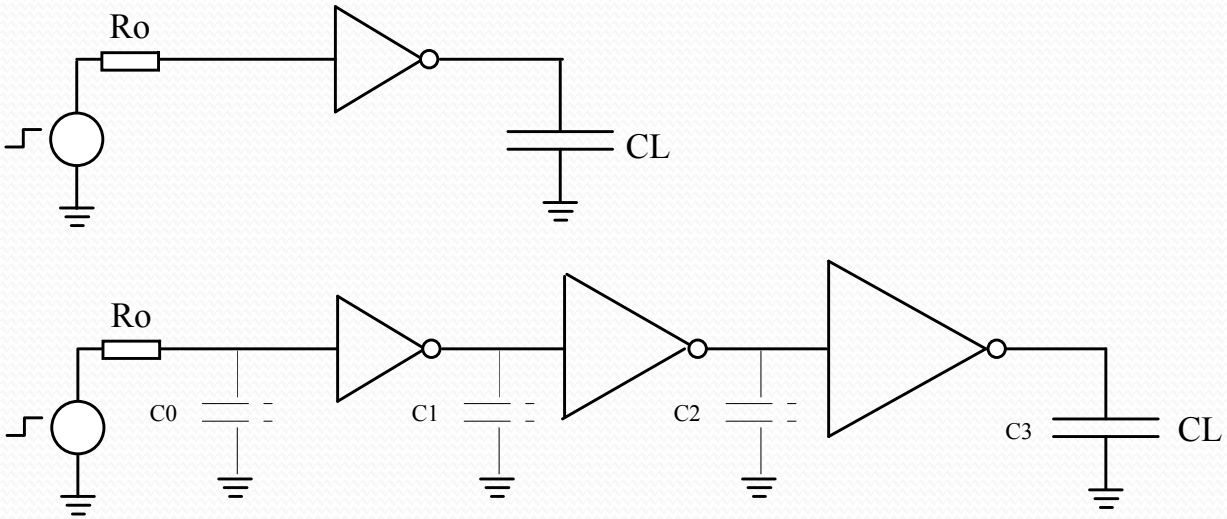
$$\Rightarrow \mathbf{P_D = C_L\, V_{DD}^2\, f_p}$$



Normalized delay, energy,
and energy-delay plots for CMOS inverter in
0.25 μm CMOS technology.

CMOS Buffers

• Whenever an inverter – or logic gate – has a large fan-out, insertion of buffers becomes mandatory to optimize the product *dissipation power x delay time*.



• Let´s consider a *buffer* with M stages, source resistance R_o and load capacitance C_L:

$$T = \sum_{i=0}^{M} R_i C_{i+1} = \tau \sum_{i=0}^{M} \frac{C_{i+1}}{C_i}$$

where T corresponds to total propagation time and $C_{M+1} = C_L$.

• To minimize delay along the chain, one should have $t_i = t_{i+1} = t_0$. Supposing a constant scaling factor *g* between subsequent (W/L),

$$\Rightarrow \quad T = \tau\,(M+1)\,g$$

$$C_L = g^{M+1}\,C_0$$

where $C_0 = \tau / R_0$

$$\Rightarrow T = \tau\,(M+1)\,(C_L / C_0)^{\,1/(M+1)}$$

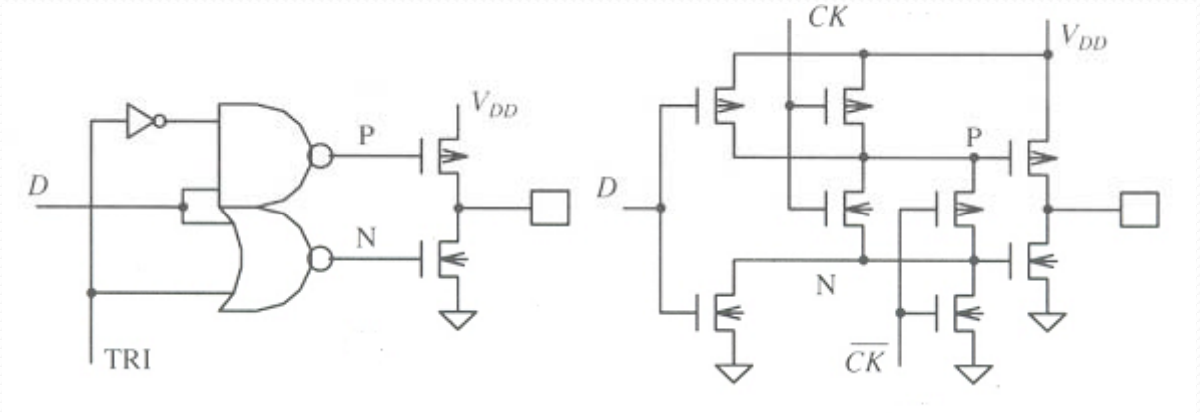
Optimizing with respect to M yields

$$\Rightarrow \mathbf{g = e \cong 2.73}$$

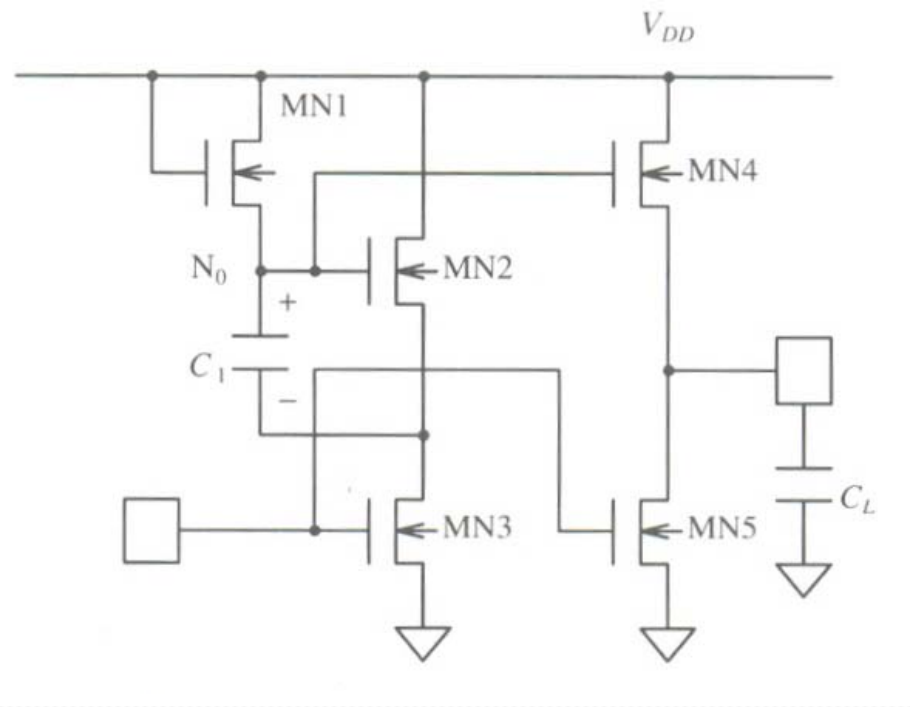
$$\Rightarrow \mathbf{M + 1 = \ln (C_L / C_0)}$$

$$\Rightarrow \mathbf{T = e\tau \ln (C_L / C_0)}$$

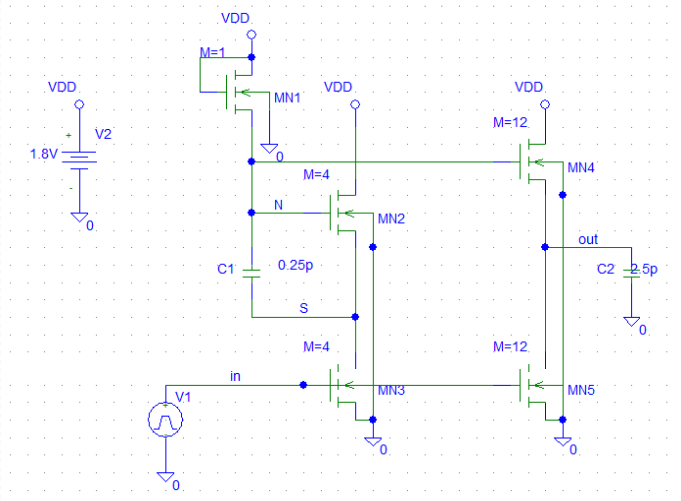
Output Buffers

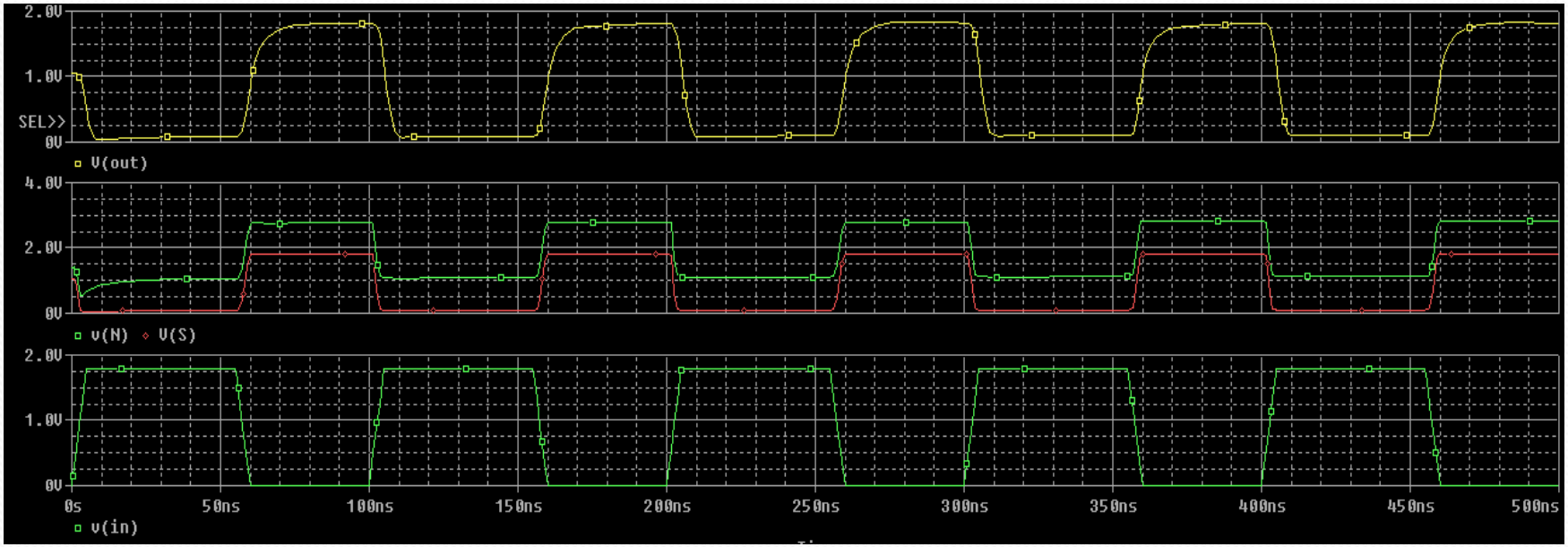


Output Buffers

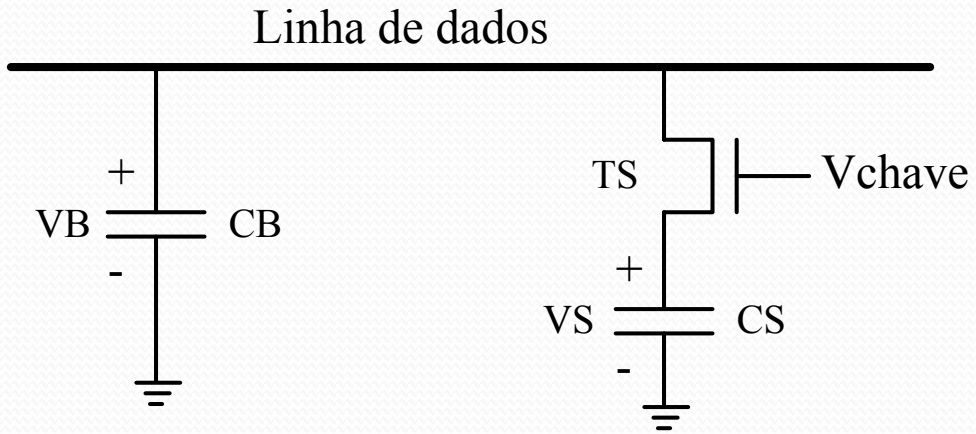


Bootstrapping


VDD
M=1
MN1
VDD
VDD
M=12
MN4
VDD
V2
1.8V
0
M=4
N
MN2
out
C1
0.25p
C2
2.5p
S
M=4
M=12
in
V1
MN3
MN5
0


2.0V
1.0V
SEL>>
0V
V(out)
4.0V
2.0V
0V
V(N)
V(S)
2.0V
1.0V
0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
450ns
500ns
V(in)

Charge Sharing



$$Q_B = C_B V_B \qquad Q_T = C_B V_B + C_S V_S$$

$$Q_S = C_S V_S \qquad C_T = C_B + C_S$$

- when switch Ts turns on, equilibrium voltage is

$$V_{eq} = Q_T / C_T = (C_B V_B + C_S V_S) / (C_B + C_S)$$

$$\Rightarrow \Delta V = V_S - V_{eq} = (V_S - V_B) C_B / (C_B + C_S)$$

$\Rightarrow$ transfer to C_S of data stored in C_B is more efficient as $C_S << C_B$

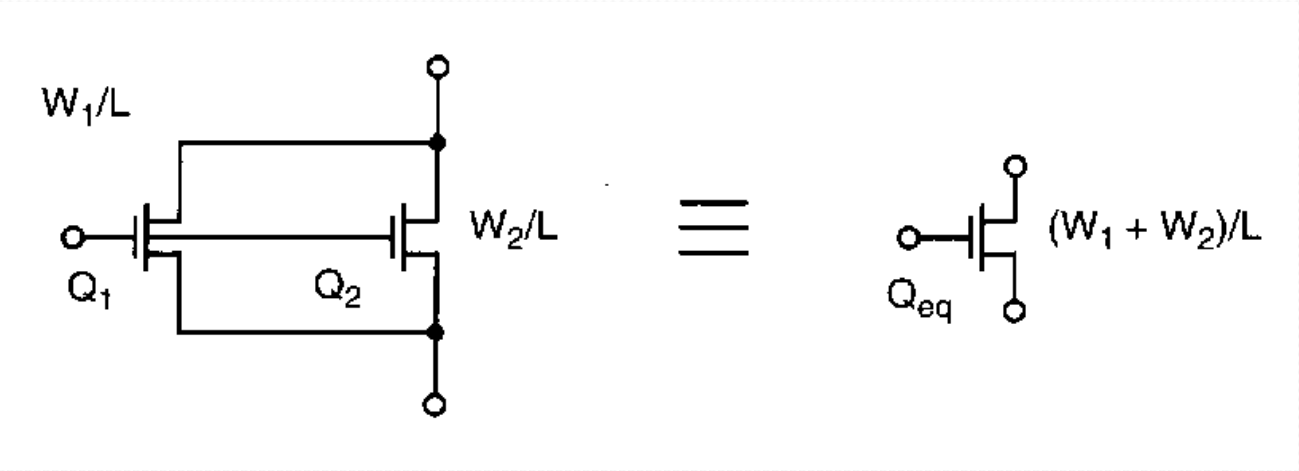
• However, the reverse situation in which data stored in C_S should be transferred to data line, - to capacitor C_B – is much more critical. The voltage change across C_B, after the transfer, is

$$\Delta V = V_B - V_{eq} = (V_B - V_S)\, C_S / (C_B + C_S)$$

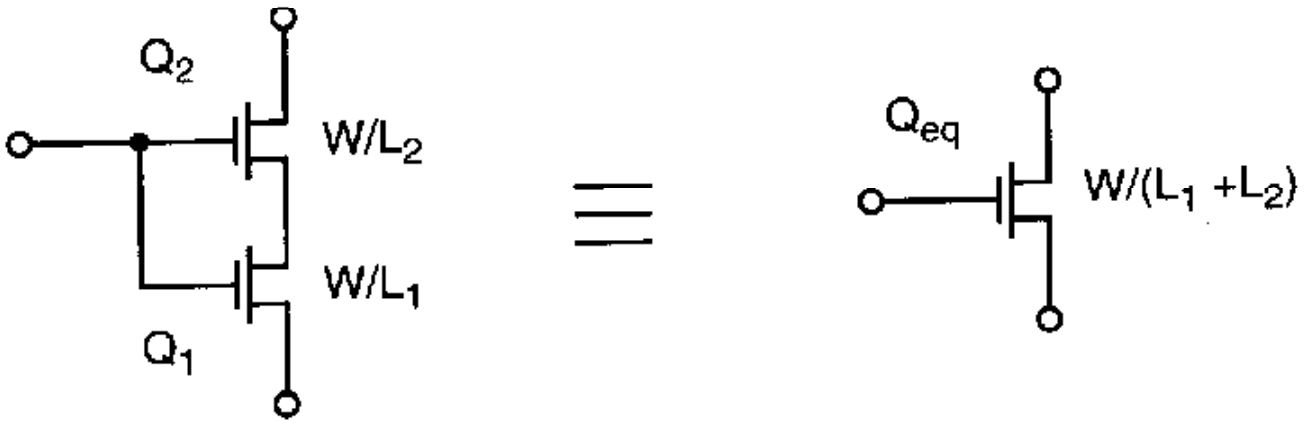
$\Rightarrow$ reduction of original voltage difference $(V_B - V_S)$ by factor $C_S / (C_B + C_S)$, as commonly $C_B >> C_S$

$\Rightarrow$ need for sense amplifiers coupled to data line

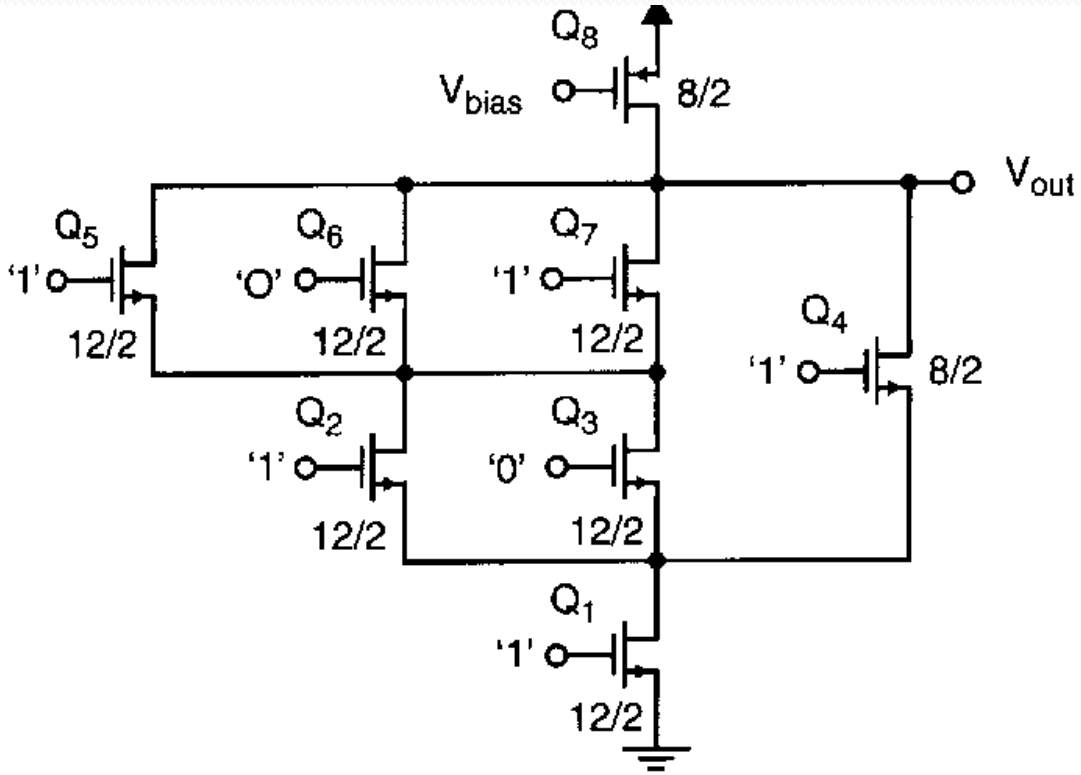
Transistors Equivalence

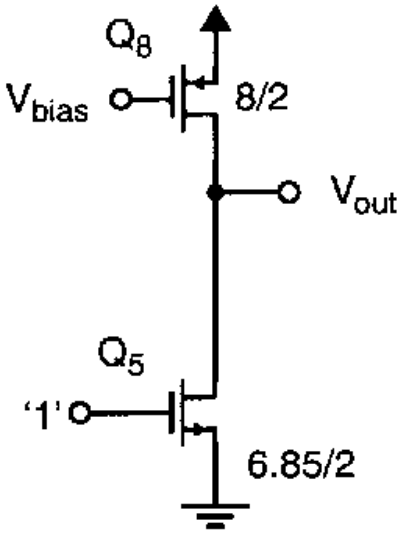


- two transistors of same channel length L in parallel are equivalent to a single transistor of channel width equal to the sum of individual widths.

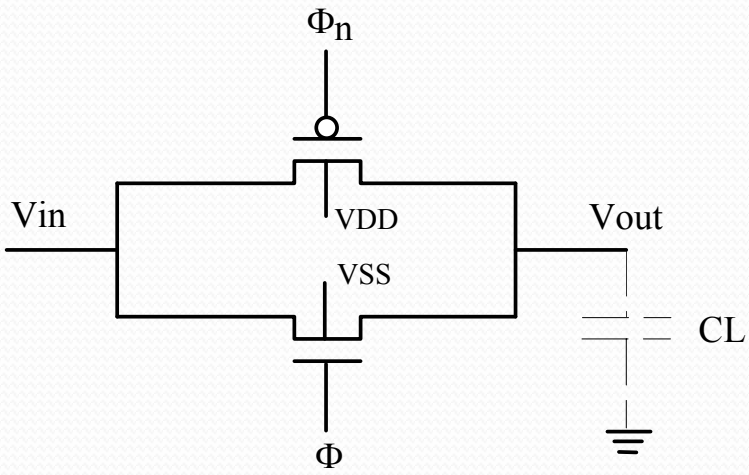


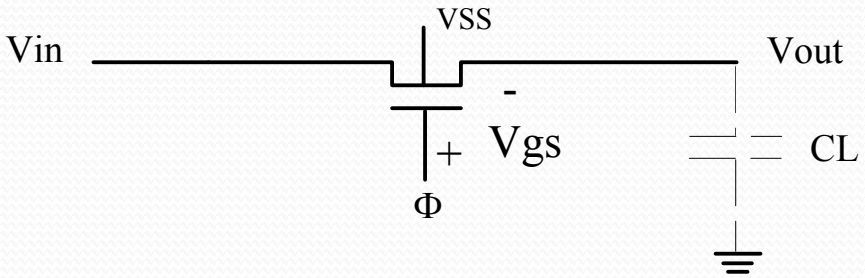
- two transistors of same channel width W in series are equivalent to a single transistor of channel length equal to the sum of individual lengths.


Q8
Vbias
8/2
Vout
Q5
'1'
12/2
Q6
'0'
12/2
Q7
'1'
12/2
Q4
'1'
8/2
Q2
'1'
12/2
Q3
'0'
12/2
Q1
'1'
12/2

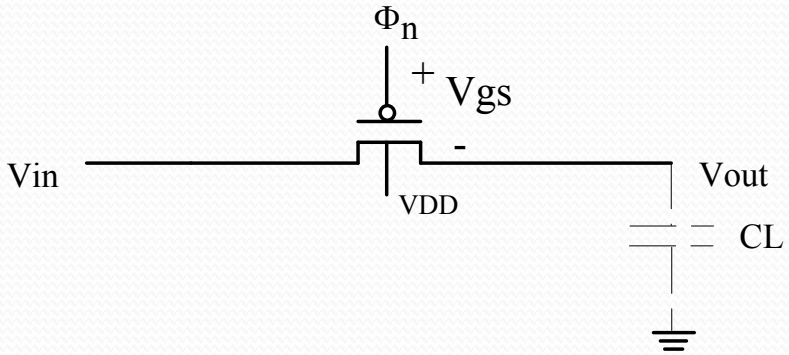

Q8
Vbias
8/2
Vout
Q5
'1'
6.85/2

Transmission Gate

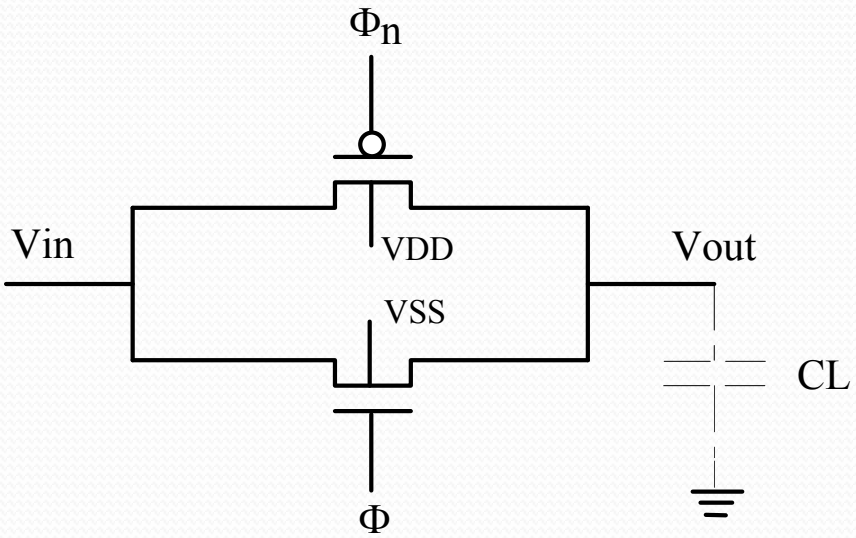




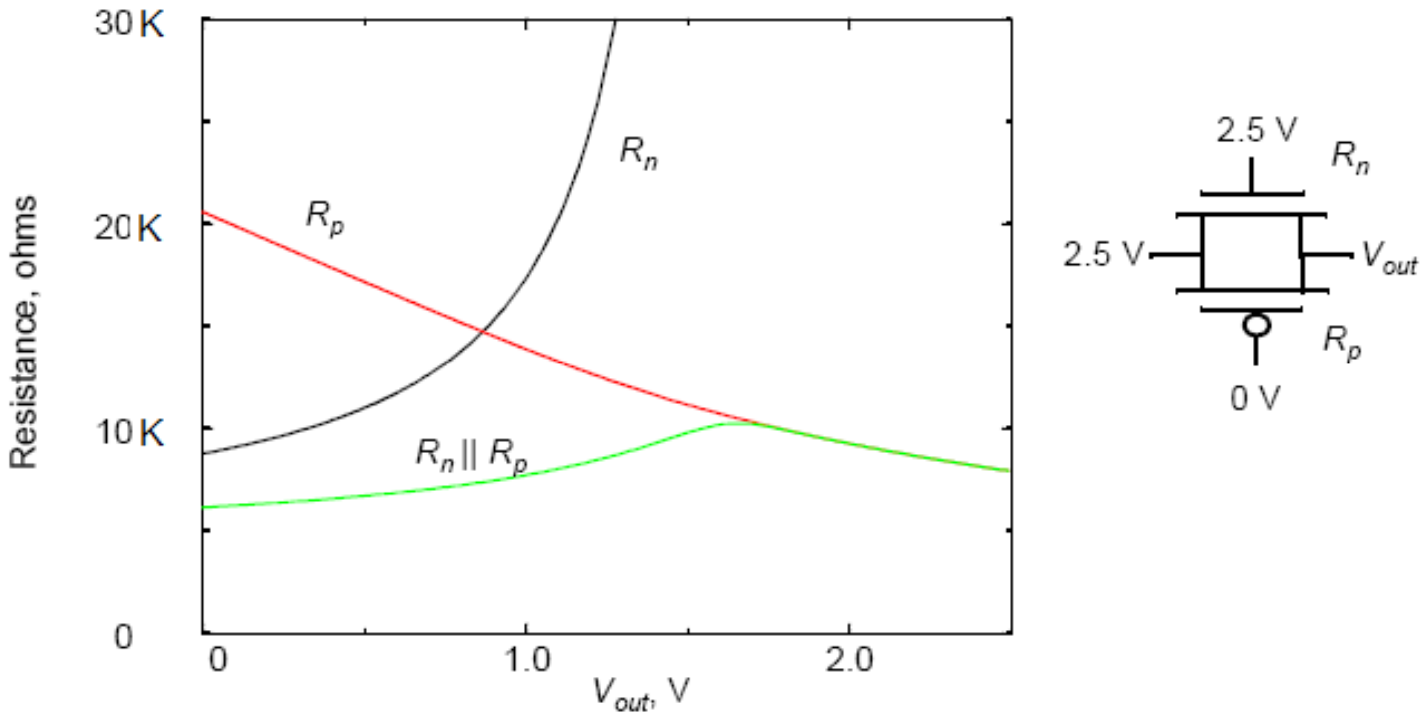
$\Rightarrow$ 0 fully pass; but not 1 ($V_{DD} - V_{THN}$).



$\Rightarrow$ 1 fully pass; but not 0 (GND + $|V_{THP}|$).

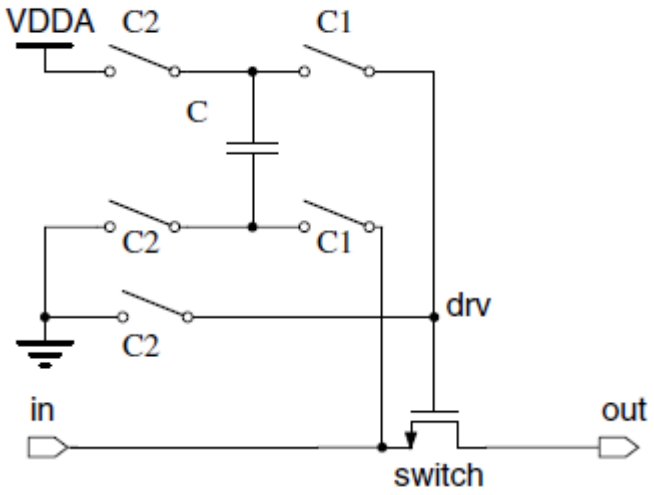


$\Rightarrow$ 0 and 1 fully pass

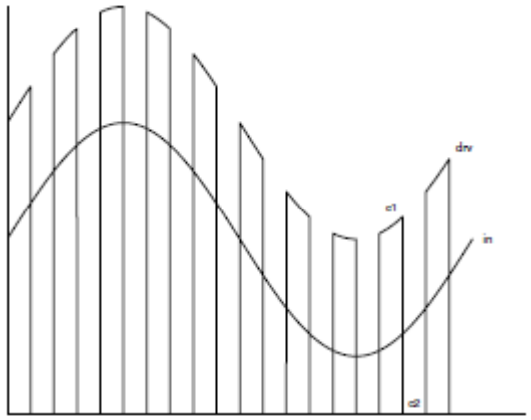


Simulated equivalent resistance of transmission gate (for $(W/L)_n = (W/L)_p = 0.5\mu m/0.25\mu m$).

Clock Boosting Switch

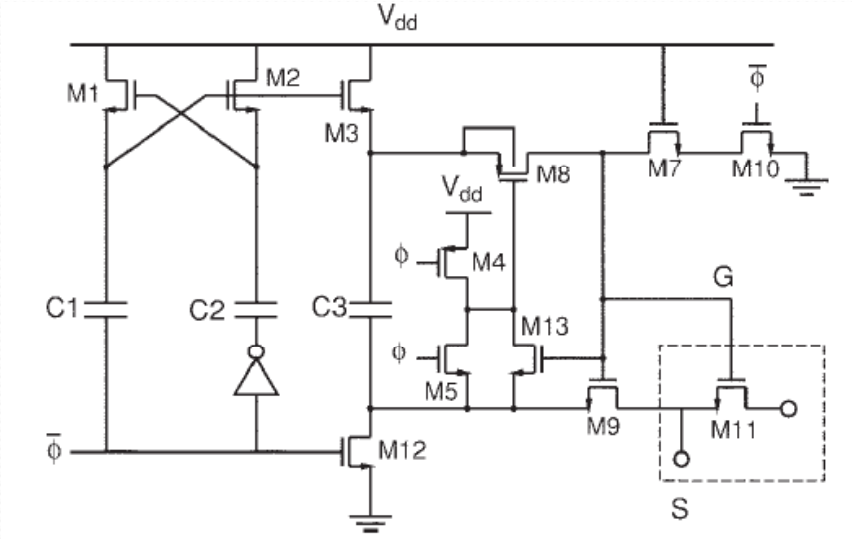


(a) The schematic of the clock boosting circuits.



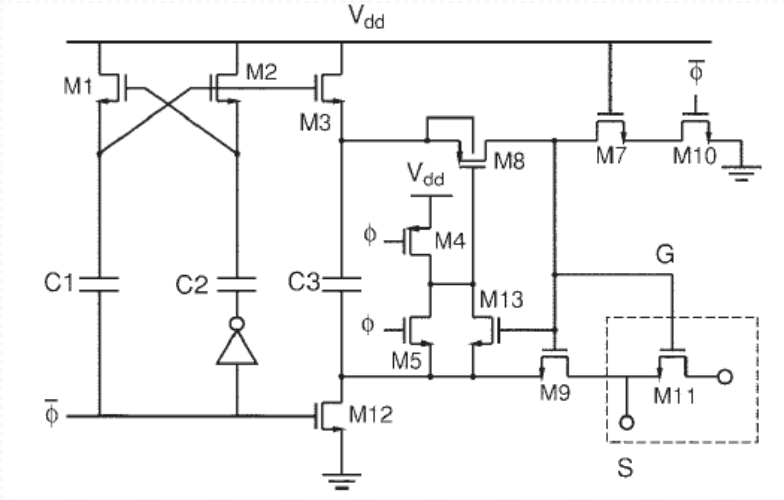
(b) The driving waveform of the switch transistor.

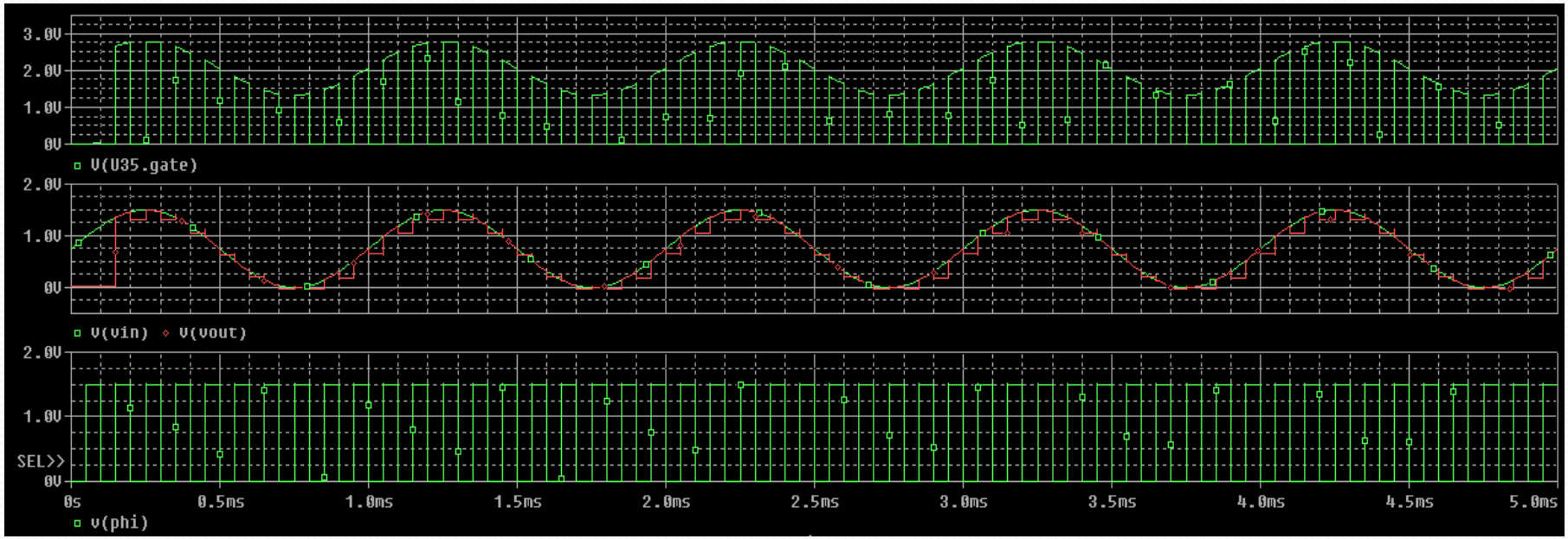
A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, 34(5):599–606, May 1999.

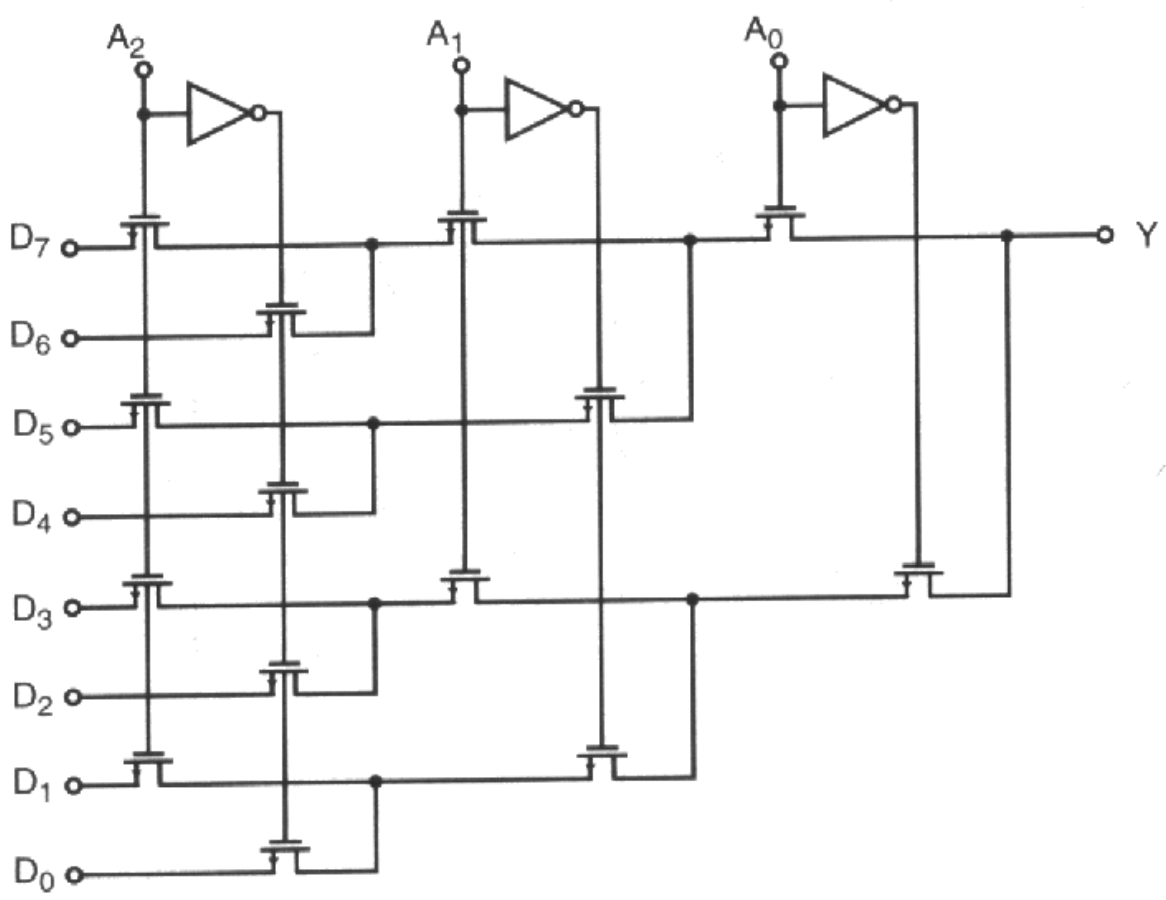


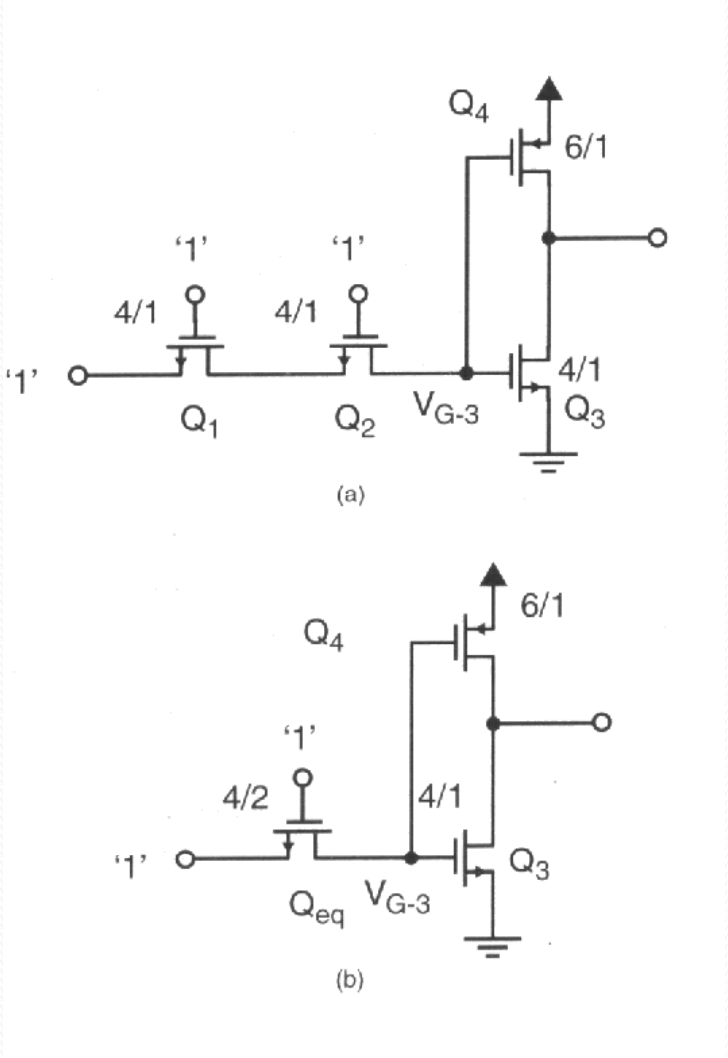
During *off* phase (hold) Φ is low:
⇒M7 and M10 discharge gate of M11 to GND
⇒ VDD is applied across C3 by M3 and M12
⇒ M8 and M9 isolate C3 from gate of M11

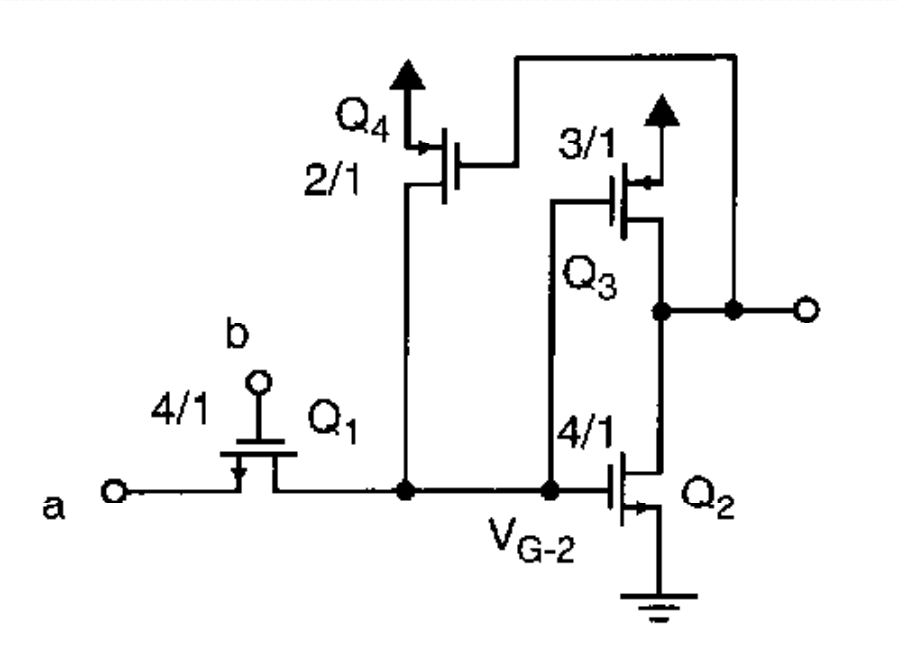
During *on* phase (sample) Φ is high:
⇒ M5 pulls down gate of M8
⇒ C3 charge is transferred onto gate M11
⇒ M9 turns on, so gate G tracks input shifted by VDD


Vdd
M1
M2
M3
M8
M7
M10
Vdd
M4
C1
C2
C3
G
M13
M5
M9
M11
M12
S

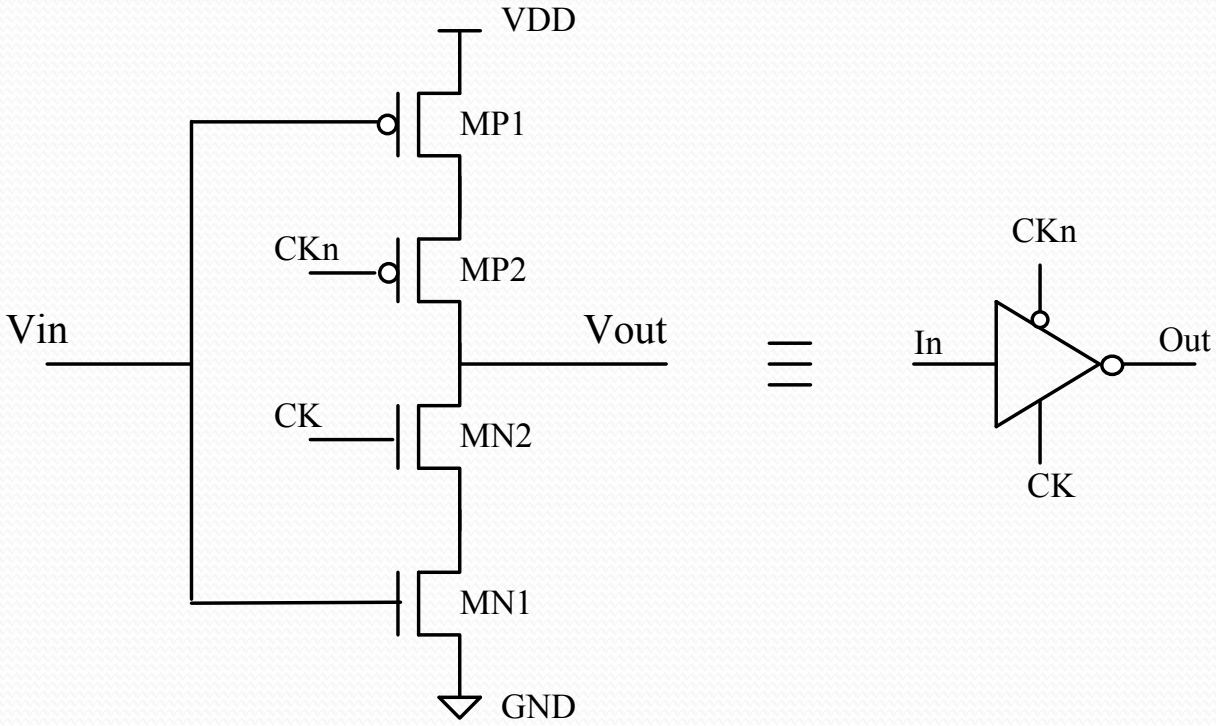

3.0V
2.0V
1.0V
0V
V(U35.gate)
2.0V
1.0V
0V
V(vin) V(vout)
2.0V
1.0V
SEL>>
0V
0s
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms
V(phi)


A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
Y

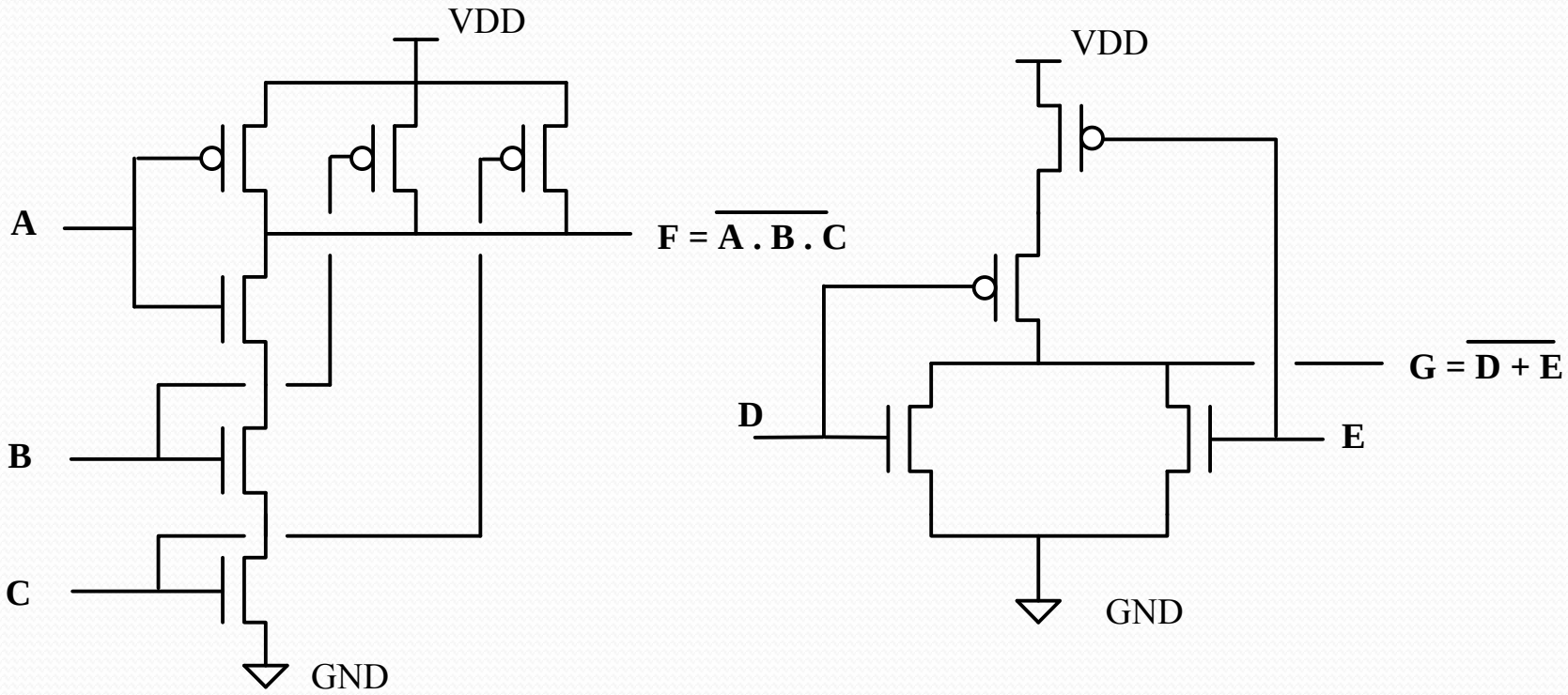

Q4
6/1
'1'
'1'
4/1
4/1
'1'
4/1
Q3
Q1
Q2
VG-3
(a)
6/1
Q4
'1'
4/2
4/1
'1'
Q3
Qeq
VG-3
(b)


Q4
2/1
3/1
Q3
b
4/1
Q1
4/1
a
Q2
VG-2

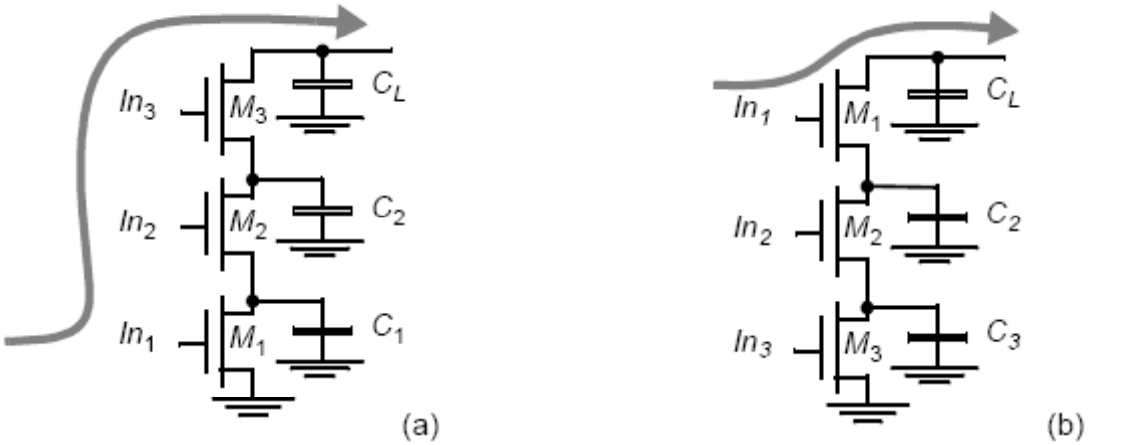
Tristate Inverter



NAND / NOR



Transistor Ordering

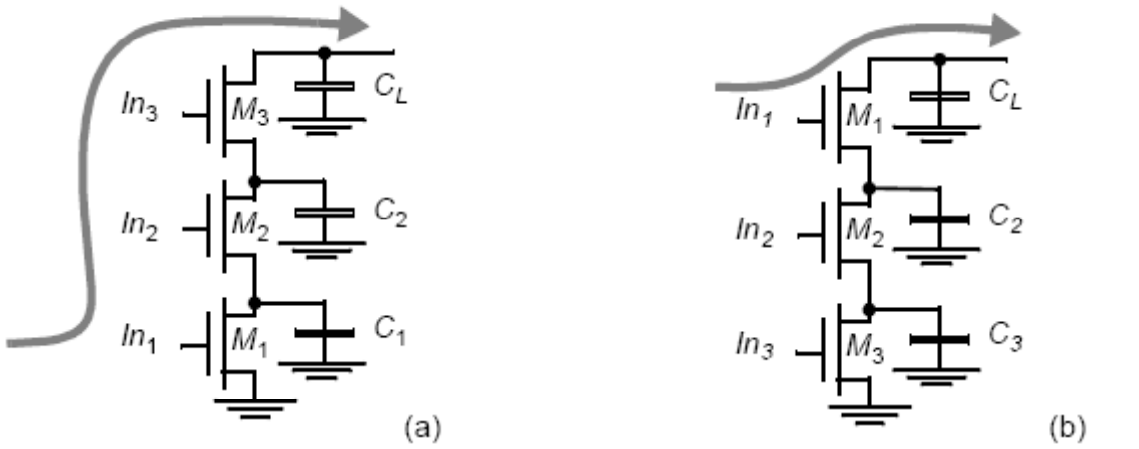


Influence of transistor ordering on delay. Signal In_1 is the critical signal.

Transistor Ordering

BAD

GOOD

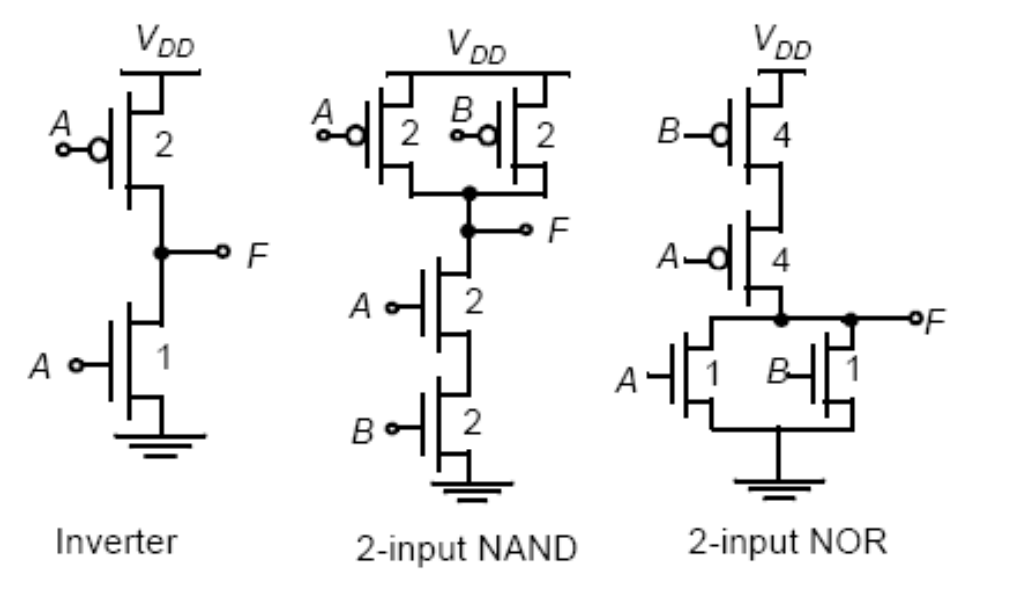


Influence of transistor ordering on delay. Signal In_1 is the critical signal.

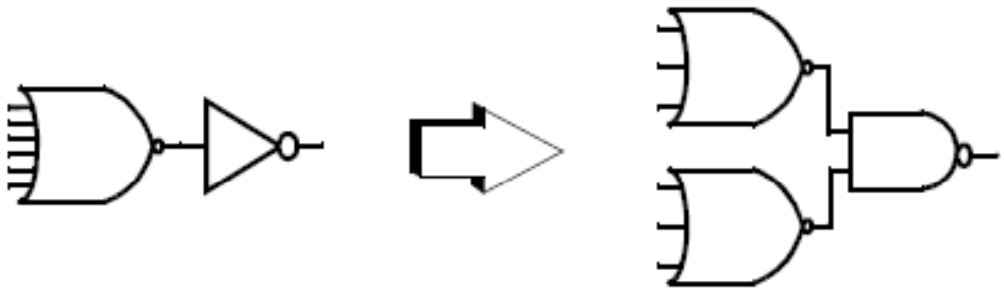
BAD : CL, C2 and C1 only discharged after assertion of IN1

GOOD : C2 and C3 already discharged before assertion of IN1

Fall/Rise Time Simmetry

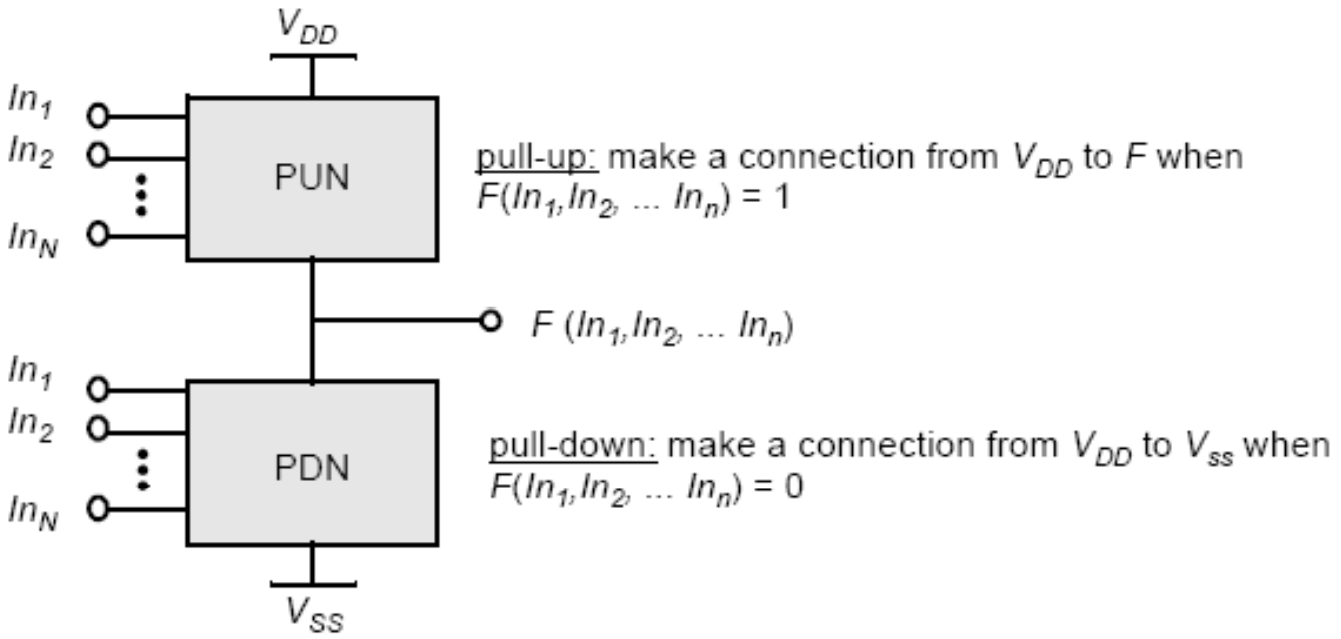


Logic Restructuring



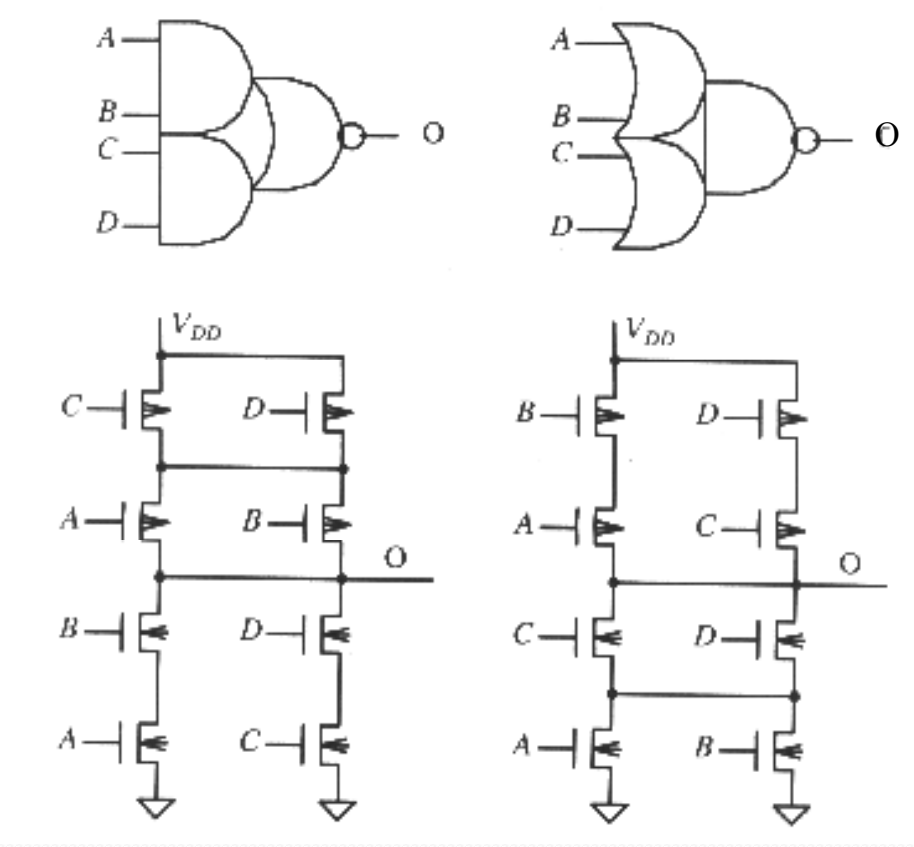
Logic restructuring can reduce the gate fan-in.

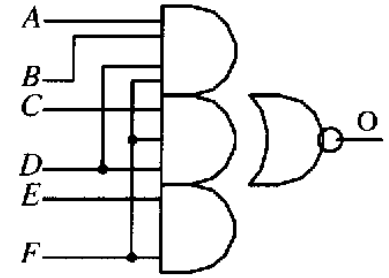
Complex Gates

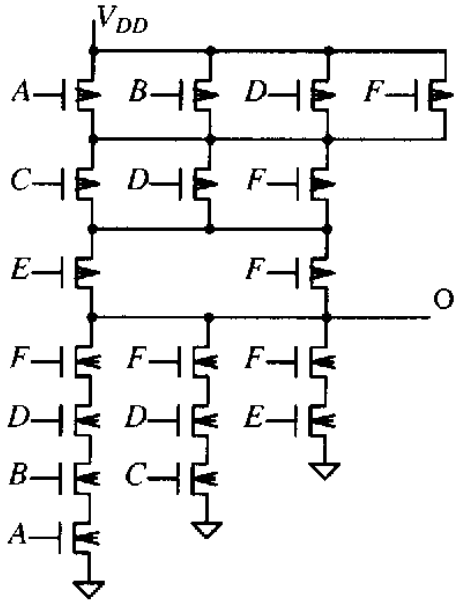


Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network).

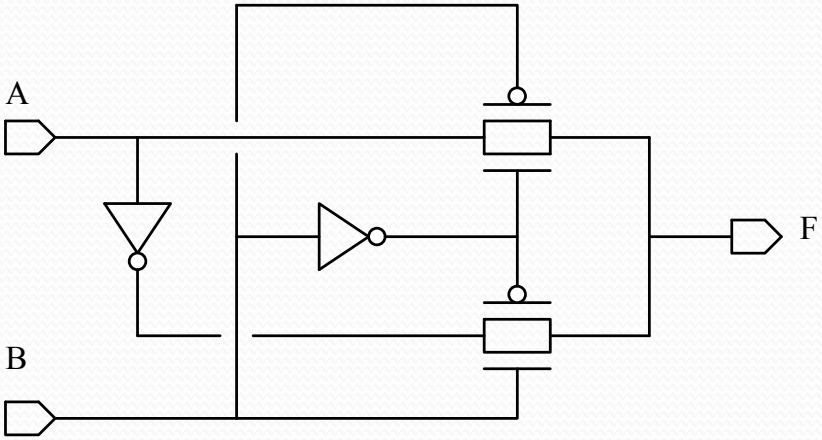
AOI OAI



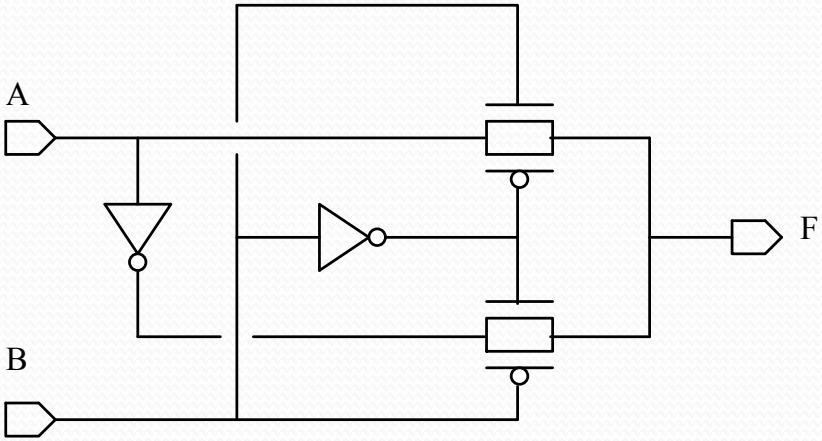

A
B
C
D
E
F
O


V_{DD}
A
B
D
F
C
D
F
E
F
O
F
F
F
D
D
E
B
C
A

XOR / XNOR



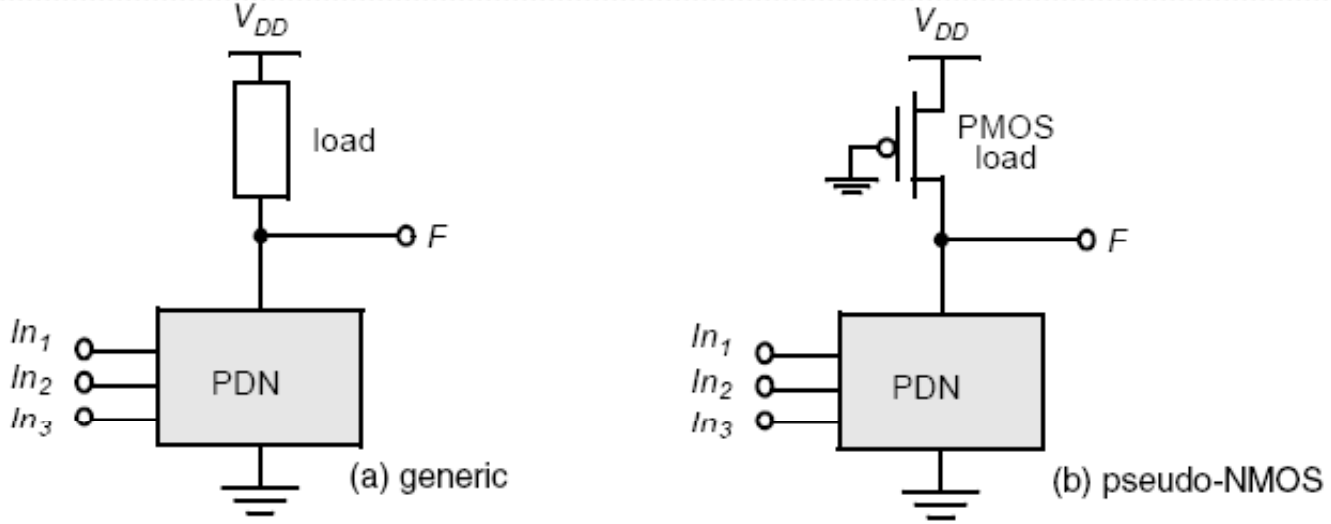
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

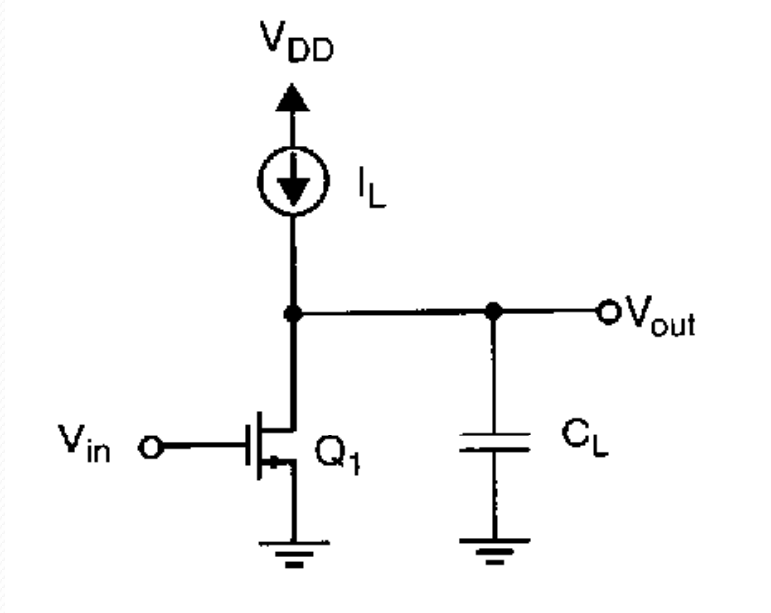
Ratioed Logic

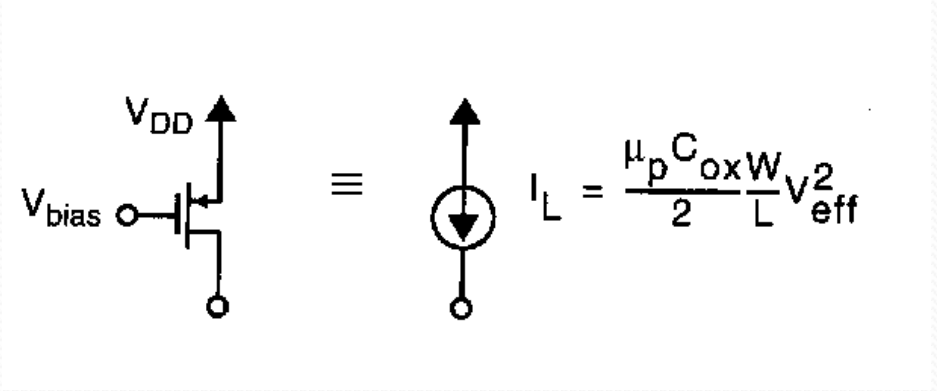
- reduces the number of transistors implementing a logic function (N+1 x 2N for complementary CMOS)
- less robustness and extra power dissipation
- V_{OH} = VDD, but $V_{OL} \neq$ GND (fight between load and PDN)



Ratioed logic gate.

Pseudo-NMOS Logic





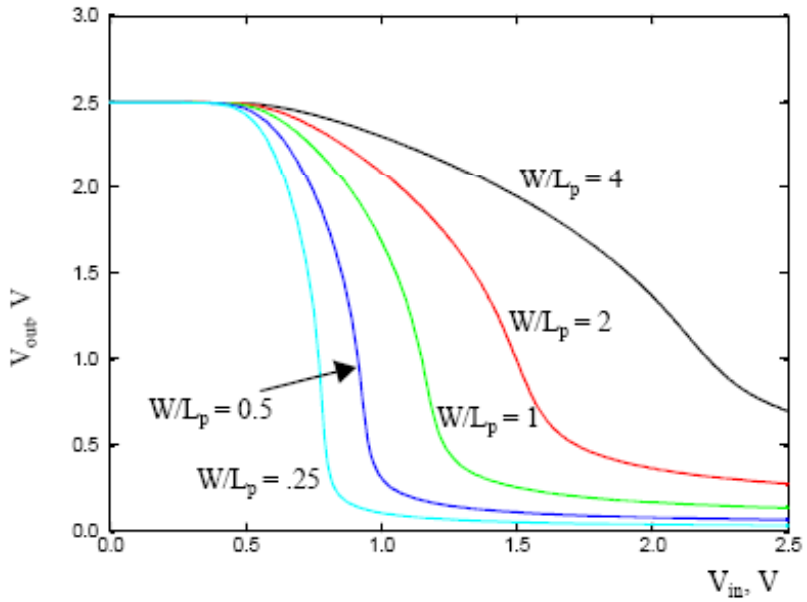
Assuming $V_{TRIP} = V_{DD}/2$

$$I_{D2} = \frac{\beta_p}{2}\left(\frac{VDD}{2} - |V_{THP}|\right)^2$$

$$I_{D1} = \frac{\beta n}{2}\left(V_{TR\ IP} - V_{THN}\right)^2$$

$$V_{TR\ IP} = V_{THN} + \sqrt{\frac{\mu_p (W/L)_2}{\mu_n (W/L)_1}}\left(\frac{VDD}{2} - |V_{THP}|\right)$$

$\Rightarrow$ imposing $V_{TRIP} = V_{DD}/2$, one has $(W/L)_2/(W/L)_1$.

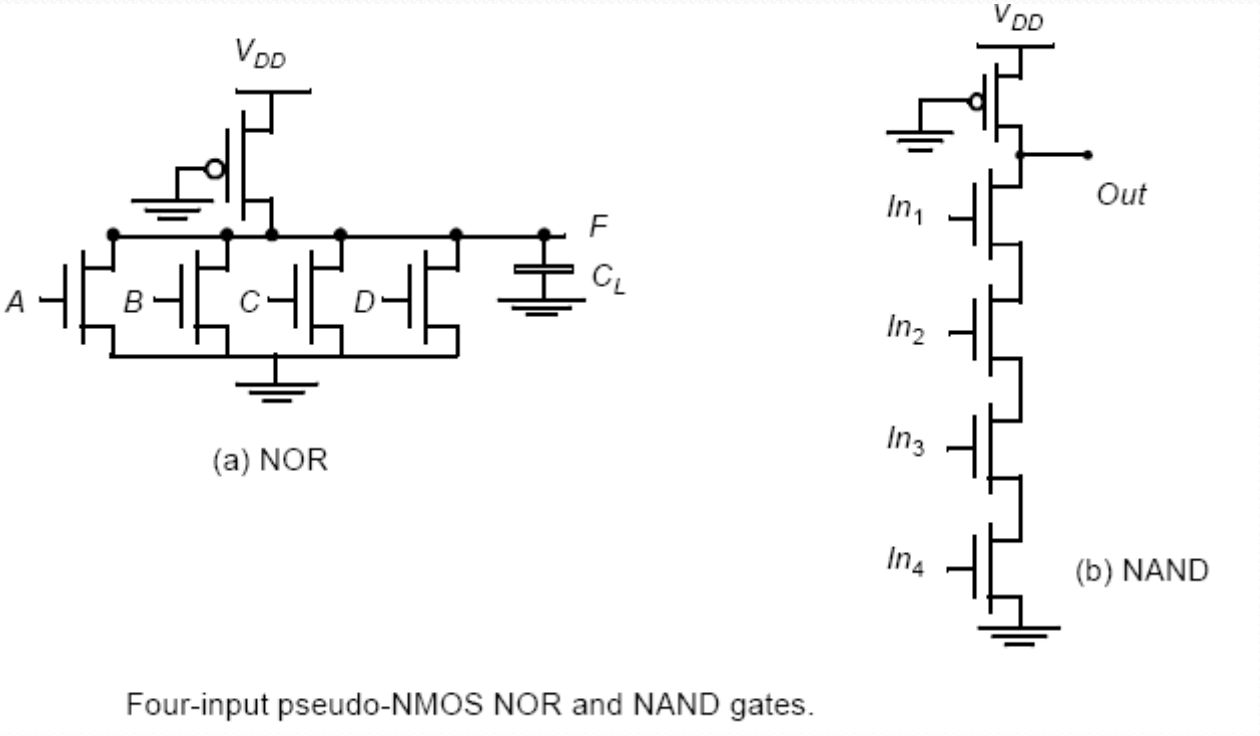


Voltage-transfer curves of the pseudo-NMOS inverter as a function of the PMOS size.

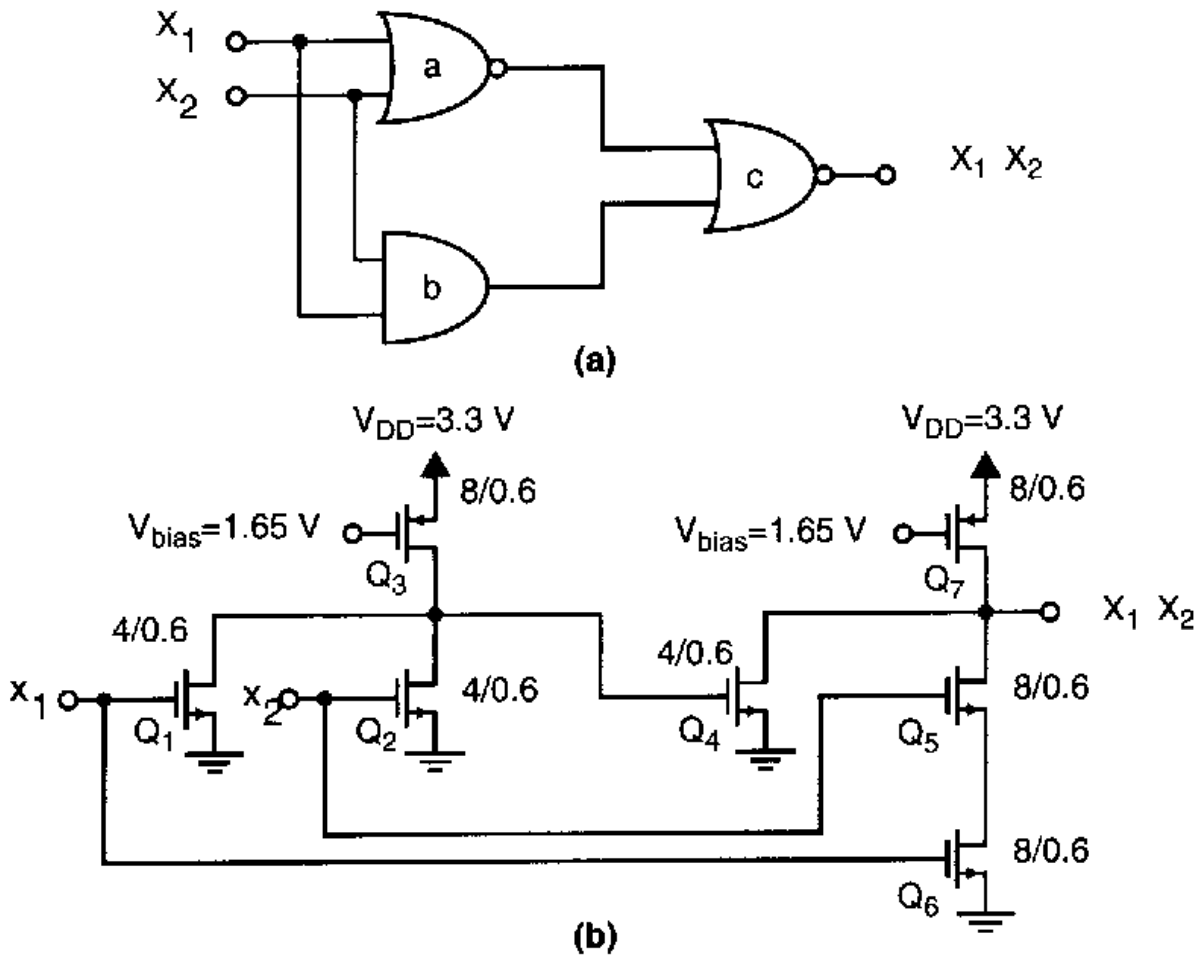
Performance of a pseudo-NMOS inverter.

PMOS (W/L)	V_{OL}	Static Power Dissipation	t_{plh}
4	0.693V	564μW	14ps
2	0.273V	298μW	56ps
1	.133V	160μW	123ps
0.5	0.064V	80μW	268ps
0.25	0.031V	41μW	569ps

- static dissipation limits the use pseudo-NMOS logic
- somewhat useful in large fan-in circuits

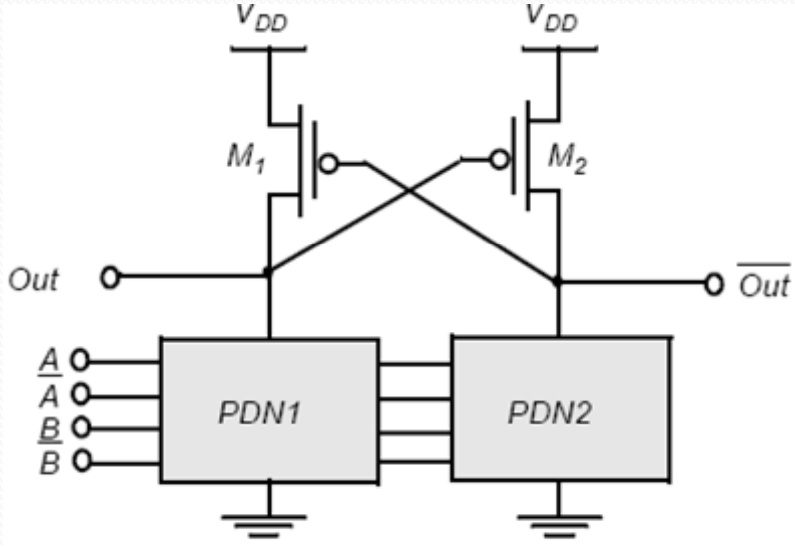


Four-input pseudo-NMOS NOR and NAND gates.


X1
X2
a
b
c
X1 X2
(a)
VDD=3.3 V
VDD=3.3 V
8/0.6
8/0.6
Vbias=1.65 V
Vbias=1.65 V
Q3
Q7
X1 X2
4/0.6
4/0.6
x1
x2
4/0.6
8/0.6
Q1
Q2
Q4
Q5
8/0.6
Q6
(b)

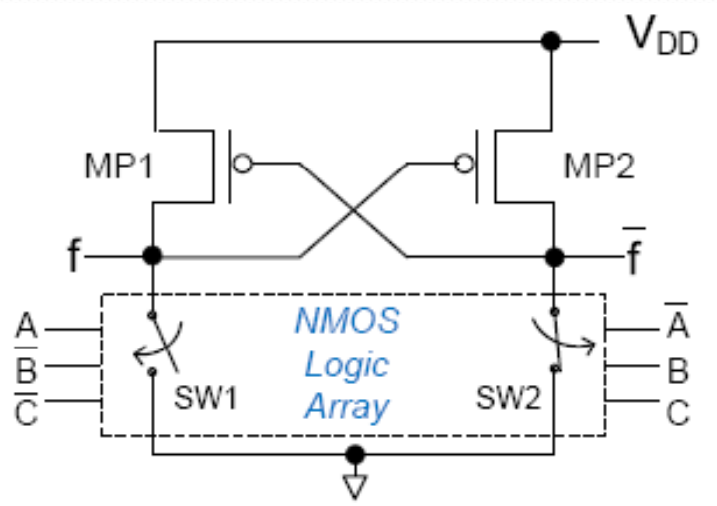
Differential Cascode Voltage Switch Logic (DCVSL)

- ratioed logic with no static dissipation and rail-to-rail swing
- differential logic + positive feedback

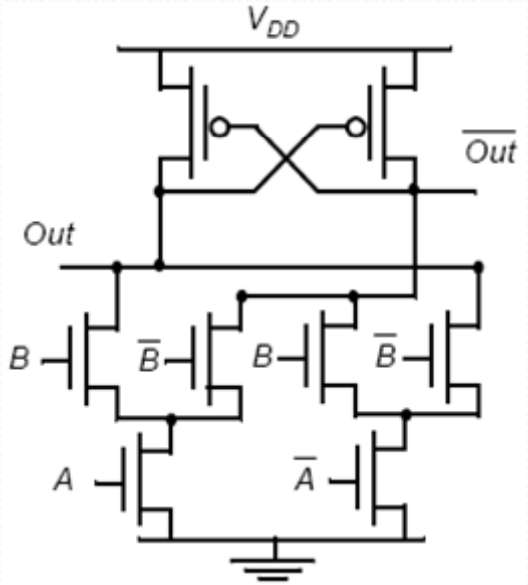


(a) Basic principle

DCVSL logic gate.



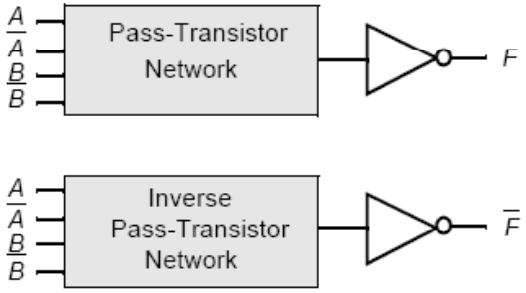
- PDN1 and PDN2: mutually exclusive. PDN1 (on), PDN (off). and vice-versa



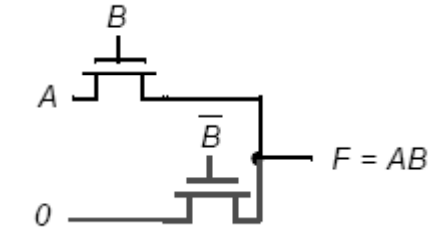
(b) XOR-XNOR gate

Complementary pass-transistor logic (CPL)

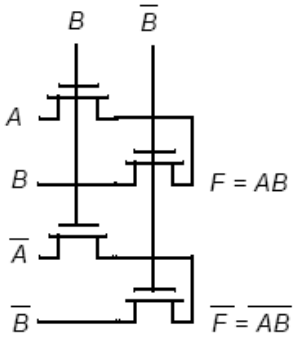
- inputs drive gate terminals as well as source/drain terminals
- fewer transistors



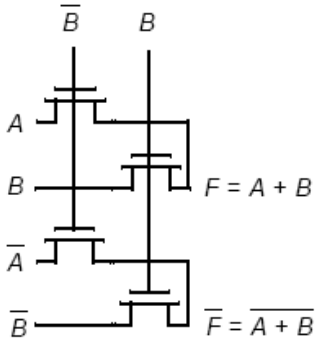
(a) Basic concept



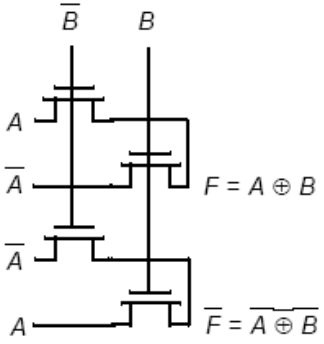
Pass-transistor implementation of an AND gate.



AND/NAND

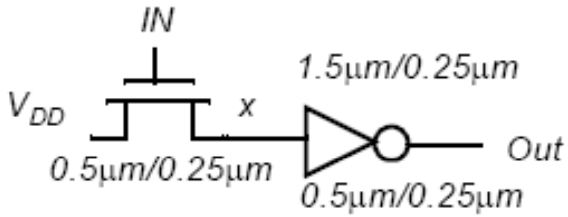


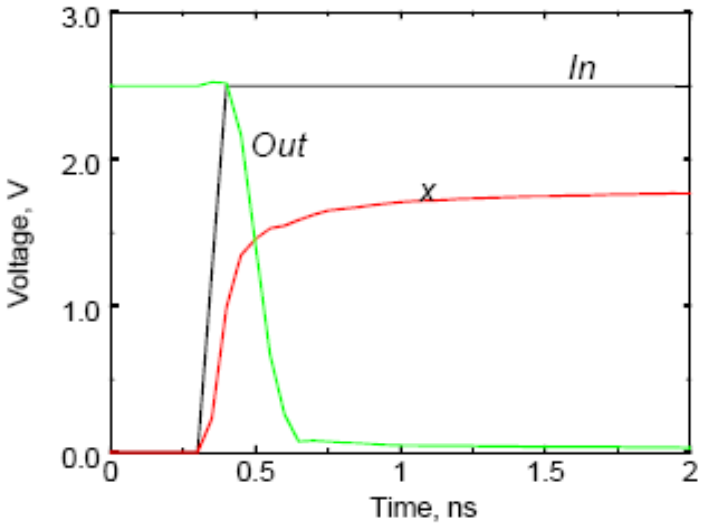
OR/NOR



XOR/NXOR

- NMOS device is effective at passing a 0, but poor at pulling a node to *VDD*
- *VOH = VDD – VTH (VBS)*

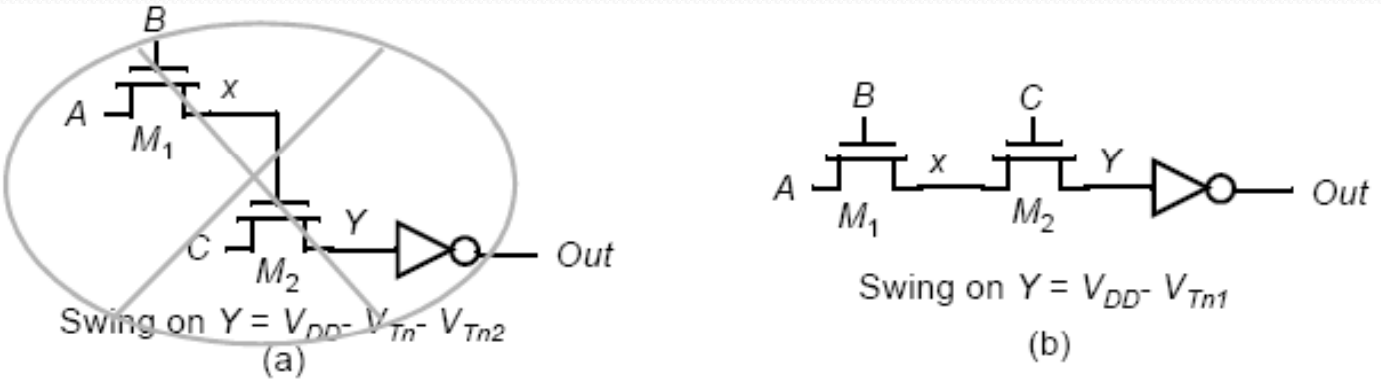




Transient response of charging up a node using an *N* device. Notice the slow tail after an initial quick response.

$$V_x = V_{DD} - (V_{tn0} + \gamma((\sqrt{|2\phi_f| + V_x}) - \sqrt{|2\phi_f|}))$$

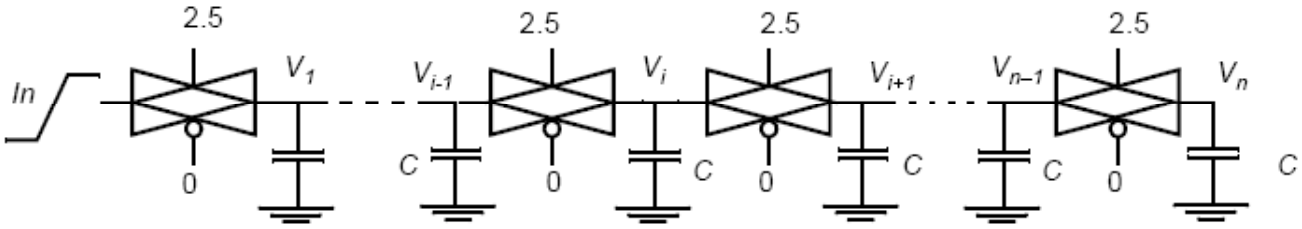
• pass-transistor gates **cannot** be cascaded by connecting the output of a pass gate to the gate input of another pass transistor



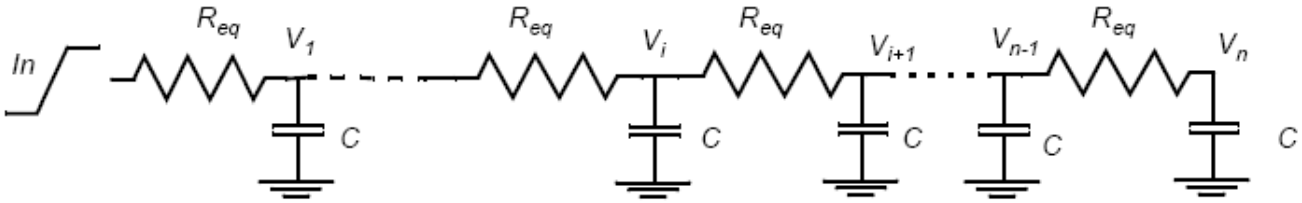
Pass transistor output (Drain/Source) terminal should not drive other gate terminals to avoid multiple threshold drops

Performance of Pass-Transistor and Transmission Gate Logic

- pass-transistor is not an ideal switch: series resistance.



(a) A chain of transmission gates

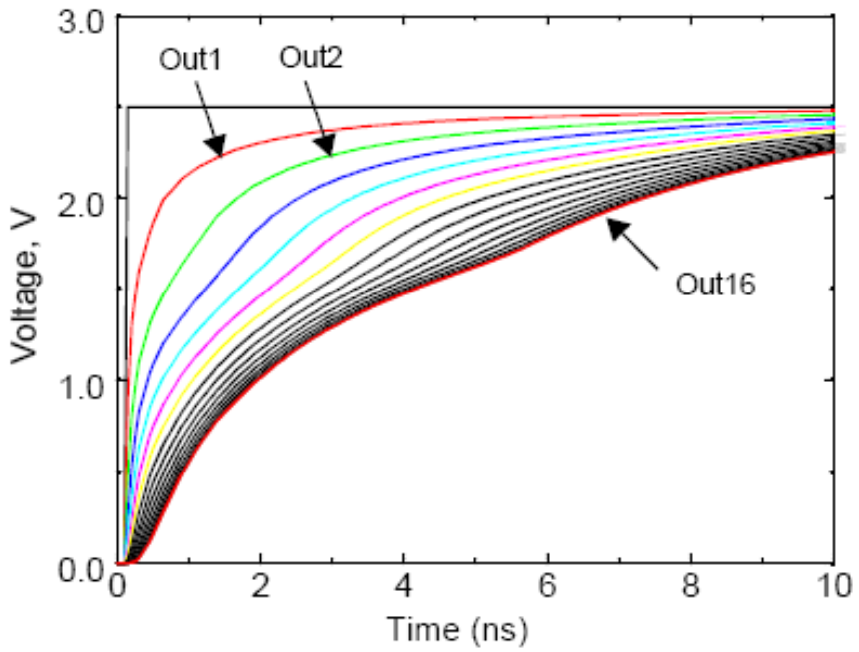


(b) Equivalent *RC* network

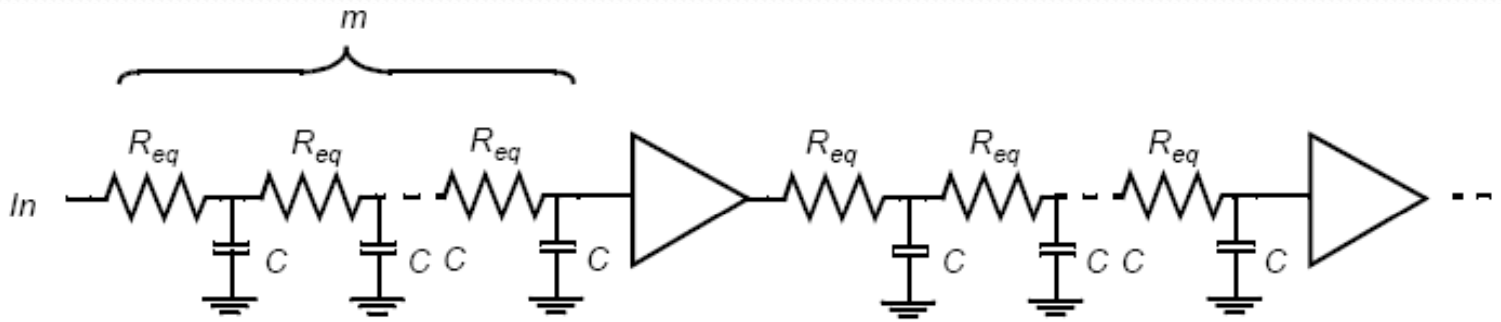
$$t_p(V_n) = 0.69 \sum_{k=0}^{n} CR_{eq}k = 0.69 CR_{eq} \frac{n(n+1)}{2} \Rightarrow$$

propagation delay is proportional to n^2

$$t_p = 0.69 \cdot CR_{eq}\frac{n(n+1)}{2} = 0.69 \cdot (3.6fF)(8K\Omega)\left(\frac{16(16+1)}{2}\right) \approx 2.7ns$$



Transient response of 16 transmission gates cascaded in series.



Breaking up long transmission gate chains by inserting buffers.

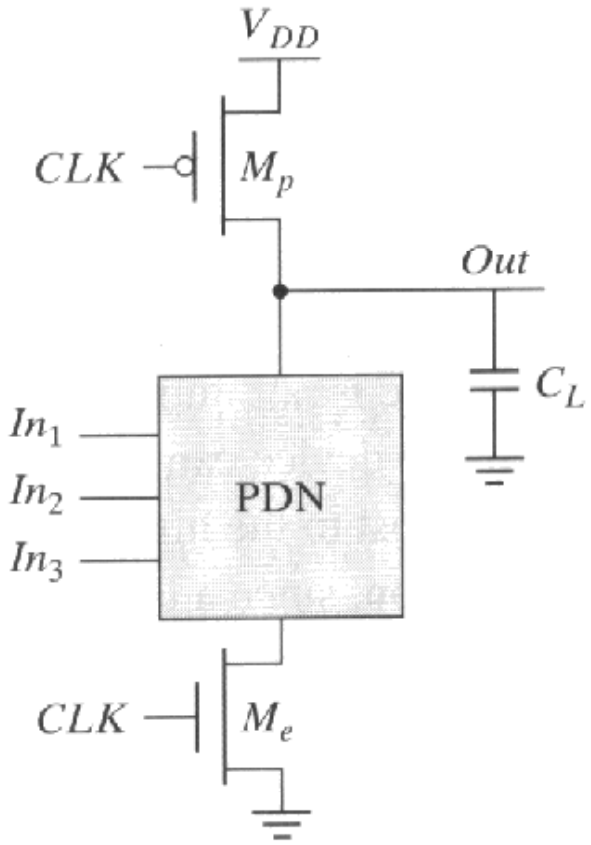
$m_{opt} \cong 3$

Lógica CMOS Dinâmica

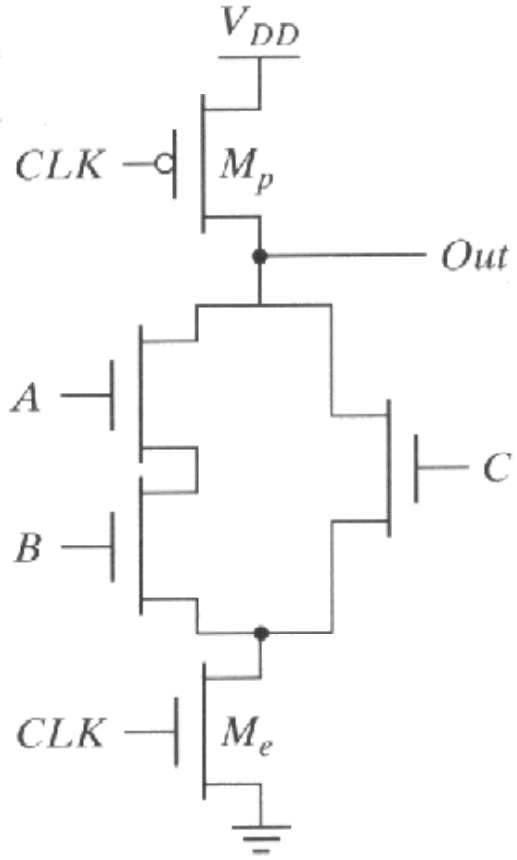
- A lógica estática CMOS requer 2N transistores para N entradas
- Diferentes técnicas de projeto, como pseudo-NMOS, lógica a transistor de passagem (*transmission-gate logic*),

- excelente alternativa é a lógica dinâmica, a qual apresenta resultados semelhantes à lógica pseudo-NMOS, mas sem a consumação estática

• CondiCionada a um clock, a operação desta lógica compreende duas fases: pré-carga (*precharge*) e avaliação (*evaluation*).



(a) *n*-type network



(b) Example

•. Durante a pré-carga (CLK = 0)

- C_L pré-carregada a V_{DD} pelo transistor M_p
- M_e está cortado, o que impede a descarga de C_L

$\Rightarrow$ nenhuma dissipação estática ocorre

• Durante a avaliação (CLK=1)

- a saída condicionalmente descarregada
- se PDN on, haverá um caminho entre a saída e GND
- se PDN off, a saída não será descarregada, mantendo-se a V_{DD}

$\Rightarrow$ uma única transição à saída é possível: 1 $\Rightarrow$ 0

• Caso PDN off, a saída permanece em alta impedância durante a avaliação

- Principais propriedades

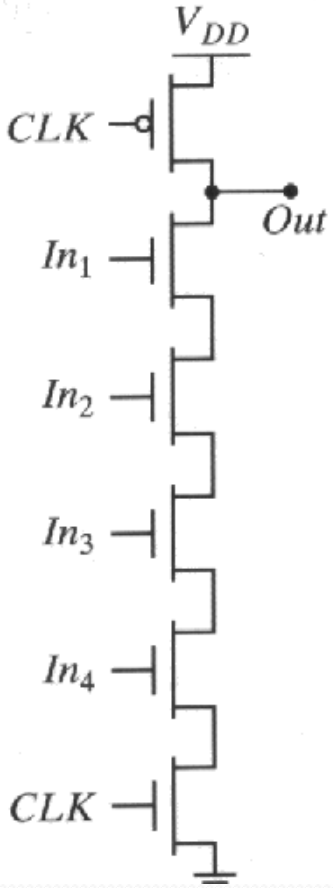
• A função lógica é implementada pelo circuito PDN utilizando NMOS.

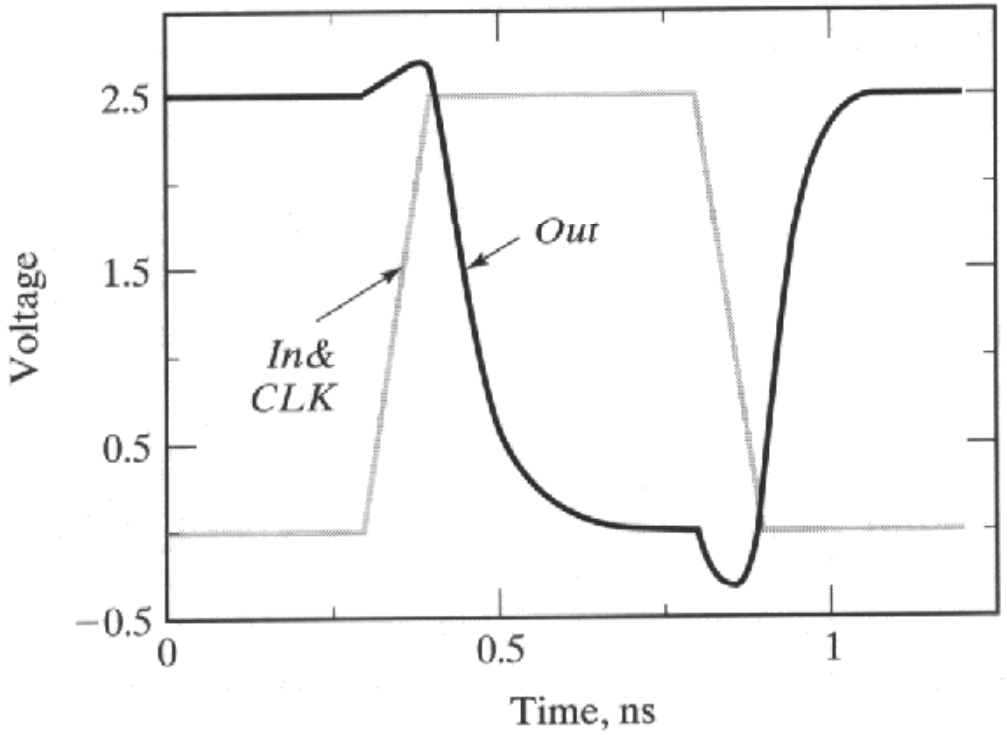
• N° transistores = N + 2 (contra 2N na lógica CMOS estática)

• Não há necessidade de razão entre (W/L)'s (*nonratioed*).

• Apenas dissipa potência dinâmica

• Transições mais rápidas podem ocorrer pela diminuição do número de transistores, e conseqüentemente, das capacitâncias envolvidas.


V_{DD}
CLK
Out
In_1
In_2
In_3
In_4
CLK


2.5
1.5
0.5
−0.5
0
0.5
1
Voltage
Time, ns
Out
In&
CLK

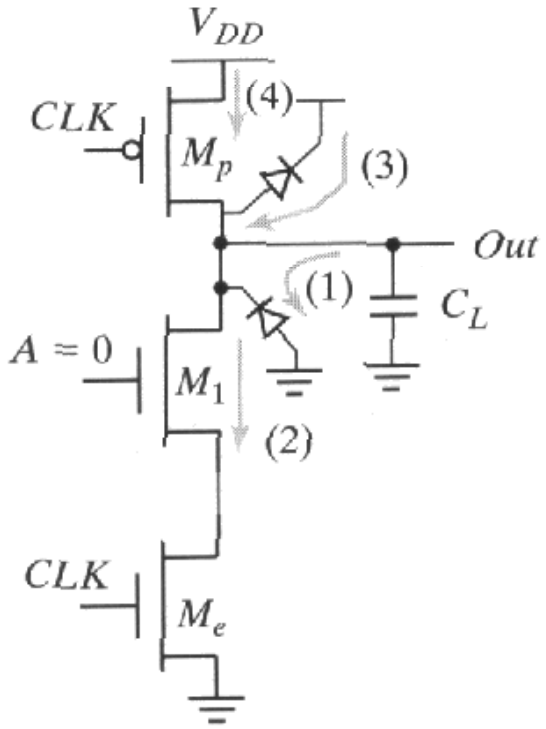
Integridade do Sinal em Lógica CMOS Dinâmica

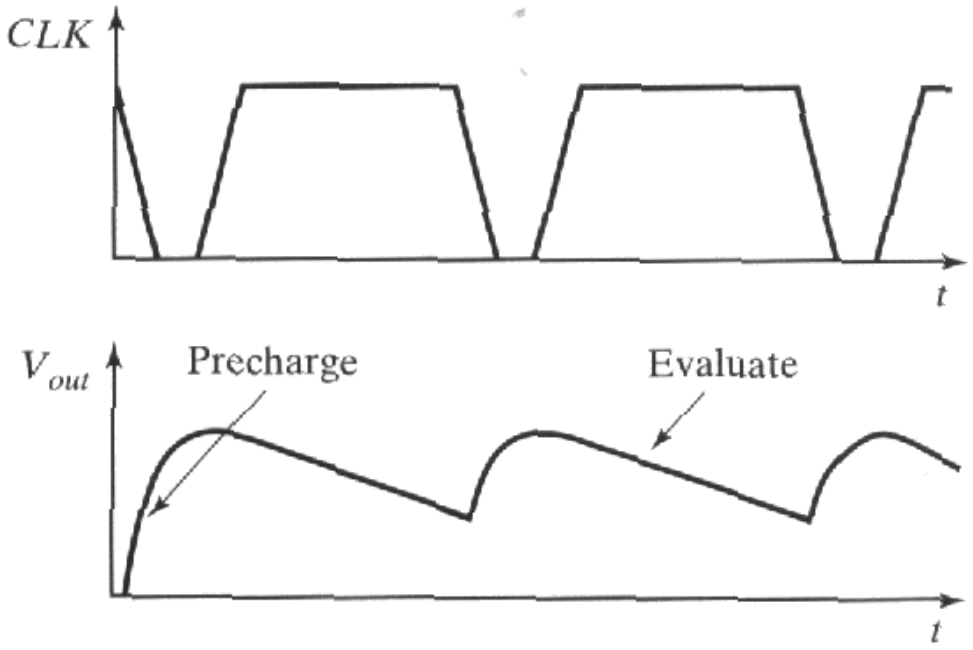
• Correntes de Fuga (*Charge Leakage*)

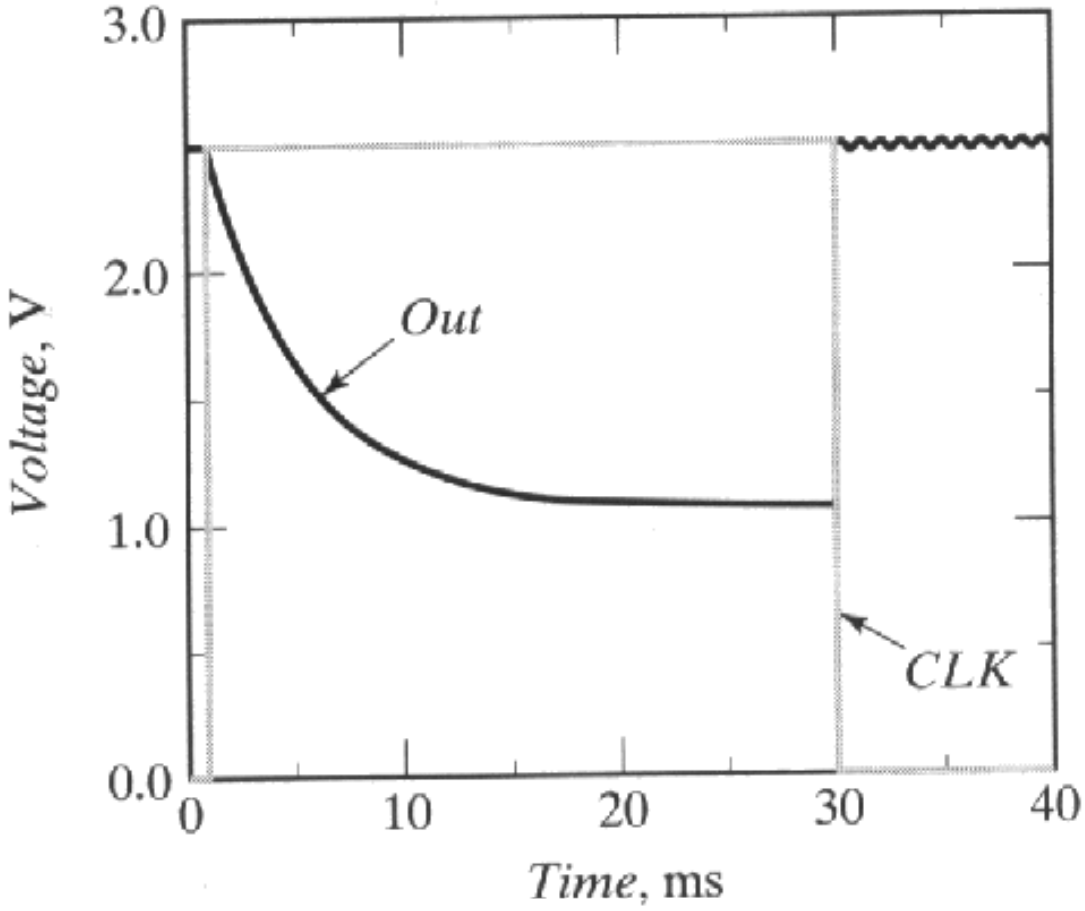
• Se o circuito PDN off durante a avaliação, a saída deve permanecer com a tensão de pré-carga V_{DD}

• C_L é gradualmente descarregado pelas correntes de fuga das junções fonte/substrato dos transistores M_p e M_1

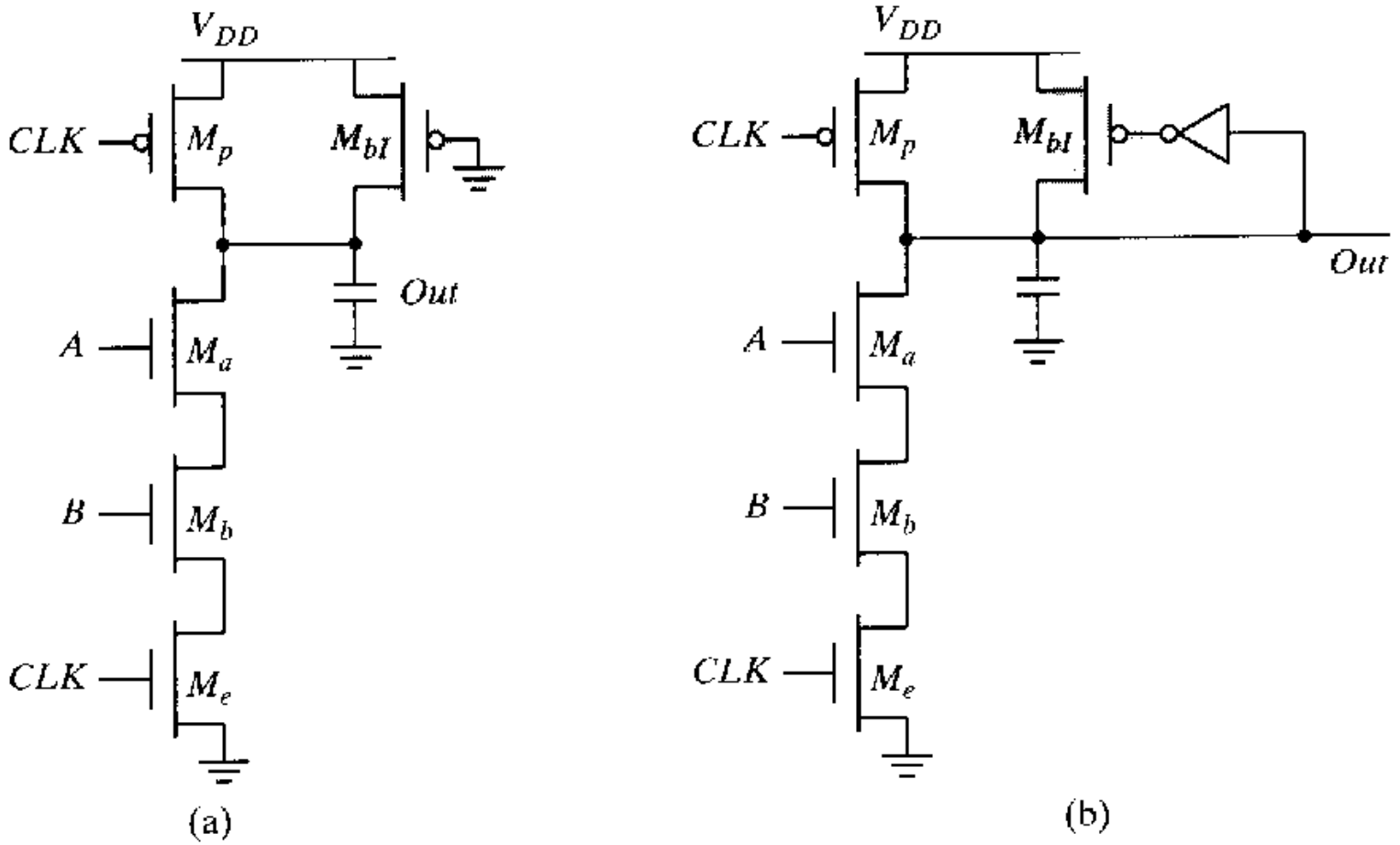
$\Rightarrow$ nível lógico degradado
$\Rightarrow$ eventualmente, um funcionamento errático.


V_{DD}
CLK
(4)
M_p
(3)
Out
(1)
C_L
$A \approx 0$
M_1
(2)
CLK
M_e

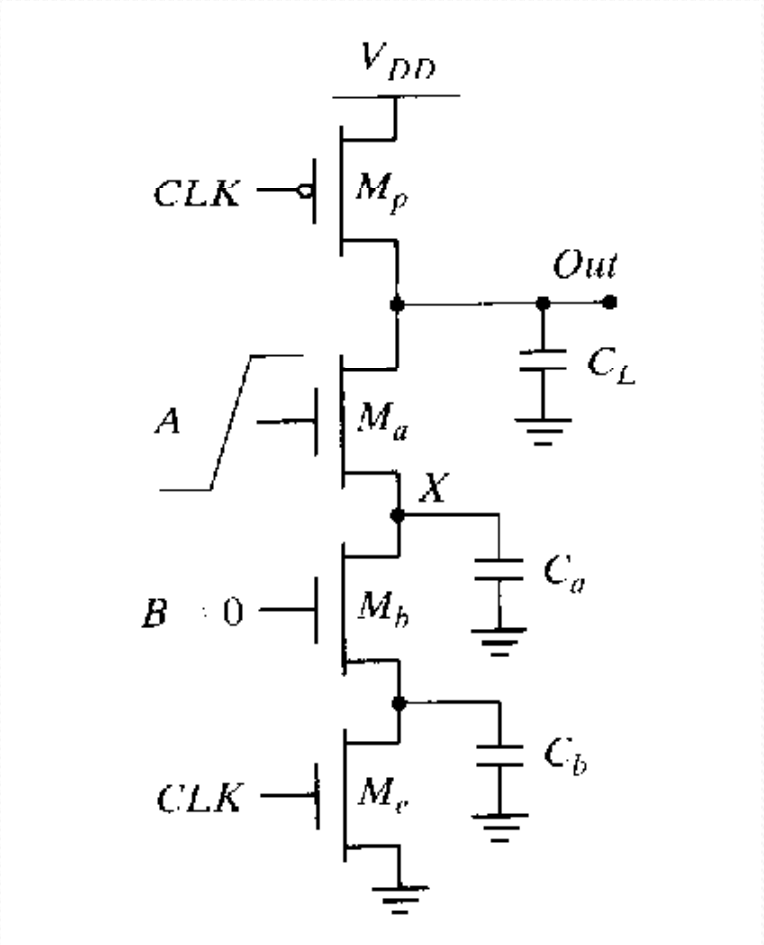

CLK
t
V_{out}
Precharge
Evaluate
t

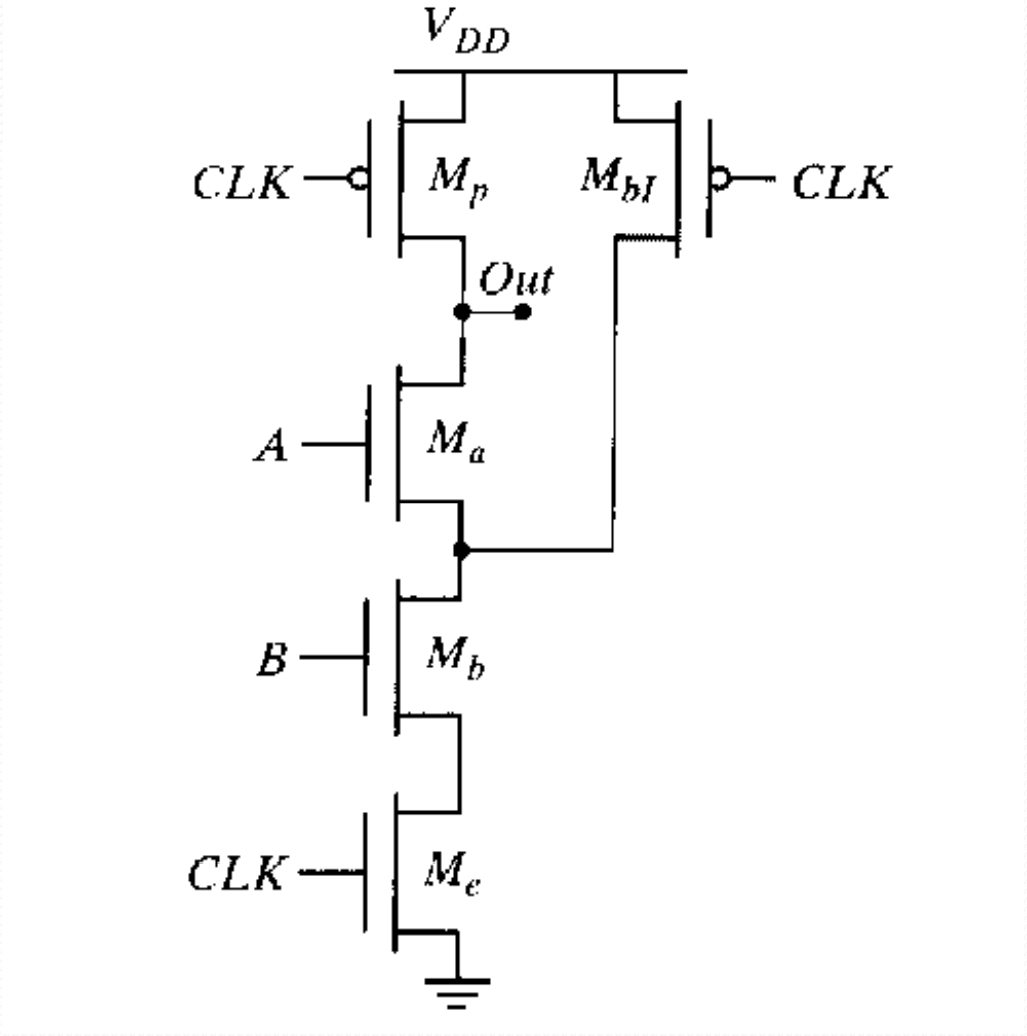


⇒ Circuitos dinâmicos requerem uma freqüência mínima de *clock*, tipicamente da ordem de alguns KHz.

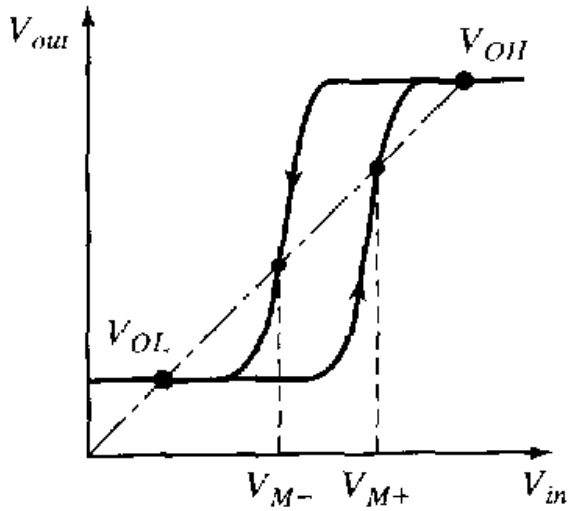

V_{DD}
CLK
M_p
M_{bl}
Out
A
M_a
B
M_b
CLK
M_e
(a)
V_{DD}
CLK
M_p
M_{bl}
Out
A
M_a
B
M_b
CLK
M_e
(b)

- Redistribuição de Carga (*Charge Sharing*)

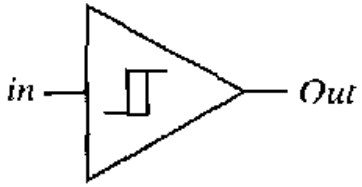



V_{DD}
CLK
M_p
M_{bl}
CLK
Out
A
M_a
B
M_b
CLK
M_e

SCHMITT TRIGGER

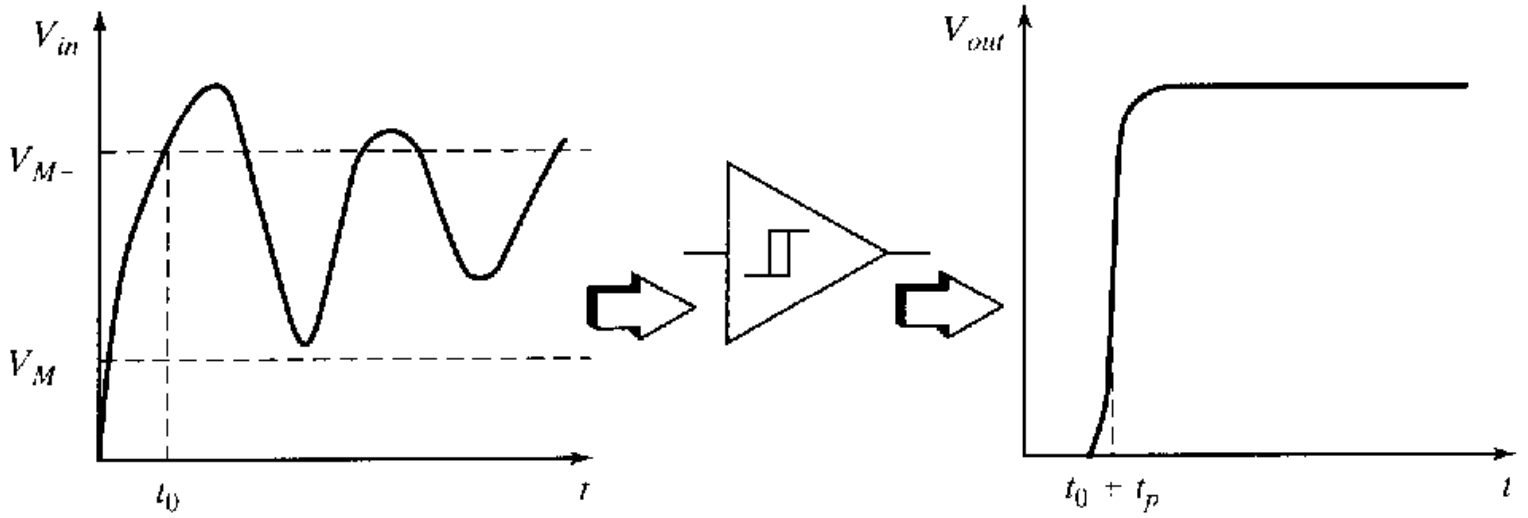


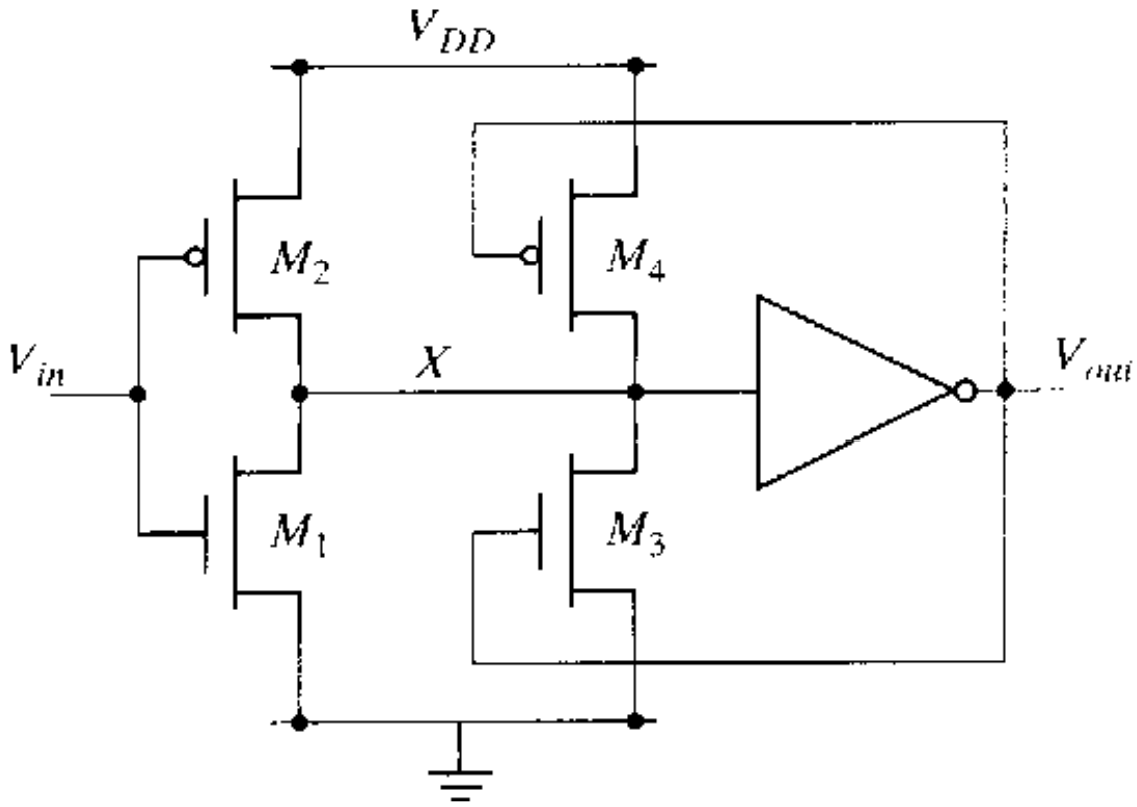
(a) Voltage-transfer characteristic



(b) Schematic symbol

• converter um sinal de entrada ruidoso e/ou lentamente variando no tempo em um sinal digital “limpo” e de transição abrupta





$\Rightarrow$ as tensões de comutação dependem de β_n/β_p entre os transistores

- Supondo $V_{in} = 0$ inicialmente, tem-se, também, $V_{out} = 0$

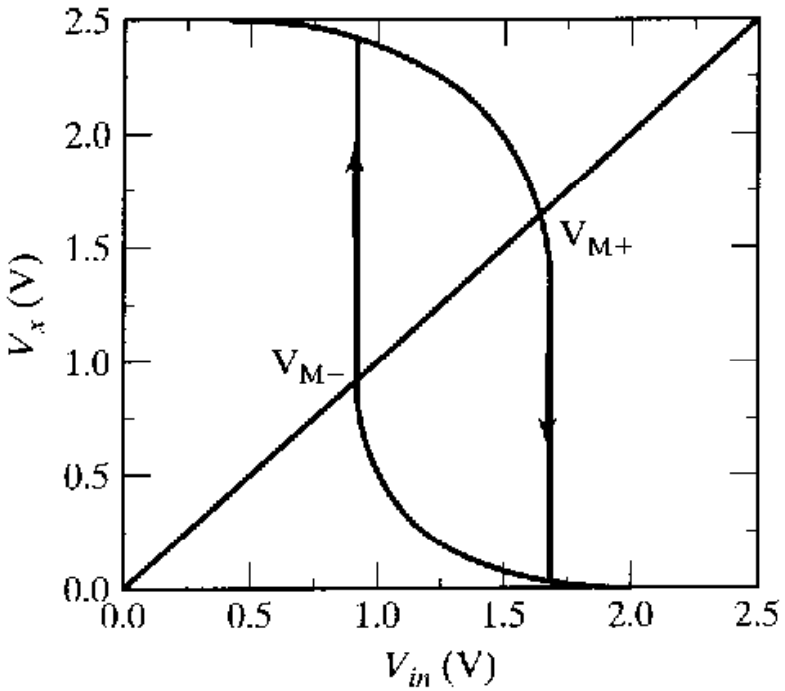
- A malha de realimentação polariza M_4 de modo a conduzir, enquanto M_3 permanece cortado

- O sinal de entrada é então conectado, efetivamente, a dois PMOS *pull-up* em paralelo (M_2 e M_4) e a apenas um NMOS *pull-down*

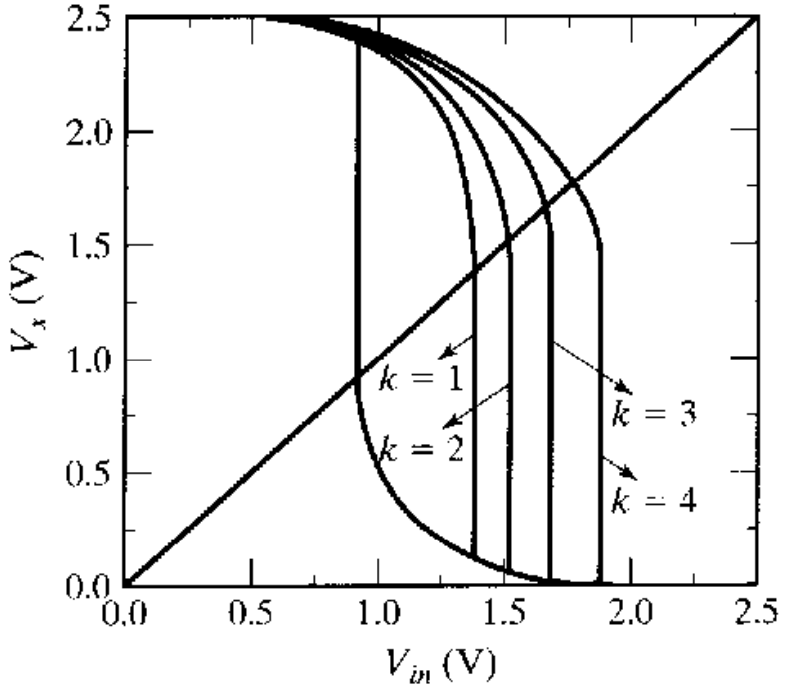
$\Rightarrow \beta_{M1}/(\beta_{M2}+\beta_{M4})$ alterada, aumentando a tensão de comutação do ST em relação ao valor do inversor (β_{M1}/β_{M2})

$\Rightarrow$ Quando o circuito comuta, a realimentação corta M_4, ativando M_3, o qual, em paralelo com M_1, acelera a transição

$\Rightarrow$ Alto ganho de malha (realimentação positiva) durante a comutação causa uma transição abrupta.

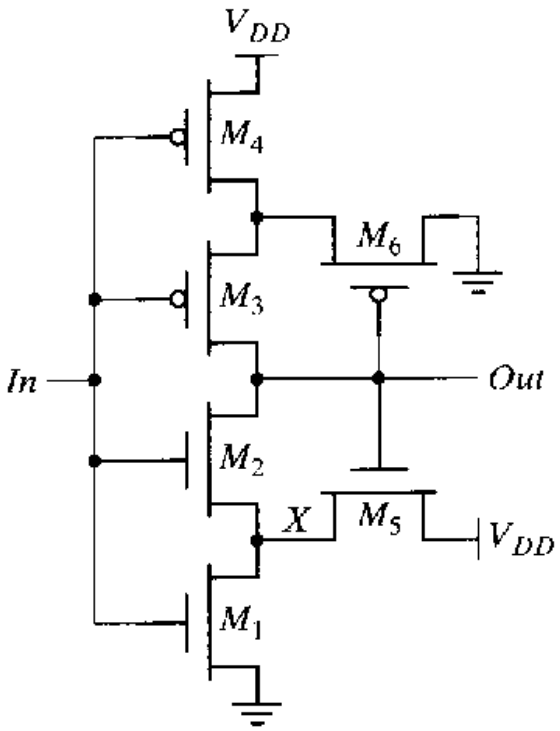


(a) Voltage-transfer characteristics with hysteresis.

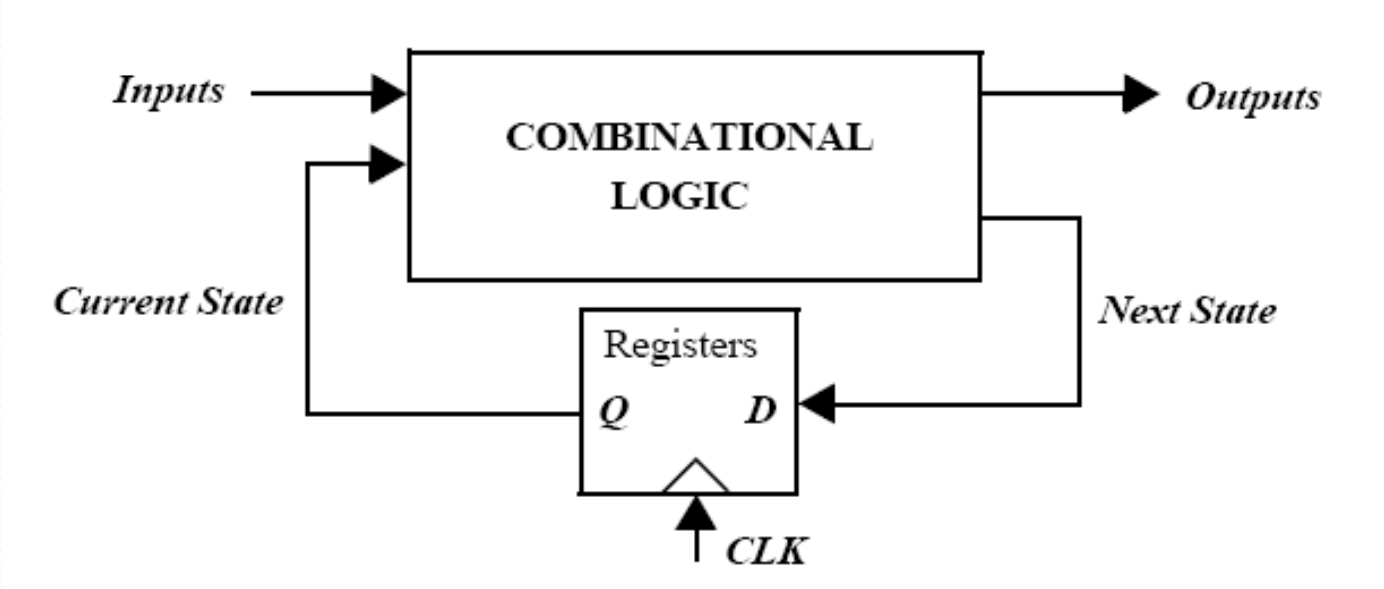


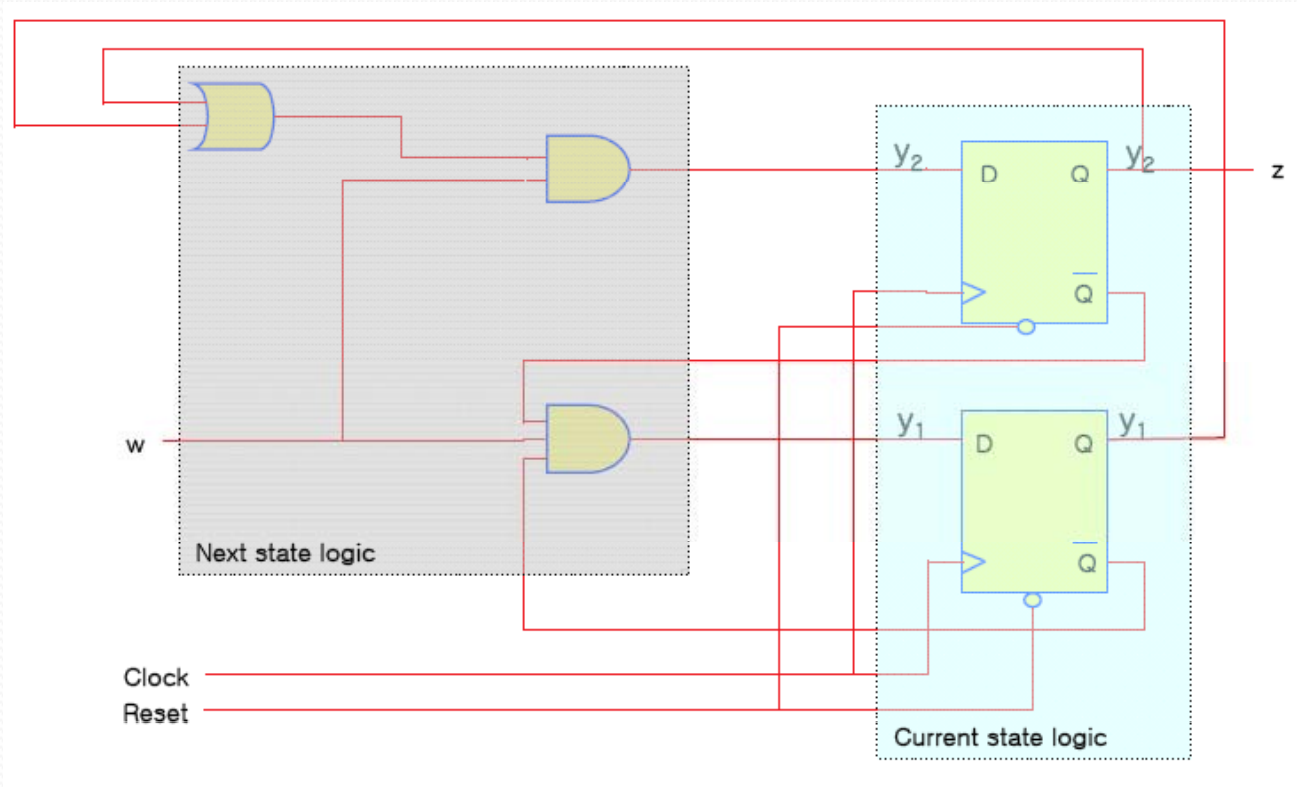
(b) The effect of varying the ratio of the PMOS device M_4. The width is $k \times 0.5$ μm.

Implementação típica de um circuito ST CMOS

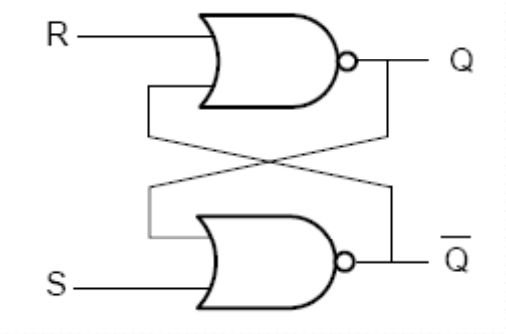


Finite State Machine (FSM)



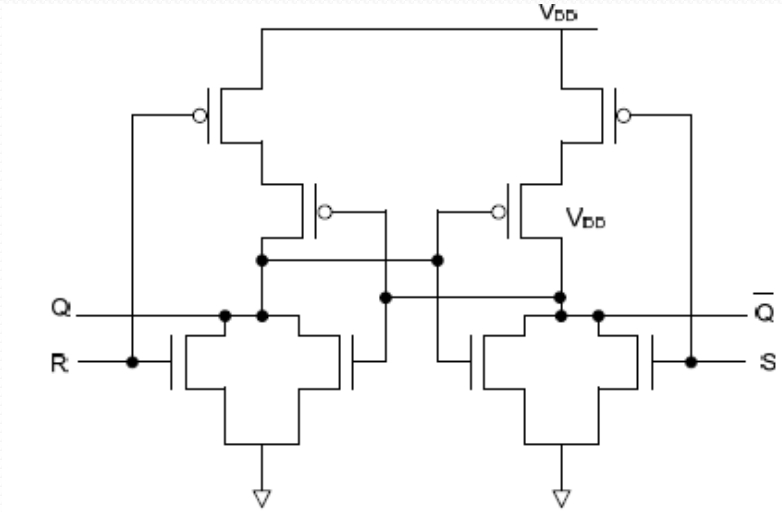

y_2
D
Q
y_2
z
$\overline{Q}$
y_1
D
Q
y_1
w
$\overline{Q}$
Next state logic
Clock
Reset
Current state logic

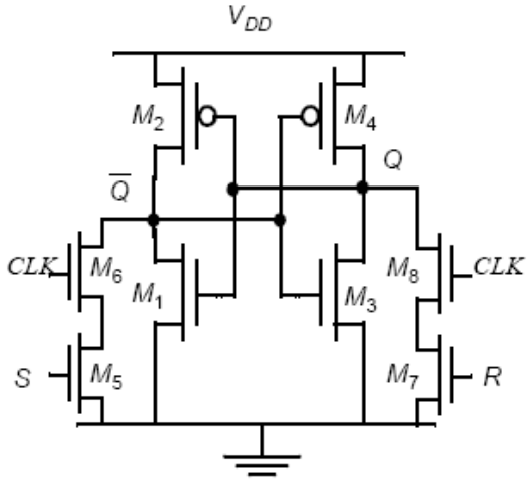
NOR-based Set-Reset Latch



S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

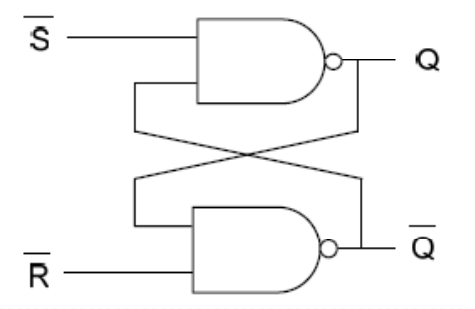
Forbidden State





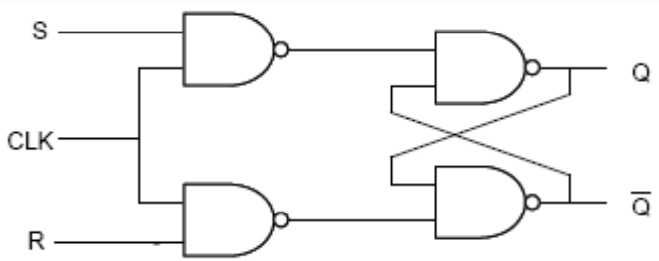
CMOS clocked *SR*

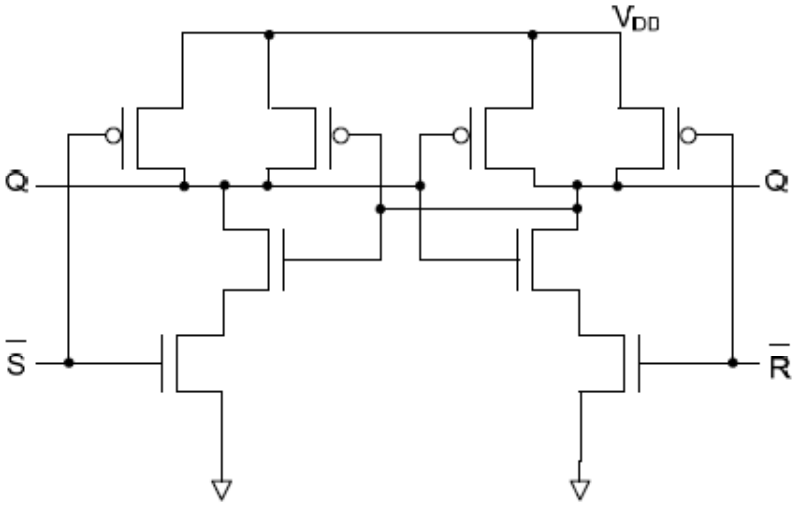
NAND-based Set-Reset Latch

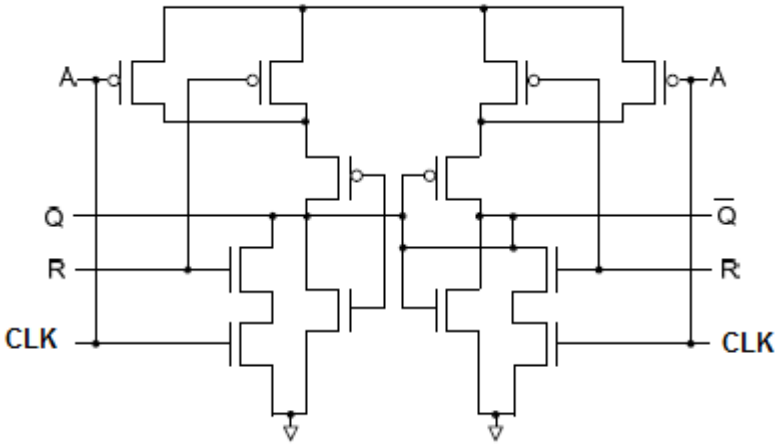


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

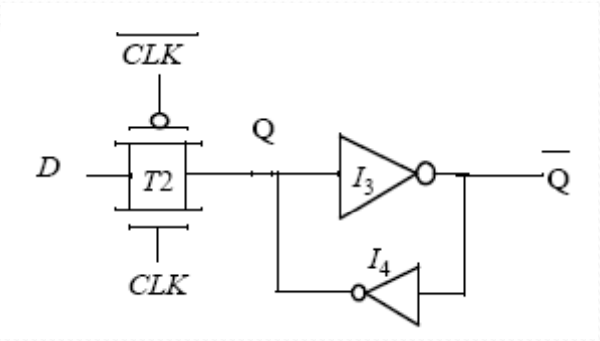
Forbidden State



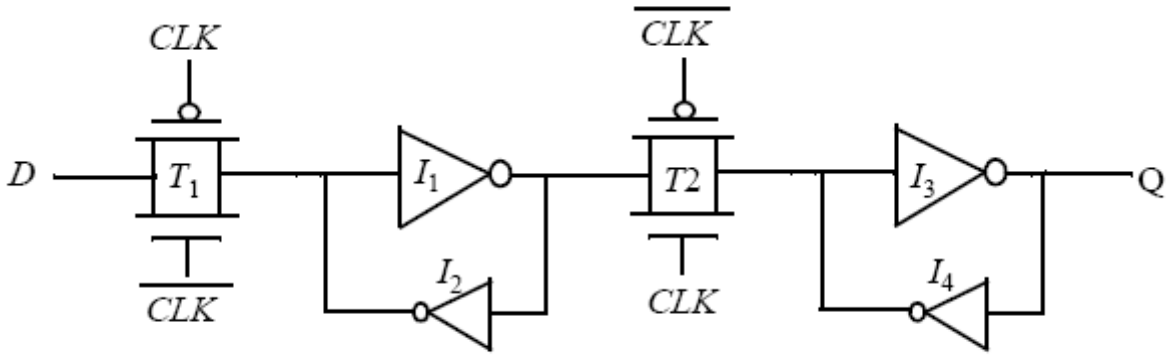




D-Type Latch



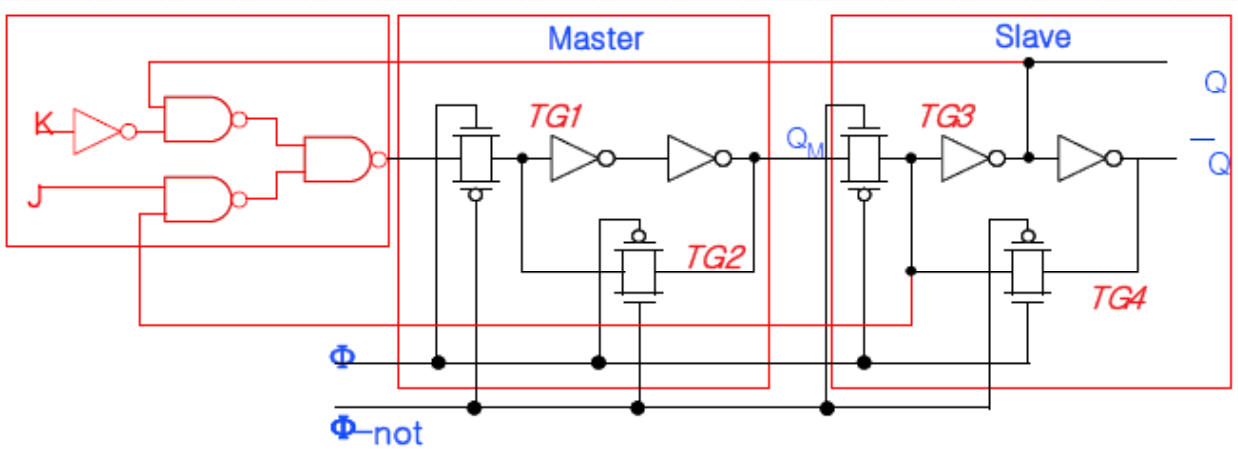
D-Type Master-Slave Flip-Flop



Reduced load clock load static *master-slave* register

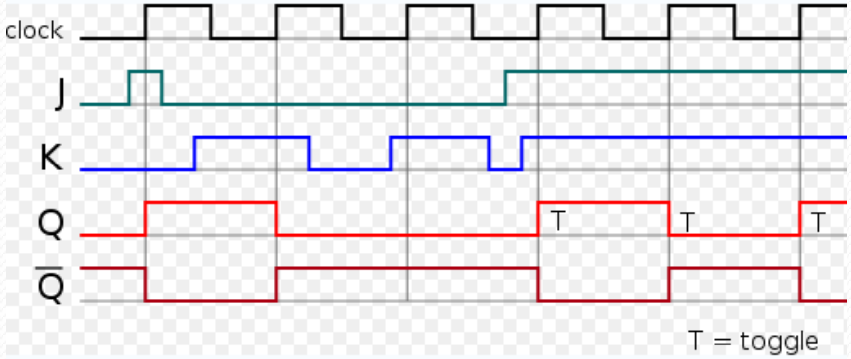
JK Flip-Flop

• improves the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or toggle command

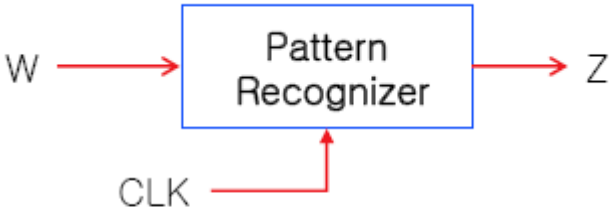


$$Q_{next} = J\overline{Q} + \overline{K}Q$$

J	K	Q_{next}	Comment
0	0	Q_{prev}	hold state
0	1	0	reset
1	0	1	set
1	1	$\overline{Q}_{prev}$	toggle



Example: Pattern Recognizer

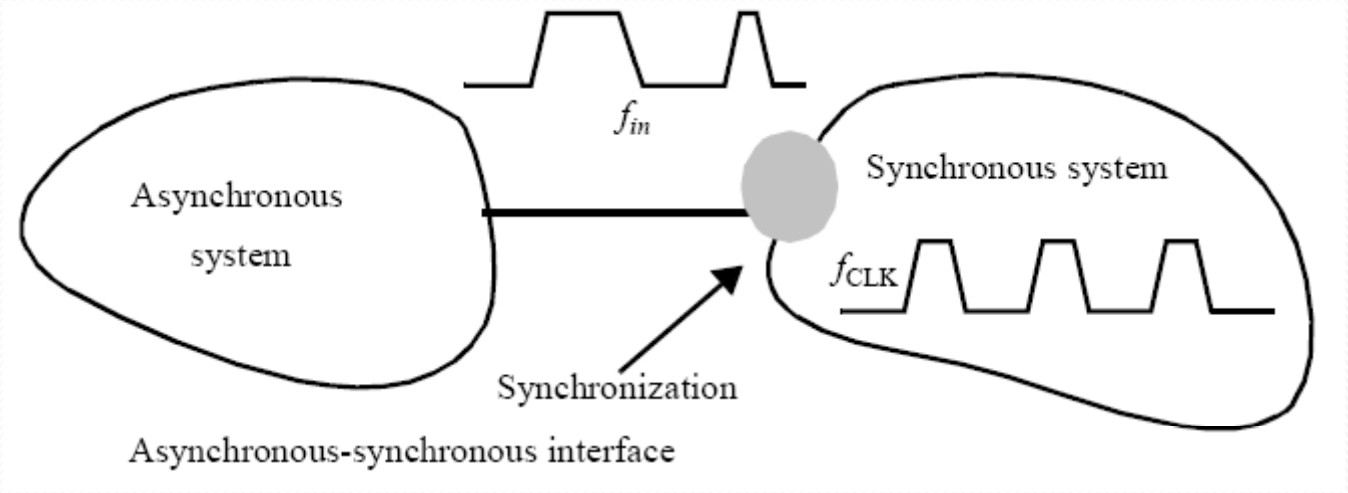


Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
W:	0	1	0	1	1	0	1	1	1	0	1
Z:	0	0	0	0	0	1	0	0	1	1	0

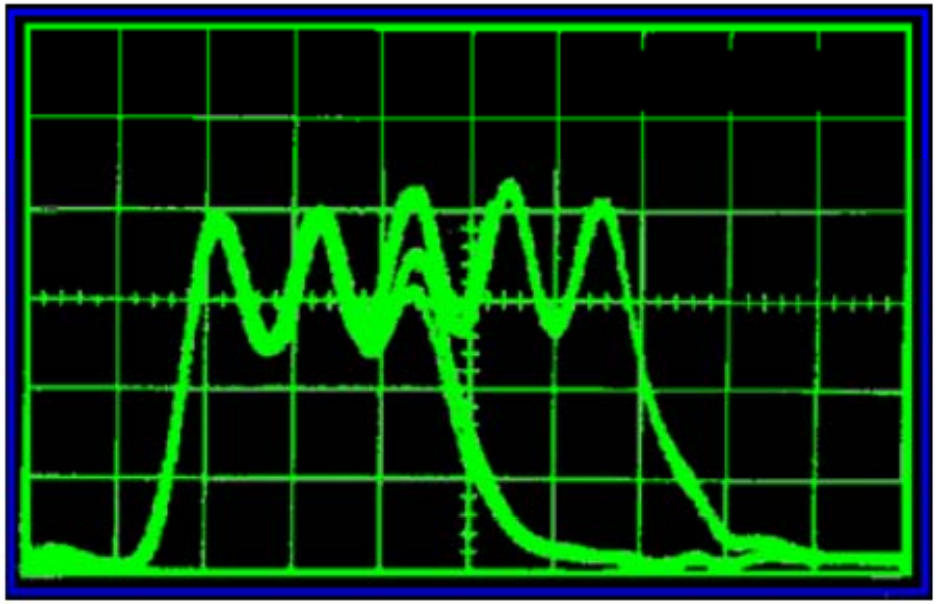
Problem:

- Circuit has input, *W*, and output, *Z*.
- All changes in the circuit occur at positive edge of the clock.
- The output *Z* is equal to 1 if
  - During two immediately preceding clock cycles, the input *W* was equal to 1
  - Otherwise, the value of *Z* is equal to 0
- It is evident that the output *Z* cannot depend solely on the present value of *W*.

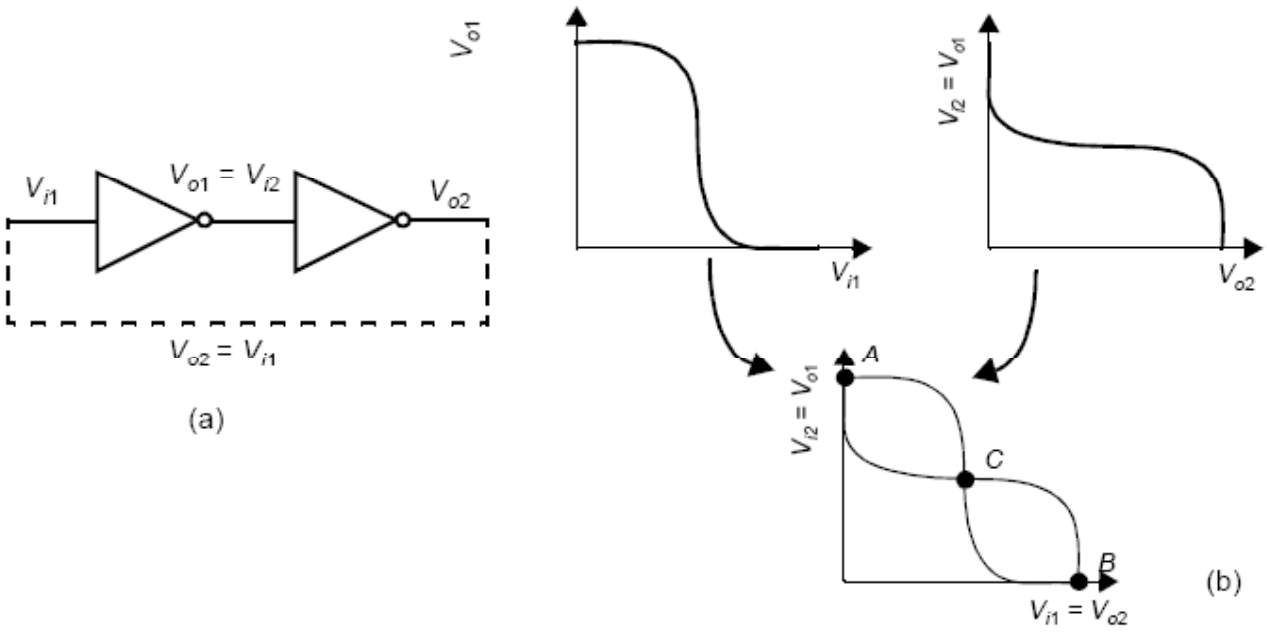
Synchronizers—Concept and Implementation



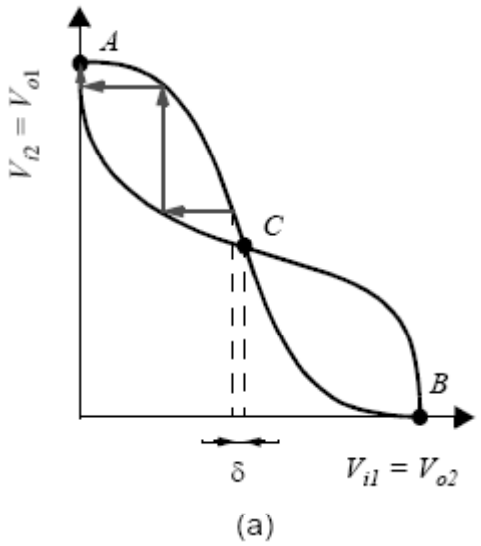
Asynchronous-synchronous interface

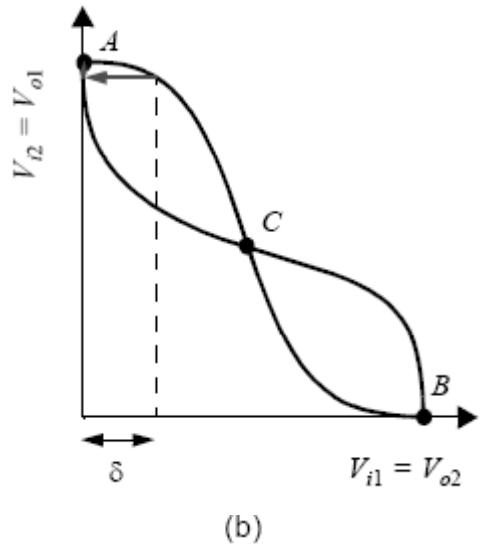


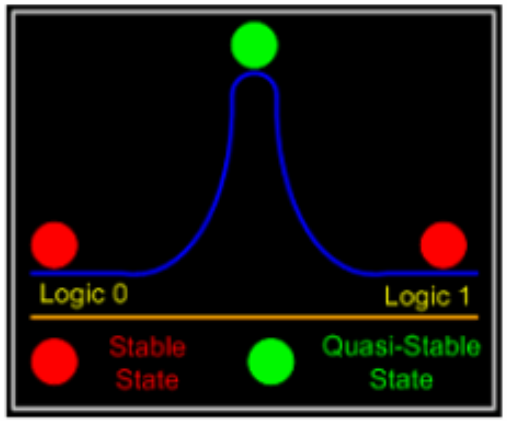
When a flip-flop is in a metastable state, its output oscillates between 0 and 1 as shown. (The flip-flop output settles down to 0.)



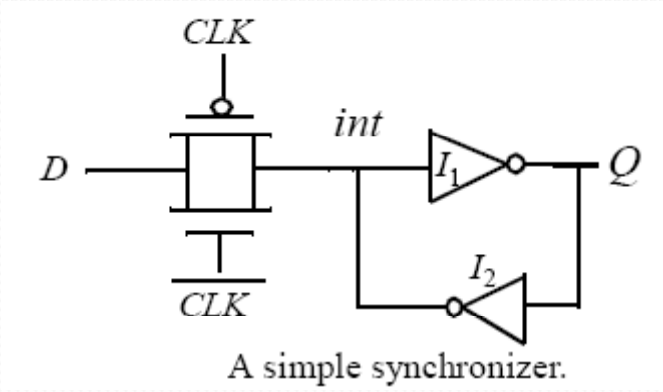
Two cascaded inverters (a) and their VTCs (b)



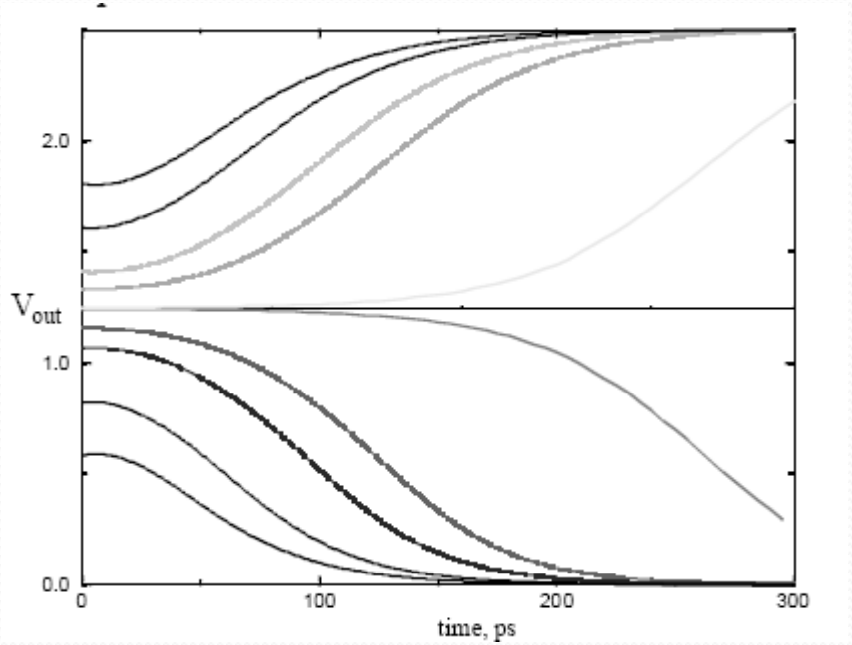




Metastability.

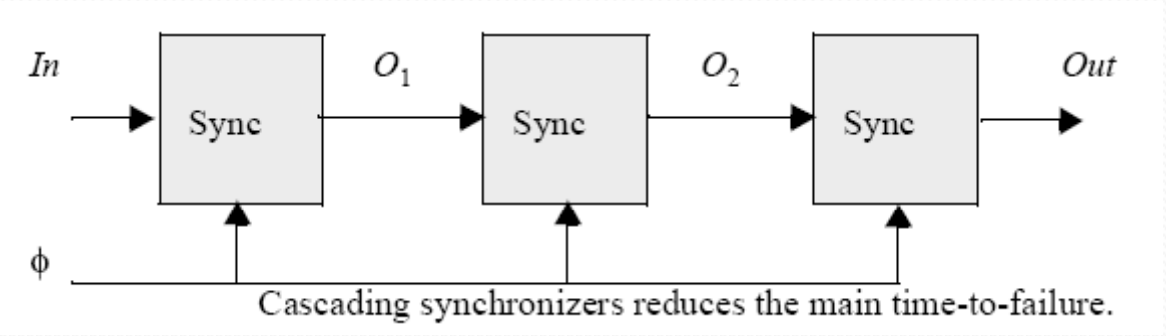


A simple synchronizer.



Simulated trajectory for a simple *flip-flop* synchronizer

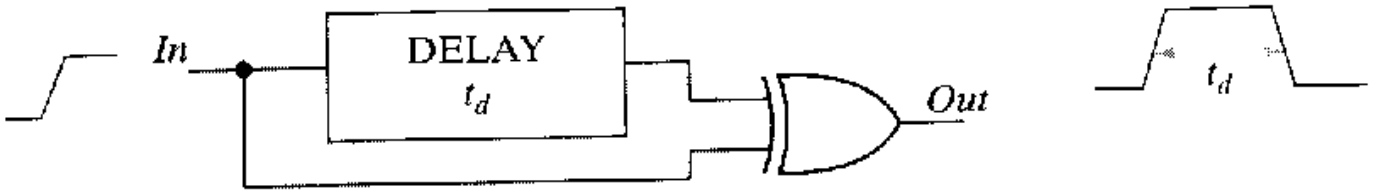
To build a perfect synchronizer that always delivers a legal answer is impossible!



Cascading synchronizers reduces the main time-to-failure.

CIRCUITOS MONO-ESTÁVEIS

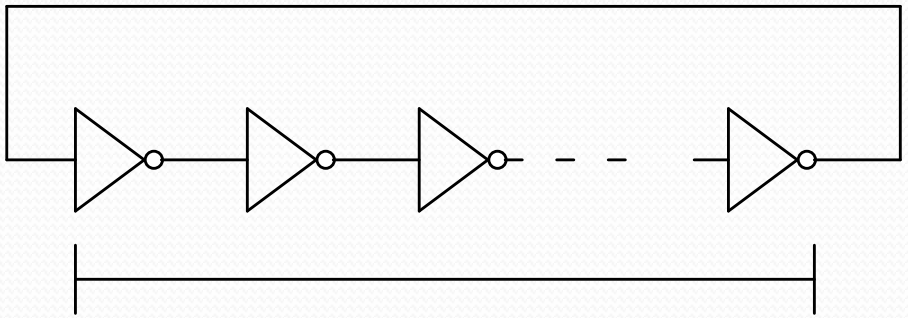
• Um circuito mono-estável gera um pulso de largura pré-determinada sob a ação de um disparo, como por exemplo, uma transição de sinal.



CIRCUITOS ASTÁVEIS

- circuito astável não possui estados estáveis
- saída oscila entre dois estados quasi-estáveis
- período determinado pela topologia e parâmetros do circuito, como atraso de propagação, tensão de alimentação

oscilador em anel (*ring oscillator*)



N inversores (N ímpar)