1.5 Low-voltage ultra-low-power analog IC design — switched-MOSFET technique

Switched-MOSFET Sampled-Data Technique for Low-Voltage Supply

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Outline

- Introduction
- The basic Switched-MOSFET (SM) cell
- Why Switched-MOSFET
- Basic SM Integrators
- Universal SM Biquad
- Practical Issues
- Results
- Conclusions

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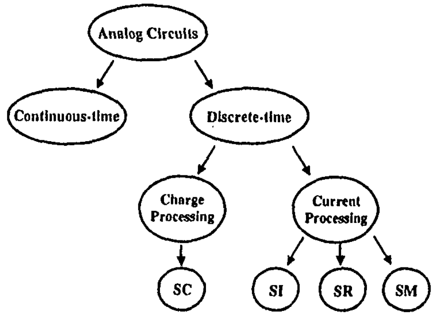
Introduction



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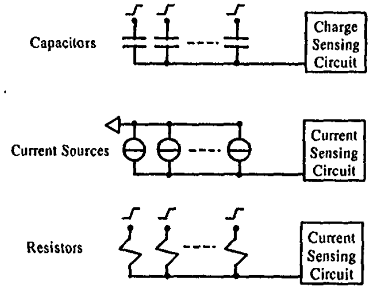
Sampled-data Circuits

Three basic elements may be used



Switched-capacitor (SC)

Switched-current (SI)

Switched-resistor ?? (SR)

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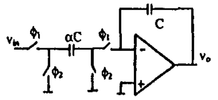
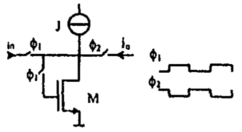
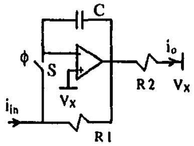
Sampled-data Circuits – Basic building blocks



Switched-capacitor (SC)
Integrator

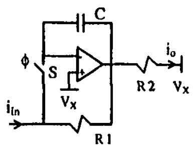


Switched-current (SI)
Delay Cell

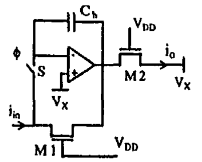


Switched-resistor (SR)
Delay Cell

Switched-resistor / Switched-MOSFET



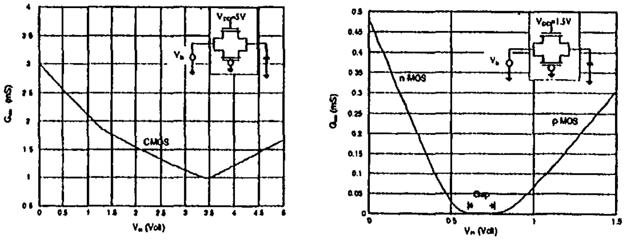
$i_o = -[R1/R2]i_{in}$



$i_o = -[(W/L)_{M2}/(W/L)_{M1}]i_{in}$

Why Switched-MOSFET ? (1) – **Low-voltage operation**

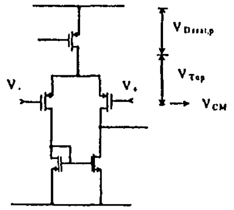
Conduction Gap of CMOS Switches



Why Switched-MOSFET ? (1) – **Low-voltage operation**

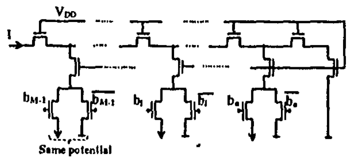
Op_amp input stage

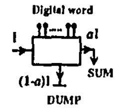
The maximum common-mode input voltage V_{CM} is around $V_{DD} - (|V_{Top}| + |V_{DSsat}|)$



Why Switched-MOSFET ? (2) – Programmability

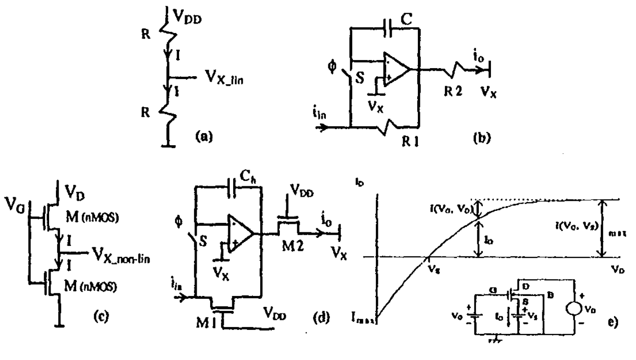
The MOSFET-Only Current Divider (MOCD)





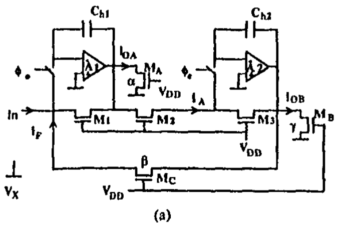
$$a = \sum_{i=0}^{M-1} b_i 2^{(i-M)}$$

Generation of common-mode voltage



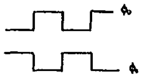
Basic SM Integrators

1st Generation Integrator



$$\frac{I_{OA}^{\phi_e}(z)}{I_{IN}^{\phi_e}(z)} = -\alpha\frac{1}{1-\beta z^{-1}}$$

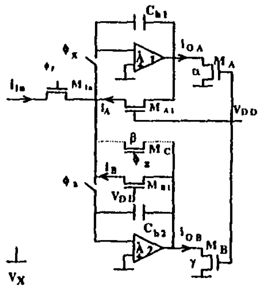
$$\frac{I_{OB}^{\phi_e}(z)}{I_{IN}^{\phi_e}(z)} = \gamma\frac{z^{-1}}{1-\beta z^{-1}}$$

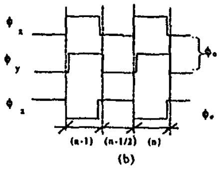


$\alpha=(W/L)_{MA}/(W/L)_{M1}$, $\beta=(W/L)_{MC}/(W/L)_{M3}$ and $\gamma=(W/L)_{MB}/(W/L)_{M3}$

Basic SM Integrators

2nd Generation Integrator



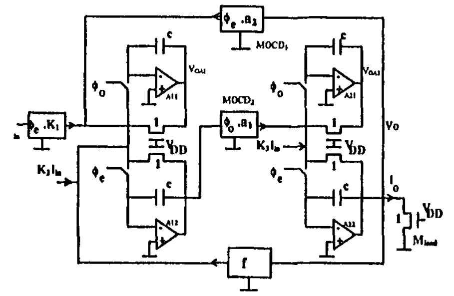


$$\frac{I_{OA}^{\phi_o}(z)}{I_{in}^{\phi_o}(z)} = -\alpha\frac{1}{1+\beta-z^{-1}}$$

$$\frac{I_{OB}^{\phi_o}(z)}{I_{in}^{\phi_o}(z)} = \gamma\frac{z^{-1}}{1+\beta-z^{-1}}$$

$\alpha=(W/L)_{MA}/(W/L)_{MA1}$, $\beta=(W/L)_{MC}/(W/L)_{MB1}$ and $\gamma=(W/L)_{MB}/(W/L)_{MB1}$

Universal SM Biquad



First Conclusions

1. SM does not need any special process or voltage doubler;
2. SM allows independent digital programming of the filter center frequency (f_0), quality factor (Q) and gain.
3. Programming is not area demanding.

♣ **The SM technique is adequate for the implementation of programmable filters at low-voltage supply.**

Some practical issues

1 – SM technique relies on opamps. Opamp GBW > 3.5 fs (same as for SC circuits) and $Av_{(DC)} > 77$ dB (linear – easily achievable) for THD < 0.1% (sinusoidal signals).

2 – Charge injection will give rise to harmonic distortion. The nonlinearity of the output current is dependent on both the Q-to-V conversion of the holding capacitor and the V-to-I conversion of the MOSFET. Therefore, switches should be minimum-size.

3 – In the SM technique, there are no "natural" integrators as in SC circuits. In SC circuits the integrator (non-switched capacitor in the feedback loop of an op amp) is the "natural" element while current amplifier is the "natural" element of the SM technique. Integrators of the SM technique are implemented by feeding back a fraction of the output current to the input. As a consequence of the operating principle of the SM technique, the offset of filters is not as easily compensated as in SC circuits.

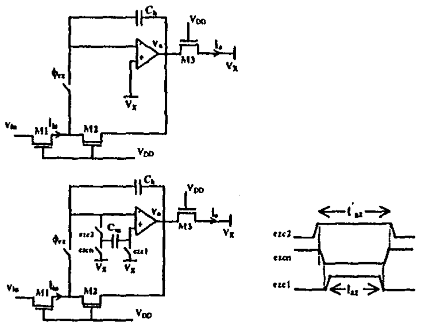
Some practical issues

4- Offset-compensating schemes may be used. In this case, the compensating capacitor contributes to total noise in the same way as holding capacitor, and thus cannot be made very small.

5 - Opamps must drive resistive loads. Hence, opamps with class AB output stage should be employed in order to avoid large power consumption.

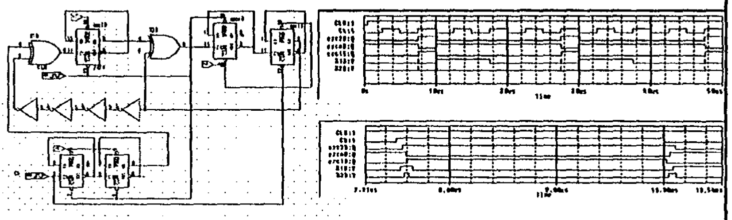
Some practical issues

Offset Compensation



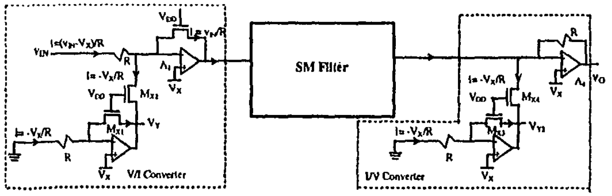
Some practical issues

Offset Compensation / Clock Generation



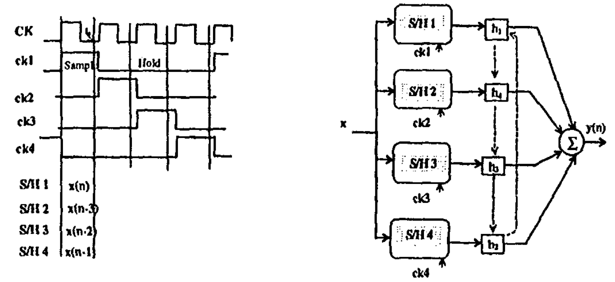
Some practical issues

V/I and I/V Converters



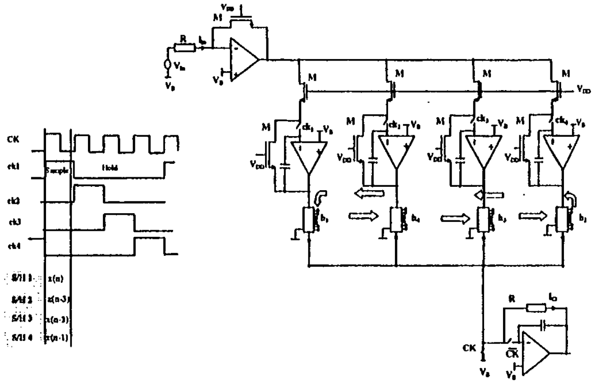
Some Results

Circulating FIR Structure

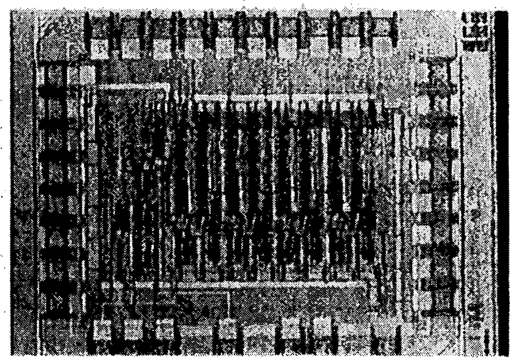


$y(n)=h_1\,x(n)+h_2\,x(n-1)+h_3\,x(n-2)+h_4\,x(n-3)$

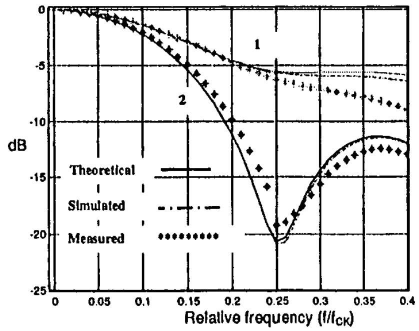
SM 4-Tap FIR Filter Realization



Fabricated Chip of Single-Ended FIR Filter (AMS 0.8μm CMOS technology)



Programmable Low-Pass Filter



1 <3F 15 0B 06>

2 <3F 36 2E 27>