SWITCHED-MOSFET TECHNIQUE FOR PROGRAMMABLE FILTERS OPERATING AT LOW-VOLTAGE SUPPLY

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ABSTRACT

The recently introduced switched-MOSFET (SM) technique is a sampled-data technique suitable for low supply voltage operation since it avoids the conduction gap of the switches and does not need any dedicated process. Nevertheless, a formalization that allows one to establish the limits of the technique has not been presented yet. In this work, a detailed analysis of the basic SM delay cell is developed. The analysis includes offset correction, settling time, noise, charge injection and harmonic distortion.

1. INTRODUCTION

Sampled-data circuits have been extensively employed in VLSI chips. The switched-capacitor (SC) technique has been the prevailing one, but in the last few years a lot of research has been done on switched-current (SI). For low supply voltage operation, however, both techniques have as the main problem the so-called "conduction gap" of the switches [6,7]. There are some special techniques to deal with this problem, such as the use of dedicated processes, on-chip generation of a voltage higher than the power supply, bootstrap circuits and the switched op-amp [7,8]. Of course, these techniques add some extra cost to the chip, and some other problems like, for example, reliability and increase in power consumption.

The recently introduced switched-MOSFET (SM) technique [1-5] overcomes the problem of the conduction gap of the switches. The SM technique uses current processing, allows easy programmability through MOSFET-only current dividers (MOCDs) [11] and does not need any dedicated process. In [1] the SM technique was introduced and a delay cell and integrator were presented. In [2-3] a second generation SM integrator and a second order SM programmable filter were presented and implemented. In [4] a single-ended FIR filter suitable for equalizer architectures was integrated and tested. In [5] a fully balanced FIR filter was designed and integrated. All these circuits can be designed to operate at low-voltage supply (i.e. 1.5V or less). Nevertheless, a formalization that allows one to establish the limits of the SM technique and to compare it with the conventional sampled-data techniques had not been presented yet. In this work, a detailed analysis of the delay cell proposed in [2] is developed. The analysis includes offset correction, switching sequence, settling time, noise, charge injection and harmonic distortion.

2. THE SWITCHED-MOSFET TECHNIQUE

The basic delay cell of the switched-MOSFET technique is presented in Figure 1 [2]. This cell, a switched current mirror, operates as follows. When the switch is closed, assuming the operational amplifier (op-amp) to be ideal, we have, neglecting transistor mismatch,

$$i_o = -[(W/L)_{M3}/(W/L)_{M2}]\, i_{in} \qquad (1)$$

since M2 and M3 are both biased with the same set of voltages. The output current i_o is an inverted replica of the input current i_{in}. The capacitor C_h is charged to a voltage V whose value depends on i_{in}, on the parameters of transistor M2 and on the gate voltage. When the switch opens, the voltage V is held on the memory capacitor (C_h) and the current is sustained at the output. The n-MOS switch (S) operates at a constant voltage equal to V_X, which is generated by the series association of two identical transistors as shown in Figure 2 [2,6]. This network, apart from its nonlinearity, is similar to a resistive voltage divider with two identical resistors, one connected to V_{DD} and the other to ground. The connection of a resistor between V_X and either V_{DD} or ground would result in the same current with opposite directions. Thus, the voltage V_X provided by the circuit in Figure 2 allows for the highest current swing. It also guarantees that the n-switch operates outside of the conduction gap.

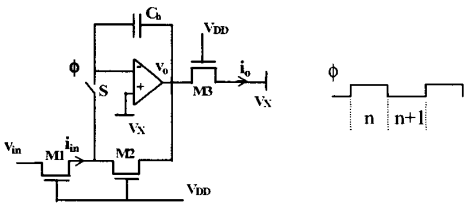

Figure 1. The delay cell of the switched-MOSFET methodology [2].

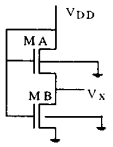

Figure 2. Bias circuit for the delay cell and integrators. M_A and M_B are identical transistors. $V_X = V_P(1-1/\sqrt{2})$. V_P is the pinch-off voltage [9,10].

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3. ANALYSIS OF THE SM DELAY CELL

3.1 Offset correction

Consider the circuit in Figure 1. The offset voltage V_{OS} of the op-amp gives rise to a DC error Δi_O in the output current given [2] by

$$\frac{\Delta i_O}{I_{max}} = 2\sqrt{2}\frac{V_{OS}}{V_P} \quad (2)$$

where

$$I_{max} = \frac{\beta_2 n}{4} V_P^2 \quad (3)$$

In (3), n is the slope factor [9] and $\beta = \mu_n C_{ox}(W/L)$, where μ_n is the electron mobility and C_{ox} is the oxide capacitance per unit area. Figure 3 illustrates the transistor output characteristic for $V_S = V_X$. The curve shows that $V_S = V_X$ allows for equal positive and negative current swings (I_{max}).

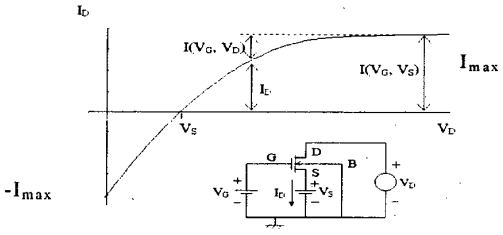

Figure 3. Maximum current in the delay cell.

In the S/H circuit, the error in the output current is proportional to the offset voltage of the op-amp. This error will affect the dynamic range of the circuits. Thus, in some applications, it will be necessary to overcome this drawback by using offset compensation techniques. The offset compensation circuit suggested in [5] is shown in Figure 4. It is based on Nagaraj's correlated double-sampling (CDS) circuit for switched-capacitor circuits [12].

The operation of the circuit is as follows. When ϕ_c is high, the offset voltage is stored in C_c. Consequently, when ϕ_c is low the offset appears as an input signal and its effect on the output is ideally cancelled out.

In the sequel, the circuits in Figure 1 and in Figure 4 will be compared. For the circuit in Figure 1, we have, for identical transistors:

$$i_o(n+1) = \frac{-i_{in}(n)}{1+A^{-1}} + \left(\frac{V_{OS}}{1+A^{-1}} - A^{-1}V_X\right)\frac{1}{R} \quad (4)$$

where $R = (\partial I_D/\partial V_S)^{-1}\big|_{V_S=V_D=V_X}$ and A is the DC gain of the op-amp. For the circuit in Figure 4 (identical transistors):

$$i_o(n+1) \equiv -\frac{i_{in}(n+1/2)}{1+A^{-1}} + \frac{A^{-1}.V_{OS}}{(1+A^{-1})^2}\frac{1}{R} - \frac{A^{-1}.i_{in}(n-1/2)}{1+(2+K_c)A^{-1}} \quad (5)$$

where $K_c \equiv (C_c/C_h)$.

Comparing (4) with (5) we note that the offset correction circuit not only attenuates V_{OS} by the DC gain of the op-amp but also eliminated the effect of V_X on the output. As a drawback, there is a term (the right-most one in (5)) that depends on the previous sample. Nevertheless, this term is attenuated by the DC gain of the op-amp and, in most cases, is not significant.

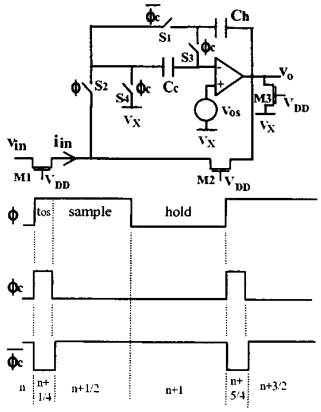

Figure 4. Delay cell with offset correction.

An appropriate switching sequence is fundamental for the correct operation of the circuit in Figure 4. If ϕ_c closes before $\overline{\phi_c}$ opens, a fraction of the charge stored in C_C may be lost.

The results obtained in (5) are similar to those obtained for SC offset correction schemes [12].

3.2 Settling time

To keep distortion within acceptable values, the settling error must be small. For the circuit in Figure 1, the settling error is given by

$$\gamma = e^{(-T/2\tau)} \quad (6)$$

where T is the clock period and τ is a time-constant which depends on the hold capacitor, the transistor conductances, and the gain-bandwidth product of the op-amp. In the analysis that follows we are going to calculate the value of C_h in order to keep the settling error below a given value. For the circuit in Figure 4, t_{OS} can be very small because C_C, in each cycle, charges to a value whose drift is negligible. Thus, (6) also holds for the circuit in Figure 4.

The small signal equivalent circuit for the delay cell (for both circuits of Figures 1 and 4) is shown in Figure 5. The resistance of the switches is assumed to be negligible.

For the circuit in Figure 5, assuming $g_m >> g_1+g_L+g_Lg_1/g_2$, where $g_L=g_3+g_o$, and the op-amp finite transconductance represented by a single-pole function, that is, $g_m = g_m(s) = \frac{g_{m0}}{1+s/\omega_1}$ where ω_1 is the dominant pole of the op-amp, we have:

$$C \le g_2 \frac{T}{2}\frac{1}{\ln(1/|\gamma|)} - \frac{g_1g_2 + g_1g_L + g_2g_L}{2\pi f_u g_o} \quad (7)$$

in order to have a settling error smaller than γ. Here, f_u is the unity-gain frequency of the unloaded op-amp in open-loop, g_1, g_2

and g_3 are the drain-source conductances of the transistors, which in strong inversion are given [10] by:

$$g_{mS(D)} = \beta n(V_P - V_{S(D)}) . \quad (8)$$

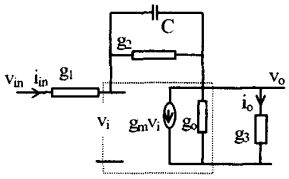

Figure 5. Small signal equivalent circuit.

Considering an 8-bit settling error (γ = 0.004), g_1=g_2=g_3 and g_o>>g_2, (7) can be rewritten as:

$$C \le \frac{g_2}{11}\frac{1}{f_s} - \frac{g_2}{\pi}\frac{1}{f_u} \quad (9)$$

where f_s is the sampling frequency. Therefore, if $f_u < 3.5f_s$, (9) has no solution. This constraint in f_u is the same as for SC circuits [13].

If the on-resistance of the switches is taken into account, then a reduction of the value of C in (7) given by the factor $g_{on}/(g_{on}+2g_2+g_1)$ is a good approximation. The results given by (7) and the approximation mentioned above were compared against SMASH [14] simulation results (the ACM model [14] was used), showing good agreement.

3.3 Noise

The noise analysis has been carried out in the circuit with offset correction (Figure 4), which employs correlated double sampling technique. Therefore, the 1/f noise as well as the offset are considerably reduced [15]. For noise analysis, the methodology proposed in [16] has been employed. It consists in decomposing the equivalent noise circuit into time-invariant subcircuits, valid for specific time intervals, and into a transientless sampled-data network with band-limited noise sources.

The total noise in the hold interval is:

$$v^2_{tot\_hold} = \pi f_u \theta R_{eq} + \frac{1}{2}\frac{\theta}{C_h} + \frac{1}{2}\frac{\theta}{C_c}\left[1+\left(\frac{g_1}{g_2}\right)^2\right] \quad (10)$$

where θ =kT, k is Boltzmann's constant, T the absolute temperature, and R_{eq} the noise equivalent resistance of the op-amp. The mean-square value of the output voltage of the circuit without offset correction does not contain the influence of C_c; however, the 1/f noise has to be taken into account.

3.4 Charge injection

The charge injected by the switches into the capacitors has two components [13,15]. The first one is called clock feedthrough and is caused by the overlap gate/drain and gate/source capacitances. The second one is due to the channel charge, which has to flow through drain and source when the switch opens. In general, the channel charge is the dominant one [15].

The voltage variation in a linear capacitor C due to clock feedthrough in a MOS switch is given by

$$\Delta V_{ov} \cong \Delta V_{GB(OFF)} \frac{C_{ov}}{C_{ov}+C} \quad (11)$$

where $\Delta V_{GB(OFF)}$ is the V_{GB} swing between switch cut off and V_{SS}. The switch cuts off when V_{GB}<nV_{SB}+V_{T0}, where V_{TO} is the threshold voltage [2,9]. As long as all switches operate at constant voltage V_X, we have

$$\Delta V_{ov} \cong (V_{T0} - V_{SS})\frac{C_{ov}}{C} \quad (12)$$

where C_{ov} is the overlap capacitance. For the analysis of the effect of the channel charge, the inversion charge density in strong inversion is given by:

$$Q_I' \cong -nC_{ox}'(V_P - V_c) \quad (13)$$

where V_c is the channel voltage, equal to V_X in this case. Substituting $V_c = V_X$ and V_p= (V_{GB}-V_{T0})/n into (13) yields

$$Q_I = WLQ_I' \cong -WLC_{ox}'\frac{V_{GB} - V_{T0}}{\sqrt{2}} \quad (14)$$

where W and L are the effective width and length of the channel, respectively. In the worst case, we have the following expression for the voltage variation in the output (Figure 4):

$$\Delta V_{tot\_max\_out} = (V_{T0} - V_{SS})WC_{ov}'\left(\frac{1}{C_c}+\frac{1}{C_h}\right) + \\ + WLC_{ox}'\frac{V_{DD} - V_{SS} - V_{T0n}}{\sqrt{2}}\left(\frac{1}{C_c}+\frac{1}{C_h}\right) \quad (15)$$

The result given by (15) is in close agreement with SMASH simulation, i. e., the simulated value is about 50% of the *maximum* value calculated by (15).

3.5 Harmonic distortion

In this section, we analyze the influences of charge injection, component mismatch and finite op-amp DC gain on the harmonic distortion are analyzed, for the circuit in Figure 1.

The channel charge is signal-independent because the switches operate at constant voltage. Nevertheless, the fraction of the charge that flows to C_h depends on the impedances on both sides of the switch; which are assumed to be signal-independent [17]. Thus, the voltage error introduced in C_h due to charge injection will be considered to be constant (for that, C_h has to be linear). Even though the charge injected into the capacitor is signal-independent, this error will give rise to harmonic distortion since the V-to-I conversion is nonlinear. As the harmonic distortion caused by charge injection is independent of the frequency of the input signal, the circuit of the delay cell will be assumed a continuous-time circuit; thus:

$$i_{O(t)} \cong 2\sqrt{2}\frac{V_{c\_inj}}{V_P}I_{max} - \hat{I}\cos(\omega t) \\ -\frac{\sqrt{2}}{8}\frac{V_{c\_inj}}{V_P}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{\sqrt{2}}{32}\frac{V_{c\_inj}}{V_P}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t)... \quad (16)$$

where $\hat{I} \le I_{MAX} = \frac{\beta n}{4}V_P^2$ is the peak input current, and V_{c_inj} is the voltage variation in C_h due to charge injection. The first term on the right hand side of (16) is the offset. If we neglect clock feedthrough, the offset current becomes:

$$\frac{I_{OS}}{I_{max}} \leq 2n\frac{C_{switch}}{C_h} \quad (17)$$

where $C_{switch} \equiv C_{ox}^{'}(WL)_{switch}$.

In a delay cell with a 2V supply, 5.6μm/5.6μm transistors and 3μm/0.7 switch S, C_h=2pF, (0.7μm ES2 technology): (I_{OS}/I_{Omax}) ≤ 0.60% and the total harmonic distortion (THD) ≤ 0.039%.

A difference in the transconductance parameters (β's) produces a relative gain error proportional to the mismatch in the transconductance parameters. A mismatch in the threshold (pinch-off) voltage causes gain error and harmonic distortion, summarized by the following expression [2]:

$$x_2 = \left(1 + \frac{\Delta V_P}{V_P}\right)x_1 + \frac{\Delta V_P}{V_P}\left(\frac{x_1^2}{8} + \frac{x_1^3}{32} + ..\right) \quad (18)$$

where $\frac{\Delta V_P}{V_P} = \frac{\Delta V_{TO}}{V_{DD} - V_{TO}}$ is the threshold voltage mismatch normalized to the overdrive voltage and $x_1 = i_{in}/i_{in\,max}, x_2 = i_o/i_{o\,max}$ are the normalized input and output currents.

The influence of the finite op-amp DC gain A in the output current of the circuit in Figure 1is given by

$$i_{O(t)} \equiv \frac{2\left(1-\sqrt{2}\right)}{A} I_{max} - \hat{I}\cos(\omega t) - \frac{1}{8A}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{1}{32A}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t)..(19)$$

Using the same considerations as for charge injection and with A=100: (I_{OS}/I_{Omax}) = 0.83% THD = 0.13%

4. CONCLUSIONS

The switched MOSFET technique is an alternative sampled-data technique suitable for low-voltage operation. It does not need any special process. In this particular respect, the SM technique compares advantageously with the traditional SC and SI techniques. Regarding offset correction, settling time, noise, charge injection and harmonic distortion, SM presents results similar to those presented by the SC and SI techniques. SM also excels at programming simplicity. It may be very useful in applications where programmable low-voltage low-frequency filters are required, such as hearing aid circuits.

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