A SWITCHED-MOSFET FILTER FOR APPLICATION IN HEARING AID DEVICES

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ABSTRACT

The characteristics of the recently introduced switched-MOSFET (SM) technique make it very useful in applications where programmable low-voltage filters are required, such as in hearing aids circuits. In this paper we present an SM programmable bandpass filter intended for hearing aid devices. We also address a comparison of our bandpass filter with a filter previously described in the literature [7], which has been implemented with the well-known switched-capacitor (SC) technique.

1. INTRODUCTION

The switched-MOSFET (SM) technique has recently been introduced [1-6]. It is a sampled-data technique suitable for low supply voltage operation since the switches operate within the conduction range of the MOSFET, thus overcoming the problem of the conduction gap. Besides, the SM technique does not need either dedicated processes or clock voltage multiplication schemes. The basic building block of the SM technique is a low-voltage sample-and-hold composed of an operational amplifier (opamp) and MOS transistors operating in the triode region. Programmability of SM circuits, which is achieved through MOSFET-only current dividers (MOCDs) [15], is simple and does not require a large silicon area.

The characteristics of the SM technique make it very useful in applications where programmable low-voltage filters are required (i. e., 1.5V or less), such as in hearing aids circuits [7-10]. In this paper we present an SM programmable bandpass filter intended for hearing aid devices. We also address a comparison of our bandpass filter with a filter previously described in the literature [7], which has been implemented with the well-known switched-capacitor (SC) technique. The desirable characteristics for the filter are as follows:

- Adjustable bandpass of 100-350Hz, 350-1000Hz and 1000-5000Hz.
- Adjustable Gain of 0dB, 6dB, 12dB and 18dB.
- Constant quality factor of about 1.
- Supply voltage of 1.4V.

Switched-capacitor circuits process information in the voltage domain, while SM circuits process information in the current domain. In order to provide a fair comparison between SM and SC filters, both input and output signals are considered to be in the same domain – in this case voltages. Additional voltage-to-current (v-to-i) and current-to-voltage (i-to-v) converters are thus required.

This paper is organized as follows. In Section 2 we show how the input v-to-i converter has been implemented. Section 3 presents some implementation issues about the SM filter as well as noise analysis. Section 4 shows simulation results and addresses a comparison of the SM filter with the SC filter previously described in literature [7].

2. VOLTAGE-TO-CURRENT CONVERTER

SM circuits process current signals. Therefore, if the input and output signals are voltages rather than currents, v-to-i and i-to-v converters are required. Figure 1 shows a v-to-i converter that can be employed for SM circuits. The bias voltage labeled V_X is determined by a voltage divider composed of the series connection of two identical n-MOS transistors, one connected to the positive supply and the other to the negative supply [2,4]. The gates are connected to V_{DD}. The voltage V_X at the intermediate node of the series association is closer to V_{SS} than to V_{DD}. The v-to-i converter in Figure 1 presents a serious drawback: the allowable negative voltage swing of V_{in} is smaller than the positive voltage swing since V_X is closer to V_{SS} than to V_{DD}. We proceeded to find a structure that avoids this drawback and thus allows us to increase the dynamic range of the filter by a significant amount. The improved v-to-i converter is conceptually shown in Figure 2 and is similar to the proposal in [11].

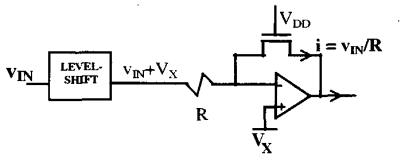

Figure 1. v-to-i converter.

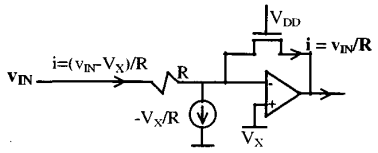

Figure 2. Improved v-to-i converter.

Once the concept of Figure 2 was taken on, we had to come up with a solution to implement the current source $-V_X/R$, which must be independent of technology. Such a circuit is shown in Figure 3. The current $-V_X/R$ flows through R and M_{X1}. With $M_{X1} \equiv M_{X2}$, the current through M_{X2} is also $-V_X/R$, because the two transistors are under the same set of potentials.

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The full v-to-i converter is presented in Figure 4. Figure 5 shows the simulation of the circuit in Figure 4. SMASH simulator [16] together with BSIM 3v3 model for MOSFETs was used for simulations. A sine wave voltage whose DC offset is zero applied to the input resulted in a sinusoidal current through M_F whose DC component is also equal to zero. Note that the current source that has been included in the v-to-i converter can be applied to any technology and its relative accuracy relies on matching and opamp properties.

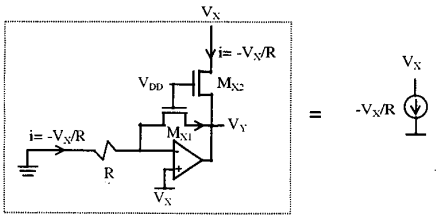

Figure 3. Current source $-V_X/R$ for the v-to-i converter.

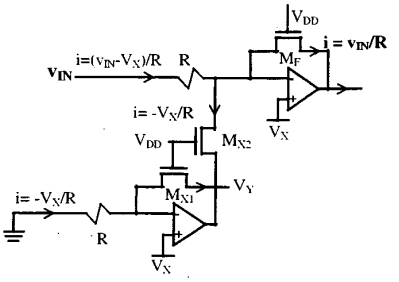

Figure 4. Complete circuit of the v-to-i converter.

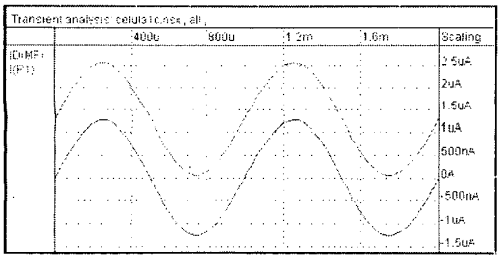

Figure 5. Waveforms for the v-to-i converter of Figure 4.

3. THE SM SYSTEM

The full SM system consists of a voltage-to-current converter, a current-processing unit (which can have one or more elementary integrators/delay blocks) and a current-to-voltage converter. Figure 6 presents the simplest SM system, where the processing unit is composed of a single delay cell.

With the proposed v-to-i converter shown in Figure 4, all operational amplifiers of the SM technique operate at constant common mode voltage, which is close to V_{SS}. Therefore, the design of the input stage of the opamp is considered simplified and even a simple Miller-compensated opamp can operate at 1.5V supply voltage. However, we decided to choose the PMOS input stage, cascode and Miller output opamp in Figure 7 [11] for two reasons: i) its gain and bandwidth are larger than those of the Miller-compensated opamp; and ii) it is able to operate at supply voltages as low as 1V [11]. The opamp in Figure 7 was designed using the equations of the current-based ACM model [12], which are written in terms of the transistor current density. Table 1 presents specifications for the SM filter design.

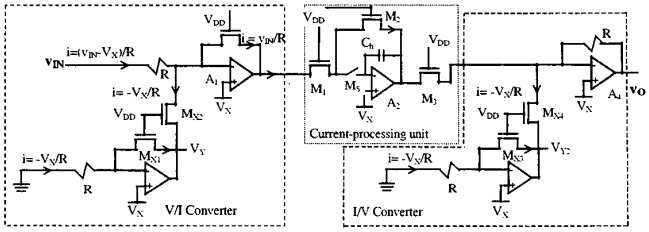

Figure 6. SM system where the current-processing unit is implemented by a 1st-order S/H.

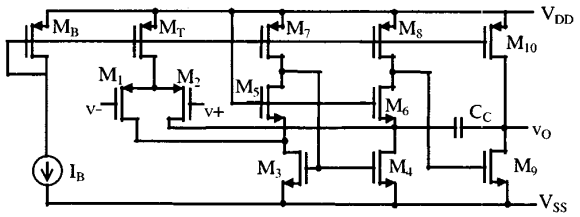

Figure 7. Low-voltage class A opamp [11].

Table 1. Specifications for opamp and filter design.

Supply Voltage	1.5V
Maximum input voltage swing	1V
Resistor for v-to-i conversion (working current per load unit)	400kΩ 1.25μA
SM transistors Switches ($R_{transistors}/R_{switches}$)	10μm/20μm 2μm/0.8μm 5
Hold capacitors, C_h	5pF
Opamp compensating capacitor	C_C= 1.2pF
Sampling frequency, f_S	64kHz
Opamp GBW	≥ 1MHz

The choice of some of the parameters in Table 1 was based on factors such as settling time, charge injection and noise [6].

In the sequel, an analysis of the SM system concerning noise and dynamic range will be carried out

3.1 Noise / Dynamic range

Both the sampled/held noise and the broadband (thermal + flicker) noise [6,13-14] contribute to total noise. As the sampled/held noise is the dominant one in our design [6], only this noise will be considered in the analysis that follows.

Regarding sampled/held noise, the simplest SM system in Figure 6 has only one capacitor. Using the values in Table 1, we have:

$$v_{n\_s/h}^2 = \frac{kT}{C_h} = \frac{kT}{5pF} \quad \Rightarrow \quad v_{n\_s/h(rms)} = 29\mu V$$

And, therefore, for the sampled/held noise in the load (M3, Figure 6), small signal analysis (AMS 0.8 technology):

$$i_{n\_s/h(rms)} = v_{n\_s/h(rms)} g_{ds} = 29\mu V.17\mu S = 493pA$$

Using a working current I_{work} = 1.25μA peak, we have for the sample/hold circuit:

$$DR_{s/h} = 65dB$$

4. THE SM FILTER

Aiming at the implementation of a filter with the characteristics as stated in section 1, we chose to use a universal SM biquad [3], as shown in Figure 8. For the desired bandpass (BP) filters, input $K_2 i_{in}$ is the only one to be used. This input needs to be sampled/held before being applied to the filter.

As can be seen in Figure 8, the opamps of the filter do not drive the same number of transistors. So, opamps with different output stages have been used for this application. Preprocessing (v-to-I converter and S/H circuit) and postprocessing (i-to-v converter) circuits were connected to the BP filter to compose the whole SM system, which has 9 opamps.

Parameters a_1 and a_2 in Figure 8 are implemented with 8-bit MOCDs (with the same digital word) to allow for the adjustment of the center frequency. The schematic of an MOCD together with its symbol are shown in Fig. 9. The output current of the MOCD is a digitally controlled fraction '**a**' of the input current. The symbol $\phi_e.a_2$ ($\phi_o.a_1$) means that the digital word "a_2" ("a_1") is ANDing with clock ϕ_e (ϕ_o) to implement the switching of the MOCD. That is, when ϕ_e is HIGH the output current of $MOCD_1$ is a fraction (a_2/a_{max}, a_{max} is an 8-bit digital word equivalent to 2^{8-1}) of its input current. Conversely, when ϕ_e is LOW, the output current of $MOCD_1$ is zero. The same applies to ϕ_o and $MOCD_2$.

Gain control is achieved by the substitution of M_{LOAD} by an MOCD. The quality factor (Q) can be adjusted by f and K_2, which are MOCDs controlled by the same digital word.

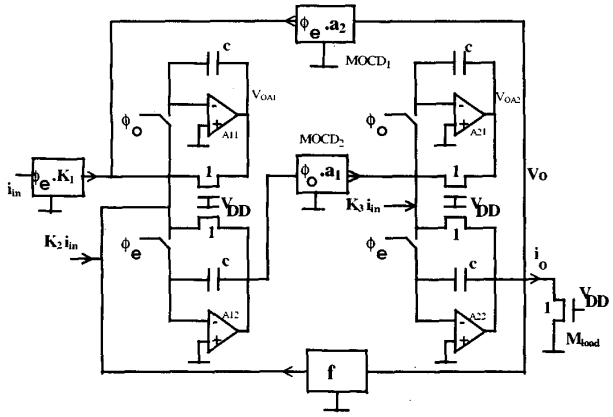

Figure 8. Universal SM biquad.

Several simulations of the complete network were run in SMASH [16]. Some simulation results are shown in Figures 10 and 11. The MOCDs were adjusted for a center frequency f_0 equal to 600Hz. Even though the simulation shows a center frequency 15% below its nominal value, this difference is of no concern because the actual digital word (and center frequency) has to be adjusted for each hearing aid device, according to the needs of the patient.

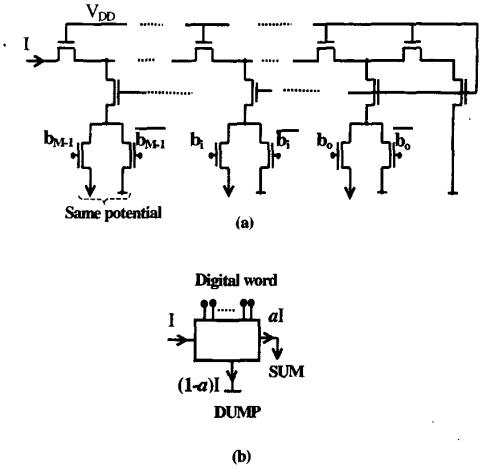

Figure 9. The MOCD circuit scheme and its symbol.

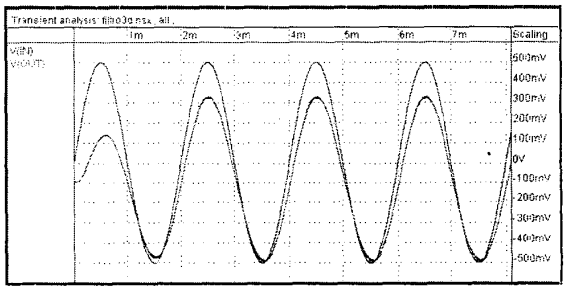

Figure 10. Time response of the bandpass filter (MOCDs adjusted for f_0=600Hz) to a 500mVpeak/500Hz sine wave input.

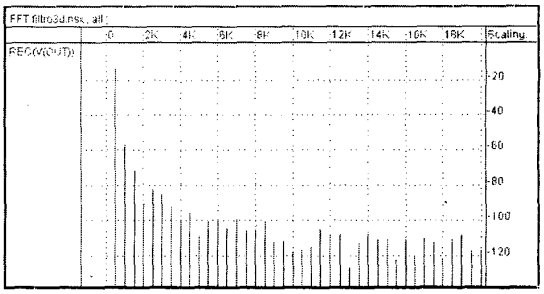

Figure 11. Fourier spectrum of the time response of the bandpass filter (MOCDs adjusted for f_0=600Hz) to a 500mVpeak/500Hz sine wave input.

The values for the ratio signal/THD are 42.8dB for the 500mVpeak input signal and 47dB for the 100mVpeak. For the simulations we have assumed the transistors to be matched and

the circuit to be single-ended. The fully-balanced filter of [7] showed a 42dB measured signal-to-distortion ratio for a 20mVpeak input signal. The simulated power consumption of the programmable SM filter (full system) presented in this paper is 78μW.

5. CONCLUSIONS / DISCUSSION

The SM technique is adequate for the implementation of programmable filters at low-voltage supply. It does not need either special processes or voltage doubler (presenting thus the capability to thrive in a low-voltage environment), and also allows independent digital programming of the filter center frequency (f_0), quality factor (Q) and gain. Programming is not area demanding. The filter power consumption is a little higher then the one of [7] (see Table 2 below). However, we can exchange power consumption for dynamic range. Moreover, the SM filter will have considerably lower power consumption if class-AB opamps are employed. The values of distortion calculated from simulations have not taken into account transistor mismatch, but were obtained for a single-ended circuit. The distortion levels of the SM filter are expected to decrease in a fully-balanced implementation.

Table 2. Specifications of the SC filter of [7] and the SM filter of this work.

	Filter of [7]	SM Filter
DR	63dB	65dB
Opamp power consumption	6μW	6.5μW
Filter power consumption	20μW – filter only	78μW – Full system with class-A opamps
Signal/THD	42dB@ 20mV (balanced, measured)	42.8dB @500mV 47dB @100mV (single-ended, simulated)
Programming	Capacitor bank. Area demanding. Only f_0 and gain (3bits).	MOCD. Small area. f_0, Q and gain (8bits).
Voltage doubler	YES	NO

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