João Vitor Testi Ferreira

ANALYSIS, DESIGN AND TEST OF ULTRA-LOW-VOLTAGE CMOS RING OSCILLATORS

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Prof. Dr. Bartolomeu Ferreira Uchoa-Filho
Coordenador
Universidade Federal de Santa Catarina, UFSC

Prof. Dr. Carlos Galup-Montoro
Orientador
Universidade Federal de Santa Catarina, UFSC

Banca Examinadora:

William Prodanov, Ph.D.
Chipus Microeletrônica S.A.

Fabian Leonardo Cabrera Riaño, Prof. Dr.
Universidade Federal de Santa Catarina, UFSC

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Se você quiser...
se você se esforçar...
se você treinar...
se você entrar de cabeça...
se você se concentrar...
nada garante que vai dar certo.

(Craque Daniel, 2018)

RESUMO

Este trabalho disserta sobre os limites físicos da mínima tensão de operação de osciladores em anel. Existem dois objetivos principais neste trabalho. O primeiro objetivo é o de comparar diferentes topologias de osciladores em anel e avaliar qual delas funciona com a menor tensão de alimentação. O segundo objetivo é propor uma nova topologia de oscilador em anel utiliando a técnica de bootstrap. Esta técnica é (idealmente) capaz de fazer um oscilador em anel oscilar a uma amplitude de 5 V_{DD} quando alimentado com uma tensão de V_{DD}. São apresentados modelos estáticos e dinâmicos para duas células básicas de osciladores em anel (inversor e Schmitt Trigger). O ganho mínimo necessário para o funcionamento de um oscilador também é modelado. São apresentados os resultados das mínimas tensões de amplificação para o inversor (36 mV) e para o Schmitt Trigger (31.5 mV). Um chip teste de tecnologia CMOS 130 nm foi confeccionado para validar os modelos apresentados. Para o Schmitt Trigger e o inversor foram medidas tensões mínimas de oscilação de 48 e 53 mV, respectivamente. É apresentada também a técnica de dual gate que tem como objetivo aumentar o ganho de um amplificador operando em baixa tensão. Por último é apresentada a técnica de projeto de osciladores em anel usando bootstrap que tem como objetivo aumentar a amplitude de oscilação do oscilador.

Palavras-chave: Oscilador em anel. Bootstrap. Dual Gate. Inversor. Schmitt Trigger

ABSTRACT

This work discusses the physical limits of the minimum operating voltage of ring oscillators. There are two main objectives in this work. The first objective is to compare different topologies of ROs and evaluate which of them works with the minimum supply voltage. The second objective is to propose a novel bootstrapped RO topology. This bootstrapped RO is (ideally) capable to oscillate at an amplitude of 5 V_{DD} when supplied with a voltage of V_{DD}. Static and dynamic models are presented for two basic ring oscillator cells (inverter and Schmitt Trigger). The minimum gain required to start an oscillator is also modeled. The minimum amplification voltages for the inverter (36 mV) and for the Schmitt Trigger (31.5 mV) are presented. A 130 nm technology test chip was sent to fabrication to validate the models presented. For the Schmitt Trigger and the inverter, minimum oscillation voltages of 48 and 53 mV, respectively, were measured. The dual gate technique is also presented. This technique aims to increase the gain of an amplifier operating at low voltage. Finally we present the ring oscillator design technique using bootstrap that aims to increase the oscillation amplitude of the oscillator.

Keywords: Ring Oscillator. Bootstrap. Dual Gate. Inverter. Schmitt Trigger

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LIST OF ABBREVIATIONS

AC	Alternate Current
ACM	Advanced Compact Model
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
EH	Energy Harvesting
INV	Inverter
INVB	Dual Gate Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ODE	Ordinary Differential Equation
RO	Ring Oscillator
ST	Schmitt Trigger
STB	Dual Gate Schmitt Trigger
TEG	Thermoelectric Generator
UCCM	Unified Charge-Control Model
WI	Weak Inversion
WSN	Wireless Sensor Network

LIST OF SYMBOLS

C'_{ox}	Oxide Capacitance per Unit Area
g_{mb}	bulk transconductance
g_{md}	drain transconductance
g_{mg}	gate transconductance
g_{ms}	source transconductance
i_f	Forward Inversion Level
i_r	Reverse Inversion Level
I_D	Drain Current
I_F	Forward Current
I_0	Transistor Force
I_R	Reverse Current
I_S	Specific Current
L	Transistor Channel Lenght
n	Slope Factor
q'_{ID}	normalized inversion charge densities at drain
q'_{IS}	normalized inversion charge densities at source
V_B	bulk voltage
V_D	drain-to-bulk voltage
V_{DD}	Supply Voltage
V_{DS}	drain-to-source voltage
V_G	gate-to-bulk voltage
V_P	pinch-off voltage
V_S	source-to-bulk voltage
V_{T0}	zero-bias threshold voltage
W	Transistor Channel Width
μ	Carrier Mobility
ϕ_t	Thermal Voltage

CONTENTS

1 INTRODUCTION

There are several applications were a device's power supply is limited. This could be the case in mobile devices (like a smartphone) or in mechanisms where the battery is not easily accessible (like a pacemaker). In these applications, the development of wireless sensor nodes (WSNs) is of remarkable importance. In such appliances the device should be capable to operate without charging or changing its battery for the largest possible time. This motivates the research of energy harvesting (EH) systems that can convert energy from the environment into electric energy and can operate as bateryless devices.

The three main sources of ambient energy that can be harvested by an EH system are: mechanical vibrations, light and heat. Each of them have different interfaces from the environment to the circuit and in order to choose between one of them the interested user should take into account parameters like area, available harvested power, application environment characteristics, etc. (1)

There are several classic blocks needed in order to make an EH system work. The specific topology depends largely on the application and transducer used, however all EH systems used in low power applications will need an energy source (transducer), power management and power conversion systems (2).

This work is focused in the power conversion system, specifically in the voltage startup block. This block is mostly used in EH devices where the energy is supplied by a thermoelectric generator (TEG). Usually a TEG can supply 100's of µW of available power but its output voltage is smaller than 100mV for temperature differences of a couple of degrees Celsius.

In the context of EH applications, many power conversion systems have been done making use of a startup block followed by a step-up converter (3) (4) (5) (6). The reason for this is that the startup block provides a kick-start to the step-up converter, making it possible to operate at voltages well below 100mV. In order to produce the startup, 2 topologies are common: one using a LC oscillator and the other using a ring oscillator (RO). Usually the LC oscillator can operate at lower voltages, but it is much more area hungry. Sometimes the inductor can't be integrated and it needs to be placed as an external component.

One of the bottlenecks of using a RO as a startup block is that the minimum operating voltage of the EH system is related to the

minimum operating voltage of the RO. In respect to this, the designer should take some strategies into account. The RO can only oscillate when its basic cells have a gain greater than unity, so choosing a basic cell that has high gain at low voltages is of great interest to the user. It is necessary to use a MOSFET model that can evaluate transistors operating in these low voltages. In this work we use the Advanced Compact MOSFET (ACM) Model to model all the transistors. We chose this model because it uses technological parameters that are easily measurable in different technologies and also because the model is valid at very low operating voltages.

Another approach that can be explored is using the bootstrap technique to make the RO oscillate at a voltage greater than the voltage supplied by the TEG, which could be used as a trade-off in the size needed by the step-up converter to boost the voltage.

1.1 OBJECTIVE

There are two main objectives in this work. The first objective is to compare different topologies of ROs and evaluate which of them works with the minimum supply voltage. This objective is more concerned in discovering the physical limitations than trying to find evident applications for this ROs. The second objective is to propose a novel bootstrapped RO topology. This bootstrapped RO is (ideally) capable to oscillate at an amplitude of 5 V_{DD} when supplied with a voltage of $V_{DD.}$

1.2 ORGANIZATION

There are two main topics in this work (minimum RO supply voltage and bootstrapped ROs), so they will be treated at different parts in the text. The work is divided into five chapters. Chapter 1 is this brief introduction containing the context and objective of this work. Chapter 2 serves as background theory for the reader. This chapter contains the minimum theory and most important results to comprehend the rest of this work. Chapter 3 contains simulations and practical results regarding the minimum voltage of operation for ROs. This is the core section of this work. Chapter 4 is the presentation of a new topology to design ROs. Chapter 5 contains the conclusions of this work.

2 MINIMUM OPERATING VOLTAGE OF A RING OSCILLATOR

The study of the minimum operating voltage of a basic cell is primarily justified by the research of ultra-low voltage circuits (7). According to (8), the minimum voltage necessary to make a CMOS inverter (figure 1) have a gain greater than unity is

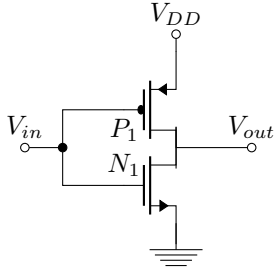
$$V_{dd}(min) = 2.ln(2).\phi_t \tag{2.1}$$

where ϕ_t is the thermal voltage (25.9 mV at 300 K). At room temperature the minimum supply voltage to obtain unity gain using a CMOS inverter would be approximately 36 mV. This value is not a fundamental limit of the CMOS technology. It is just a special case for the CMOS inverter. This result can also be derived from the study of the CMOS inverter in weak inversion (WI). Using the Schmitt Trigger (ST) can lead to a lower minimum supply voltage to obtain unit gain, as is demonstrated in the work of (9). The study of (9) demonstrated that ST, under ideal conditions, can have unity gain at voltages as low as 31.5 mV (at room temperature).

2.1 THE ADVANCED COMPACT MOSFET (ACM) MODEL

The ACM model is a charge based MOSFET model (10). In this study our main focus will be the MOSFET operating at very low supply voltages, thus in weak inversion (WI). Throughout this section we will first present the main expressions for the behavior of the drain

Figure 1 – CMOS Inverter



Source: the author

current I_D in WI. In a second moment, a simple model for the MOSFET transcondutances will be presented. The DC behavior and the transconductances are important in the process of deriving the minimum supply voltage to obtain unity gain.

2.1.1 MOSFET Transistor Operating in WI

The ACM model gives the drain current I_D of the MOSFET transistor in terms of its forward (I_F) and reverse (I_R) components as

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{2.2}$$

where i_f and i_r are the forward and reverse inversion levels, respectively, and I_S is the specific current given by

$$I_S = \frac{1}{2}\frac{W}{L}\mu C'_{ox} n \phi_t^2 \tag{2.3}$$

where W is the channel width, L is the channel length, μ is the carrier mobility, C'_{ox} is the oxide capacitance per unit area and n is the slope factor.

Expressing the inversion levels in terms of the normalized inversion charge results in

$$i_{f(r)} = [q'_{IS(D)} + 1]^2 - 1, \tag{2.4}$$

where q'_{IS} and q'_{ID} and the normalized inversion charge densities at source and drain, respectively.

The relation between the normalized charge densities and voltages, called the Unified Charge-Control Model (UCCM) (11) is given as

$$\frac{V_P - V_{S(D)}}{\phi_t} = q'_{IS(D)} - 1 + ln[q'_{IS(D)}] \tag{2.5}$$

where V_S and V_D are the source-to-bulk and drain-to-bulk voltages, and V_P is the pinch-off voltage defined as

$$V_P \approx \frac{V_G - V_{T0}}{n} \tag{2.6}$$

with V_G being the gate-to-bulk voltage and V_{T0} the zero-bias threshold voltage.

Subtracting V_D from V_S in (2.5) we have

$$\frac{V_{DS}}{\phi_t} = q'_{IS} - q'_{ID} + ln(\frac{q'_{IS}}{q'_{ID}}), \tag{2.7}$$

Deep in WI $q'_{IS(D)} \to 0$, then

$$\frac{V_{DS}}{\phi_t} \approx ln(\frac{q'_{IS}}{q'_{ID}}) \Rightarrow \frac{q'_{IS}}{q'_{ID}} = e^{\frac{V_{DS}}{\phi_t}} \tag{2.8}$$

Relation (2.8) will be important when analyzing the minimum supply voltage of the CMOS inverter.

Rearranging (2.4) and substituting it in (2.5) we obtain

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + ln[\sqrt{1 + i_{f(r)}} - 1] \tag{2.9}$$

Deep in WI $i_{f(r)} \to 0$. In this condition the square root term in $i_{f(r)}$ becomes negligible and we can approximate the logarithmic term using $\sqrt{1+x} \approx 1 + \frac{x}{2}$ in 2.9 resulting

$$\frac{V_P - V_{S(D)}}{\phi_t} = -1 + ln[\frac{i_{f(r)}}{2}] \Rightarrow i_{f(r)} = 2e^{1+\frac{V_P - V_{S(D)}}{\phi_t}} \tag{2.10}$$

Substituting (2.10) into (2.2) and using the pinch-off voltage approximation (2.6) results in

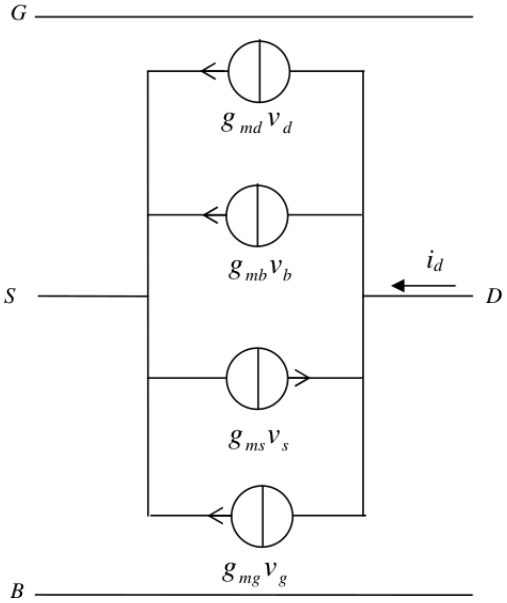
$$I_D = I_x \left[\exp\left(\frac{V_G - nV_S}{n\phi_t}\right) - \exp\left(\frac{V_G - nV_D}{n\phi_t}\right)\right] \tag{2.11}$$

$$I_x = \mu \frac{W}{L} C'_{ox} {\phi_t}^2 \exp\left[1 - \frac{V_T - (n-1)V_B}{n\phi_t}\right] \tag{2.12}$$

Equation (2.11) is the drain current I_D for a MOSFET transistor operating at WI. It is important to observe that the transistor obeys an exponential law instead of the quadratic law encountered when working in strong inversion ($i_f >> 1$).

Since in this work we are concerned with the minimum voltage to obtain gain in a MOSFET transistor, next section presents a simple model for the transconductances of this device operating in WI.

Figure 2 – Transconductance model for a MOSFET transistor considering its 4 terminals



Source: (12)

2.1.2 Transconductance model in WI

As the MOSFET transistor is a 4-terminal device, the voltage variation in each of its terminals will contribute to the variation in its drain current (I_D). In order to model these changes, 4 transconductances are necessary as depicted in Figure 2. These transconductances are modelled as:

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B \tag{2.13}$$

where

$$g_{mg} = \frac{\partial I_D}{\partial V_G}, g_{ms} = -\frac{\partial I_D}{\partial V_S}, g_{md} = \frac{\partial I_D}{\partial V_D}, g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{2.14}$$

are the gate, source, drain and bulk transconductances, respectively. Applying the definition of g_{ms} and g_{md} (2.14) to (2.11) we have

$$g_{ms(d)} = 2\frac{I_S}{\phi_t}\frac{i_{f(r)}}{2} \Rightarrow g_{ms(d)} = \frac{I_{F(R)}}{\phi_t} \tag{2.15}$$

which is very similar to the Bipolar Junction Transistor (BJT) transconductance. This result was expected since, in this operating region, both transistors obey an exponential law.

The expression for g_{mg} can be deduced from its definition (2.13)and (2.2)

$$g_{mg} = I_S\frac{\partial(i_f - i_r)}{\partial V_G} \tag{2.16}$$

Noting from (2.10) that

$$\frac{\partial i_{f(r)}}{\partial V_P} = -\frac{\partial i_{f(r)}}{\partial V_{S(D)}} \tag{2.17}$$

and using relation (2.6) to obtain

$$\frac{\partial V_P}{\partial V_G} = \frac{1}{n} \tag{2.18}$$

we can evaluate the expression of g_{mg} as

$$g_{mg} = \frac{g_{ms} - g_{md}}{n} \tag{2.19}$$

The bulk transconductance g_{mb} can derived using (2.13). If we take the special case where all the terminals of a MOSFET increase the voltage by the same amount, the change in I_D would be 0. In other words

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0 \tag{2.20}$$

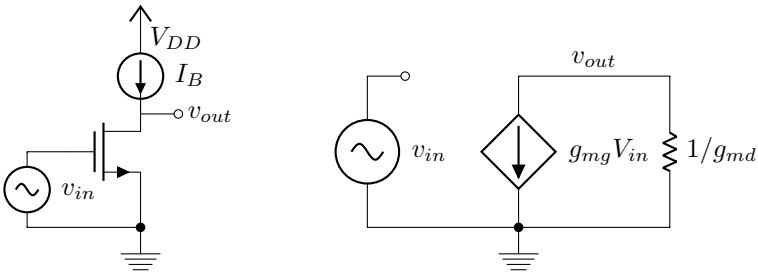
Rearranging (2.20) and substituting the right hand side of (2.19) results in

$$g_{mb} = (n-1)g_{mg} \tag{2.21}$$

More details about the ACM model can be found in (12)

Next section presents the derivation of the minimum supply voltage to obtain gain from a CMOS inverter using the transconductance model derived in this section.

Figure 3 – Small-Signal Model For Common Source Amplifier



Source: the author

2.2 MINIMUM SUPPLY VOLTAGE TO OBTAIN UNITY GAIN WITH A CMOS INVERTER

Considering the low frequency small-signal model for a common-source amplifier depicted in figure 3 and using (2.19) we have

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{g_{mg}}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right) \tag{2.22}$$

Finally, using (2.15) we have

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{1}{n}\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right) \tag{2.23}$$

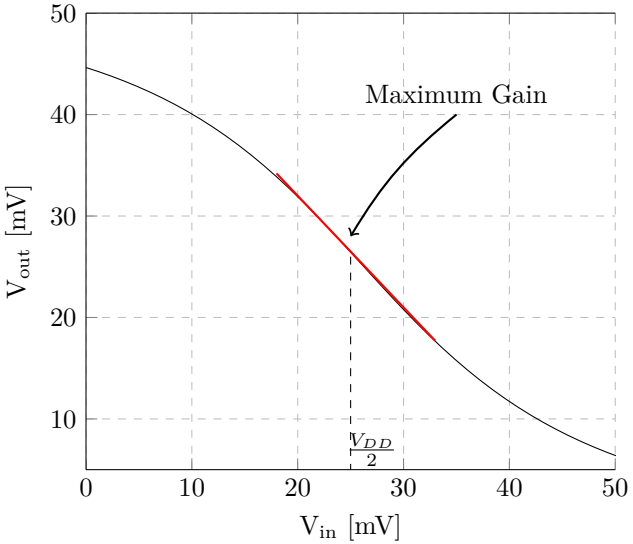
The next step in this analysis would be to transpose the result of (2.23) to the case of the CMOS inverter depicted in Figure 1. Considering the NMOS and PMOS balanced (i.e. their I_0 (2.12) has the same numerical value), by symmetry, we see that, when the input voltage v_{in} is at $V_{DD}/2$, the v_{out} will also be at $V_{DD}/2$. This is the point of maximum gain of a balanced amplifier as depicted in Figure 4. Using this constraint, at the maximum gain point $V_{DS} = V_{DD}/2$. Using it in (2.23)

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{e^{\frac{V_{DD}}{2\phi_t}} - 1}{n} \tag{2.24}$$

For a gain $\mathrm{v_{out}}/\mathrm{v_{in}} = 1$ and considering $\mathrm{n} = 1$ we obtain (2.1). In typical CMOS technologies the value of n is in the range of 1.1 and 1.3 making the voltage necessary to obtain unity gain slightly bigger.

It is worthwhile noting that the critical point in this analysis was

Figure 4 – Transfer Function of a CMOS inverter operating in WI



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that the NMOS and PMOS in the inverter were balanced. When using and unbalanced amplifier the gain will tend to decrease, since V_{DS} will be smaller in one of the transistors. This result is depicted in Figures 5 and 6, where a CMOS inverter is simulated in different corners. It can be noted that the best result is achieved in typical conditions (the amplifier was designed to be balanced in typical parameters).

The result of (2.1) contrasts with the study of (13) in which the theoretical limit of a Schmitt Trigger (ST) was calculated to be around 31.5mV. The reason for this smaller voltage is the presence of positive feedback that increases the gain of the basic cell. This positive feedback can be done using a different number of topologies. A study comparing this topologies will be presented at section 3. For the time being, it is important to point out that only 2 ST topologies were studied in this work: the classic 6T and the ST with gate and bulk connected. The study of the static and dynamic characteristic of the circuit will be presented in the following sections.

Figure 5 – Transfer Function of a CMOS Inverter in Different Corners

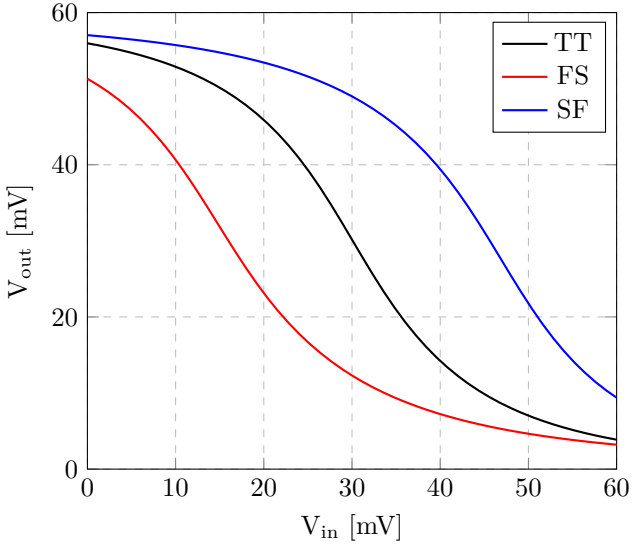

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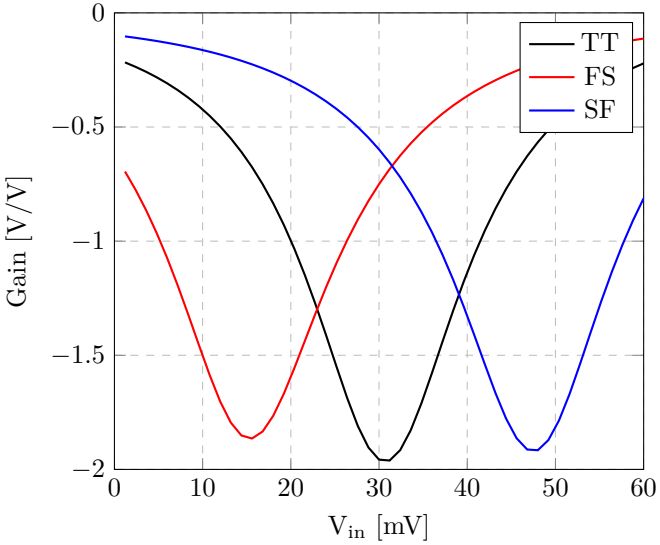
Figure 6 – DC Gain of a CMOS Inverter in Different Corners



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2.3 DC MODEL OF THE SCHMITT TRIGGER

The classic 6T ST is presented in figure 8. Its small signal voltage gain A_V, as calculated in (2.25), is a function of the ST transconductance G_m and its output conductance G_o.

$$A_V = \frac{G_m}{G_o} \tag{2.25}$$

This circuit was extensively studied in the work of (13). The Schmitt trigger small signal parameters are complex functions (2.26 and 2.27) resulted from the positive feedback. Depending on the transistor geometries and operation conditions as supply voltage and temperature, the Schmitt trigger output voltage can or can not show hysteresis, which results in a negative small signal conductance.

$$G_m = 2 \cdot \frac{g_{mg1}(g_{ms2} + g_{md0}) + g_{ms1}g_{mg0}}{g_{ms1} + g_{ms2} + g_{md0}} \tag{2.26}$$

$$G_o = 2 \cdot \frac{g_{md1}(g_{ms2} + g_{md0}) - g_{ms1}g_{mg2}}{g_{ms1} + g_{ms2} + g_{md0}} \tag{2.27}$$

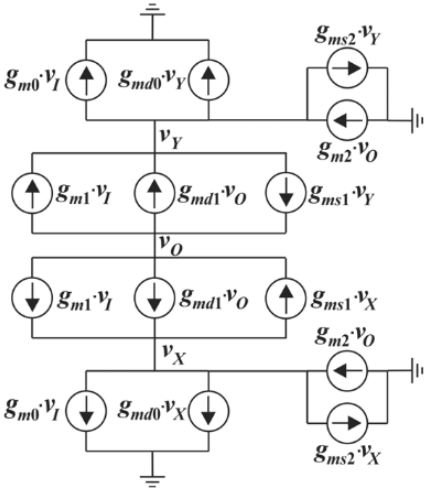
Schmmit trigger operation is rigorously described in (13), although it does not consider bulk biasing. Figure 7 represents the small-signal model of the Schmitt Trigger with matched n and p networks.

In order to include bulk biasing, the ACM transistor model for weak inversion (2.11) used here will consider a slope factor n greater than one. This way, the body terminal voltage V_B can be used to control the otherwise constant current I_x, as shown in (2.12).

Every transconductance used to calculate the small signal voltage gain A_V is presented in Table 1. They can be expressed by their respective transistor strengths I_x and the factors α and β. The factor α is an exponential function of the ratio between the supply voltage V_{DD} and thermal voltage ϕ_t, while the factor β itself is a function of α. Both factors are expressed in (2.28) and (2.29).

$$\alpha = \exp\left(\frac{V_{DD}}{2\phi_t}\right) \tag{2.28}$$

Figure 7 – Small-signal model of the Schmitt Trigger with matched n and p networks



Source: (13)

	$g_{ms}\phi_t$	$g_{md}\phi_t$	$g_{mg}n\phi_t$
$N(P)_0$	$\alpha^{1/n}I_0$	$\alpha^{1/n}\beta I_0$	$\alpha^{1/n}(1-\beta)I_0$
$N(P)_1$	$\alpha^{1/n}\beta I_1$	$\alpha^{-(n-1)/n}I_1$	$\alpha^{1/n}(\beta-\alpha^{-1})I_1$
$N(P)_2$	$\alpha^{1/n}\beta I_2$	$\alpha^{-(2n-1)/n}I_2$	$\alpha^{1/n}(\beta-\alpha^{-2})I_2$

Table 1 – Schmitt Trigger small signal transconductances

$$\begin{aligned}\beta &= \exp\left(-\frac{V_x}{\phi_t}\right)\\ &= \frac{I_0 + I_1\left[\exp\left(\frac{V_{DD}}{2\phi_t}\right)\right]^{-1} + I_2\left[\exp\left(\frac{V_{DD}}{2\phi_t}\right)\right]^{-2}}{I_0 + I_1 + I_2}\\ &= \frac{\alpha^2 I_0 + \alpha I_1 + I_2}{\alpha^2(I_0 + I_1 + I_2)}\end{aligned} \tag{2.29}$$

Considering that every transistor operates in weak inversion and

in the linear region, the transconductance G_m and output conductance G_o can be calculated as function of α and β, as shown in (2.30) and (2.31).

$$\begin{aligned} G_m &= \frac{2\alpha^{1/n}(\beta - \alpha^{-1})I_1[I_0 + (2-\beta)I_2]}{n\phi_t(I_0 + I_1 + I_2)} \\ &\approx \frac{2\alpha(\beta - \alpha^{-1})I_1[I_0 + (2-\beta)I_2]}{\phi_t(I_0 + I_1 + I_2)} \end{aligned} \tag{2.30}$$

$$\begin{aligned} G_o &= -\frac{2\alpha^{-(n-1)/n}I_1[\alpha^{1/n}\beta I_2 - n(I_0 + I_2) - \alpha^{-(2n-1)/n}I_2]}{n\phi_t(I_0 + I_1 + I_2)} \\ &\approx -\frac{I_1[2\alpha\beta I_2 - (I_0 + I_2) - \alpha^{-1}I_2]}{\phi_t(I_0 + I_1 + I_2)} \end{aligned} \tag{2.31}$$

Substituting the values encountered in (2.30) and (2.31) in the expression (2.25) we have the small-signal gain of the ST as

$$A_v = \frac{2\alpha(\beta - \alpha^{-1})I_1[I_0 + (2-\beta)I_2]}{I_1[2\alpha\beta I_2 - (I_0 + I_2) - \alpha^{-1}I_2]} \tag{2.32}$$

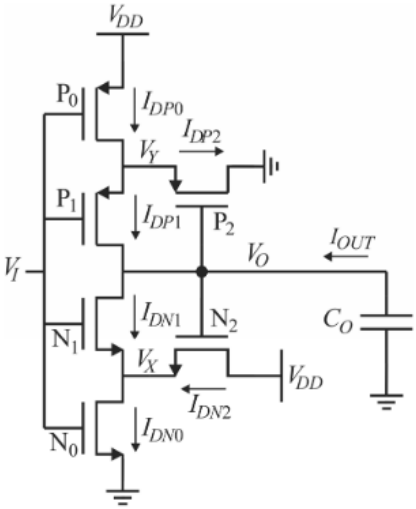
Using the simplification $n = 1$, (13) plotted the DC transfer function for $V_{DD} = 150mV$ and $V_{DD} = 60mV$ (figure 9).

As we can see from Figure 9, there is a clear hysteresis region when the ST is supplied with a voltage of 150mV. When the voltage supply is switched to 60mV the cell behaves like an amplifier (there is no hysteresis region). This suggests that as the supply voltage is decreased the hysteresis becomes smaller and there is a supply voltage where the hysteresis region will disappear. This minimum supply voltage was also estimated in the work of (13).

2.3.1 Minimum Hysteresis Supply Voltage for a Schmitt Trigger

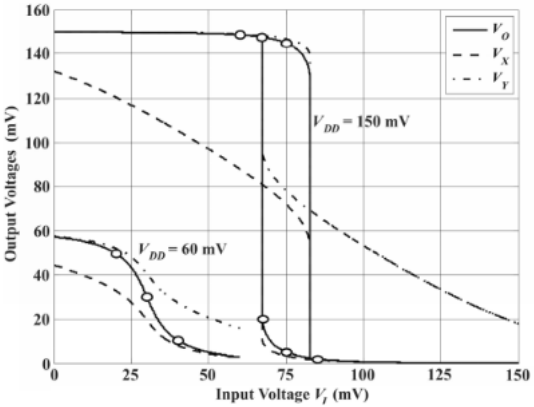
A ST comparator can be interpreted as an amplifier with infinity gain. If we start to increase more and more the gain of an amplifier, it will tend to approach the behavior of a comparator. By the time we achieve the comparator behavior, if we try to increase even more the gain, the cell will start to have a hysteresis region. This is depicted in figure 10.

Figure 8 – Classic 6T Schmitt Trigger



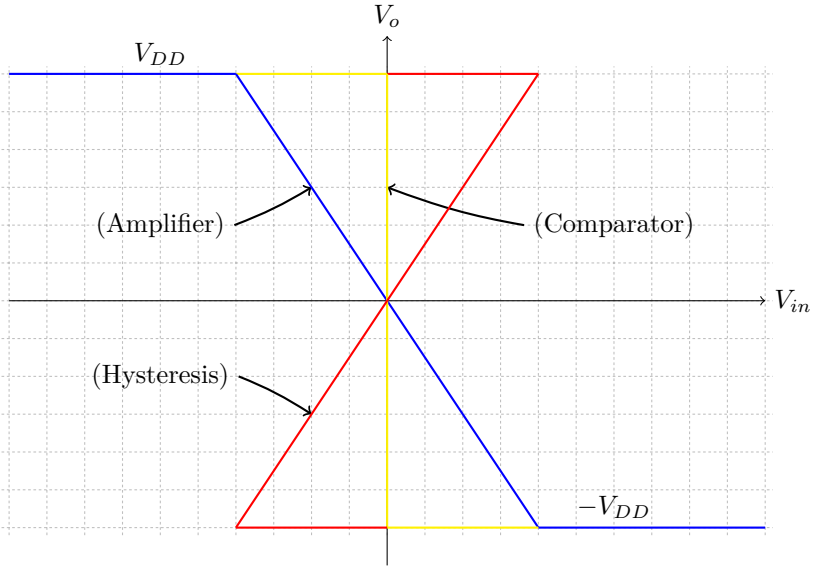
Source: (13)

Figure 9 – DC transfer function of the Schmitt Trigger



Source: (13)

Figure 10 – Transfer function of a increasing gain amplifier



Source: the author

The minimum hysteresis supply voltage will happen when the small-signal gain (2.32) tends to infinity. When the denominator of (2.32) equals zero we have the minimum supply voltage to obtain hysteresis. After some algebra we can approximate the result as

$$V_{DDH} \approx 2\phi_t ln(2 + \frac{I_2}{I_0} + \frac{I_0}{I_2} + \frac{I_1}{I_2}) \tag{2.33}$$

The minimum voltage supply necessary to obtain hysteresis is obtained when $I_2/I_0 = 1$ and $I_1/I_2 = 0$. Using the exact value calculated in (13) we obtain:

$$V_{DDHmin} = 2\phi_t ln(2 + \sqrt{5}) = 75mV@300K \tag{2.34}$$

This result represents a physical limit to obtain hysteresis using this topology and also indicates the optimal project to obtain hysteresis at very low voltages. To achieve this goal transistors $N(P)_0$ and $N(P)_2$ should have the same aspect ratio while transistor $N(P)_2$ should be kept much stronger than $N(P)_1$.

When working with the ST with a supply voltage that will lead

to hysteresis, it is important to analyze the dynamic response of the cell. The hysteresis region is known to make the cell slower. Appendix 6 provides a simple model for the ST.

Decreasing even more the supply voltage, another point of great interest is the minimum supply voltage to obtain unity gain.

2.3.2 Minimum Supply Voltage to Obtain Unity Gain With a Schmitt Trigger

As commented in the previous section, a 6T ST can only present hysteresis with a voltage supply greater than 75mV. Of course this result can only be approached when the N and P networks are matched, n = 1 and with optimal aspect ratios for the transistors ($I_2/I_0 = 1$ and $I_1/I_2 \rightarrow 0$).

When operating at supply voltages smaller than 75mV the 6T ST will operate as an amplifier. If we start to decrease even more the voltage of this cell, at a certain point it will stop working as an amplifier. This point represents the voltage supply at which the cell presents unity gain. The minimum V_{DD} value necessary obtain $A_v = 1$ can be calculated from (2.32). Since the algebra is quite lengthy, the interested reader is referred to (9). In the next paragraphs a summary of the results are presented.

The minimum supply voltage to obtain unity gain is

$$V_{DDmin} = 2\phi_t ln(\frac{8+\sqrt{73}}{9}) = 31.5mV@300K \tag{2.35}$$

which is obtained considering $n = 1$, matched P and N networks and optimal aspect ratios.

The optimal aspect ratios to maximize the gain for different voltage supplies where calculated as well. As a result I_1 should be much weaker than I_0 ($I_1/I_0 \rightarrow 0$). The optimum relation I_2/I_0 depends on the supply voltage. The optimal value for different supply voltages are presented in Table 2.

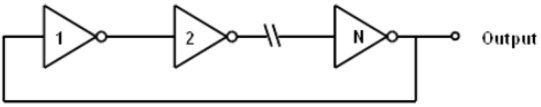
As can be noted from Table 2, the design of the cell with minimum supply voltage to obtain hysteresis is not the same design to obtain unity gain at the lowest voltage.

After calculating the minimum supply voltage to obtain gain in a cell, it is important to model how this gain will affect the RO. Next section contains a model for ROs. This model will be important to estimate the minimum gain of a cell in order to start a RO.

V_{DD}(mV)	Optimum I_2/I_0	Optimum Gain (V/V)
75	1.00	-∞
70	0.91	-20.23
60	0.73	-5.58
50	0.58	-2.76
40	0.44	-1.57
31.5	0.33	-1.00

Table 2 – Optimal I_2/I_0 for different V_{DD}

Figure 11 – Ring Oscillator



Source: the author

2.4 MODEL OF THE RING OSCILLATOR (RO)

The model for the RO, depicted in Figure 11, will be primarily focused on CMOS technologies, where we usually have a high input impedance. In a situation like that, a simple representation of an amplifier stage is depicted in figure 12.

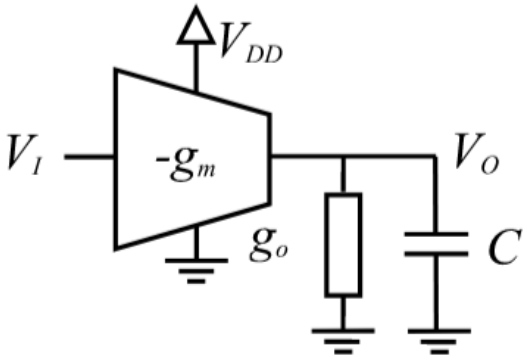
Due to the high level of isolation between stages, the open-loop transfer function G for an N stage RO is

$$G(\omega) = -\frac{A^N}{(1 + j\omega RC)^N} \tag{2.36}$$

where N is the odd number of stages, ω is the angular frequency, R is the inverse of g_o (output conductance), C is the capacitance at the output node and $A = g_m/g_o$ is the absolute gain of a single stage.

In order to achieve the Barkhausen criterion of oscillation (14), the frequency-dependent phase-shift must be π radians, thus each stage contributes π/N. Thus, the oscillation frequency is given by

Figure 12 – CMOS Amplifier model



Source: the author

$$tan^{-1}(\omega_{osc}RC) = \frac{\pi}{N} \tag{2.37}$$

$$\omega_{osc} = \frac{1}{RC} tan\left(\frac{\pi}{N}\right) \tag{2.38}$$

The minimum absolute gain per stage must be such that the magnitude of the loop gain at ω_{osc} is equal to unity, thus

$$A(\omega) = \sqrt{1 + (\omega_{osc}RC)^2} \tag{2.39}$$

Using (2.37) we have

$$A(\omega) = \sqrt{1 + tan^2\left(\frac{\pi}{N}\right)} \approx 1 + \frac{1}{2}\left(\frac{\pi}{N}\right)^2 \tag{2.40}$$

using the approximation $\sqrt{1+x} \approx 1 + \frac{x}{2}$. This an approximate expression for the minimum gain needed to start an oscillator. Expression (2.40) is important since it is a compact equation that predicts the number of stages necessary to start an oscillator at a given gain. Equation (2.40) means that the more stages in a RO, the smaller the unit cell necessary gain to establish an oscillation condition (as expected). Table 3 presents some values of minimum necessary gain to make a RO work with different number of stages.

As can be seen from Table 3 the percentual decrease in necessary gain when moving from 13 to 15 is less than 1% (0.7%). When

N	$1+\frac{1}{2}(\frac{\pi}{N})^2$	N	$1+\frac{1}{2}(\frac{\pi}{N})^2$
3	1.54831	11	1.04078
5	1.19739	13	1.02920
7	1.10071	15	1.02193
9	1.06092	101	1.00048

Table 3 – Minimum necessary gain to make a RO work with different number of stages

moving from 3 stages to 13 stages the decrease is of more than 30% (34.6%). This should be taken in consideration when designing an ultra-low voltage RO, because, in order to increase the gain, the supply voltage should be increased as well (2.23). Making the RO too big (101 stages, for example) produces a marginal decrease in necessary gain to start the oscillator. This consideration is of major importance when designing a RO.

2.5 BULK BIASING TECHNIQUE

An important technique that is used to decrease the minimum voltage necessary to have a gain greater than unity is interconnecting each gate and bulk of the transistors in inverter cells (15). This topology is depicted in Figure 13. This technique is justified by the fact that the transconductance of the amplifier is increased. When the gate is connected to the bulk, the bulk transconductance g_{mb} starts to influence in a positive manner the performance of the amplifier. The small-signal model would be the same as that of figure 3, but now, instead of only g_{mg}, we have $g_{mg} + g_{mb}$. Rearranging (2.21) we have

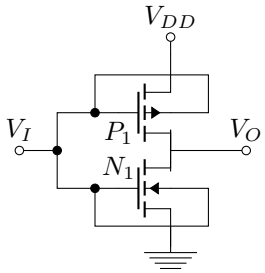
$$g_{mb} + g_m = ng_m \tag{2.41}$$

meaning that: summing g_{mb} to g_{mg} has the same effect of multiplying g_{mg} by n. If we look at equation (2.22), we conclude that the gain of an inverter cell using the bulk biasing technique is multiplied by n, thus

$$A_v = \frac{ng_m}{g_{md}} = e^{V_{DD}/2\phi_t} - 1 \tag{2.42}$$

Summarizing, when using an inverter cell with connected gate

Figure 13 – CMOS Inverter Using Bulk Biasing Technique



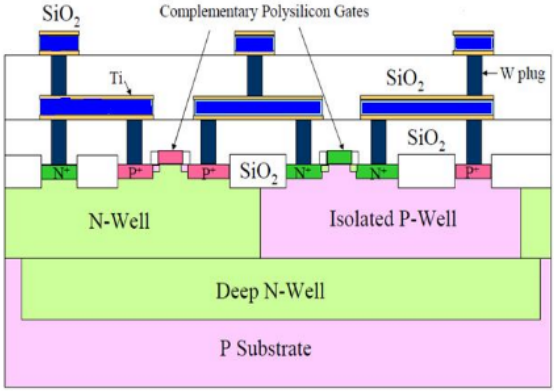
Source: the author

and bulk the attenuation due to the slope factor n will be cancelled. Increasing the unit cell gain by a factor of n (in recent technologies this would correspond to an increase of around 1.3 and 1.5 V/V for the same supply voltage), is a fair enhancement when compared to the classic CMOS inverter. This increase in the gain, together with the study of section 2.4, will serve as the basis to the design of some topologies of RO that can start with minimum supply voltage.

There are some trade-offs when using this technique to design an ultra-low voltage RO. By the time the bulk is added as an input to the RO, its capacitance is added in the delay of the RO as well, which makes the oscillator slower. Increasing the capacitance of the cell will also increase the cell power consumption, since the cell needs more current to drive the parasitic capacitances.

Another point to consider is that connecting the gate and the bulk is not something simple to accomplish in all technologies and usually translates in a big area penalty. It is necessary to have a triple well device available in the technology to have each bulk connected to a different voltage potential. A triple well device isolates the p-well bulk of a NMOS to the die substrate as depict in Figure 14. In the specific case of ROs, it is desirable to put as many CMOS devices as possible in a minimum area. The triple well devices require an extra distance between each other (in order to isolate their voltage potential) which makes the size of the RO bigger.

Figure 14 – Triple Well Device



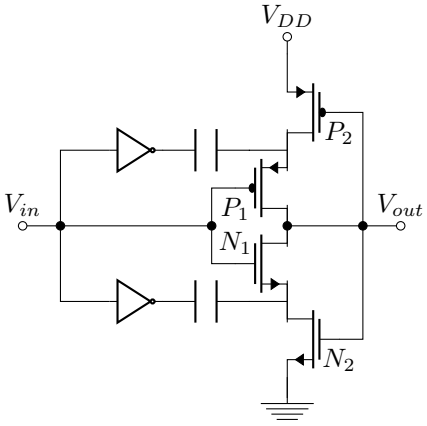
Source: (16)

2.6 BOOTSTRAP TECHNIQUE

The bootstrap technique consists of applying part of the output of an amplifier in its input, in order to alter the input impedance of the gain stage. The main advantage of using this technique is to increase the output swing of the RO. The basic bootstrap topology implemented using the CMOS technology is presented in Figure 15 and was first presented by (17). Remembering that the voltage of a capacitor cannot change instantaneously, we can estimate the voltage at each one of the nodes of the circuit. Another point to consider is that the bootstrap cell is operating in a RO, so the inputs and outputs are continuously changing its states from high to low. This makes the internal capacitors of the cells charge and discharge in a complementary manner. The following paragraphs and the sequence from figure 16 to figure 18 intend to elucidate the basic working principle of a RO oscillator operating with a bootstrap basic cell. In this sequence of figures the symbol 1 means that the node has a voltage of approximately 1 VDD, the symbol 2 in a node would mean 2 VDD and so on.

In Figure 16 the input is assumed to be low while the output is at a high state (considering the opposite case would give a similar result). In this situation transistors N1 and P2 would be off. The lower capacitor would be charged by the lower inverter and transistor N2. The potential of the node source of transistor P1 depends on the

Figure 15 – Bootstrap cell



Source: the author

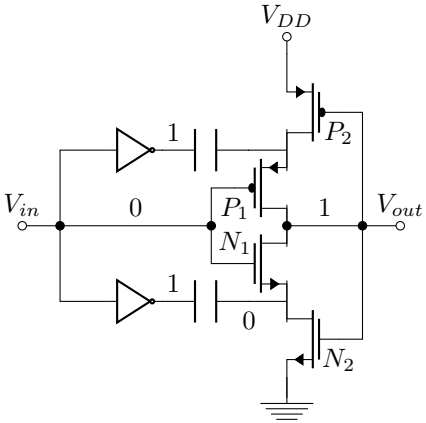
initial condition of the system and in this analysis it was assumed to be indeterminate.

Figure 17 is the following state of the oscillator when the input is assumed to be high while the output is low. In this situation transistors N2 and P1 would be off. The upper capacitor would be charged by the upper inverter and transistor P2. The lower capacitor cannot change its voltage immediately, so, as its left terminal is forced to be 0 by the lower inverter, its right terminal should acquire a voltage of -1. Noting that transistor N1 presents low impedance (it is working at on state), the voltage of the output would be forced to -1.

In the next state we see in figure 18 the input is assumed to be low while the output is high. In this situation, as in figure 16, transistors N1 and P2 would be off. The upper capacitor is charged by the upper inverter and transistor P2. The upper capacitor cannot change its voltage immediately, so, as the upper inverter is forcing a voltage of 1, the other side of the capacitor should acquire a voltage of 2. Noting that transistor P1 presents low impedance (it is working at on state), the voltage of the output would be forced to 2.

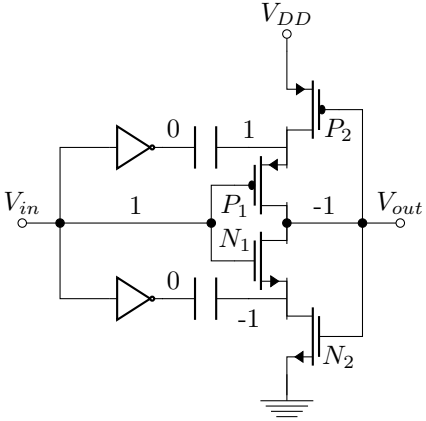
This analysis showed that, in the ideal case, the output swing of the ring oscillator would be around 3 VDD (from -VDD to 2VDD). This output swing can be further increased at the cost of area by using more capacitors as will be showed in the proposed circuit in section 4.1. The total area penalty would be of 2 capacitors and 6 transistors at each RO stage.

Figure 16 – Bootstrap cell - N network charge



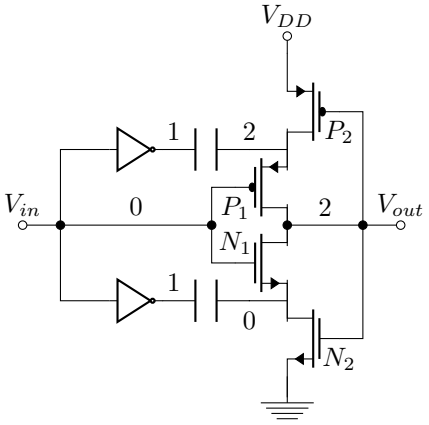
Source: the author

Figure 17 – Bootstrap cell - P network charge



Source: the author

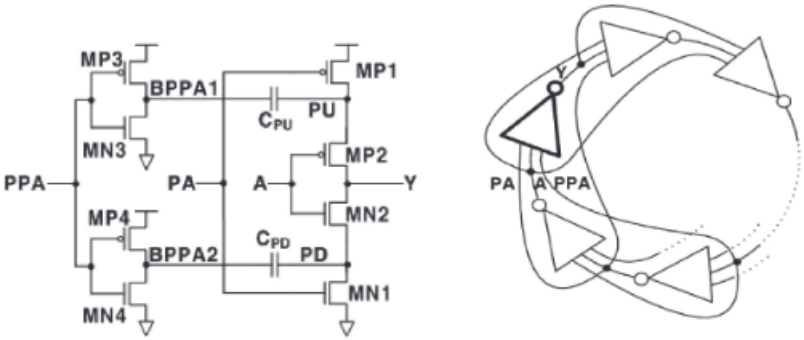
Figure 18 – Bootstrap cell - N network charge after P charge



Source: the author

When designing this cell the designer should be aware of some design characteristics. The capacitance of the charging elements will have a great impact on the driving capability of the cell. This means that a small inverter won't be able to drive the next stage of the oscillator. This effect is even worse when the impedance between source and drain of transistors N1 and P1 is not so small when they are operating at their on state, which is the case when operating in weak inversion. In the transition time, i.e when both N1 (P1) and N2 (P2) are conducting the charge stored in the lower (upper) capacitor may be lost through the path of transistor N2 (P2). This problem was addressed by (18) by a different scheme of interconnection in the RO as ilustrated in figure 19. The delay between the cells would provide a decrease in this loss at the cost of a more complex routing between the cells of the oscillators that would translate in an area penalty.

Figure 19 – Bootstrapped RO with different interconnection scheme



Source: (18)

3 COMPARISION BETWEEN THE DIFFERENT RO CELLS

A chip test was designed and manufactured in order to test the different RO basic cells. The purpose of the test was to assess the topology that would work at the minimum possible supply voltage. The technology used had 130nm of minimum nominal channel length. Low-VT transistor were used since their drive capability is enhanced, which makes the measurements easier. Four different topologies were considered including 2 inverters and 2 Schmitt Triggers. 40 Samples of the test chip were manufactured in August of 2018 through the Mosis program and the measurements were executed in the following month. The design methodology as well as the basic cell topologies will be described in section 3.1. The simulation results for the proposed ROs will be presented in section 3.2. Section 3.3 contains the result of the measurements made.

3.1 DESIGN METHODOLOGY OF THE CHIP TEST

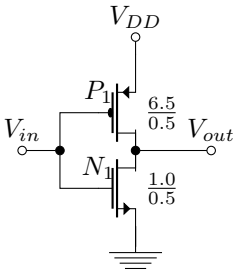
Some basic cells were chosen in order to compare which one would have the best performance operating at the minimum possible voltage.

The two inverter topologies chosen were the classic inverter and inverter using the bulk biasing technique. The reason for choosing this topologies was that the CMOS inverter is the classic basic cell for ROs, serving as benchmark for any further analysis. As discussed in section 2.5 the CMOS inverter using the bulk biasing technique has an increased gain (by a factor of n) when compared to the CMOS inverver. This can potentially make the dual gate inverter RO oscillate at smaller voltages (section 2.4).

For the ST ROs we have chosen the classic 6T and the dual gate classic 6T. This topologies were choosen in accordance with section 2.3.2 where the result of (9) was presented. This result shows that a well projected ST can achieve unit gain at a supply voltage smaller than the CMOS inverter. The considerations about the dual gate technique are the same as that for the CMOS inverter.

A study of the optimum number of stages for ROs was conducted in section 2.4. The study concluded that increasing the number of stages for more than 13 would generate marginal enhancement in the

Figure 20 – Designed CMOS Inverter used in Different Cells



Source: the author

minimum gain to start oscillation when compared with the necessary area. Because of this, in this work, all the ROs have 13 stages.

The channel length L of the transistors was chosen to be around four times the minimum available by the technology. Using a channel length that was too small would increase the presence of mismatch in the manufactured cells. Too long channel lengths would increase the output capacitance of the unit cell making the oscillator slow. A channel length of 500nm was choosen.

The channel width W was chosen to balance the oscillator DC level, by equalizing the force of the N and P networks when working at a voltage supply of 60 mV. The technological parameters in (2.12) vary with the supply voltage in a different scale in the N and P networks (specially in WI). It is not possible to balance an amplifier for all V_{DD} (although over small V_{DD} ranges the technological parameters would not vary much). The V_{DD} of 60 mV was chosen because it was near the minimum V_{DD} of oscillation for all ROs and most oscillators would oscillate at this voltage. As discussed in section 2.2, balancing the amplifiers is of primary importance in order to increase the gain at a given V_{DD}. Of course, once fabricated, the samples will suffer from mismatch and process deviation that will put the amplifier out of balance. The dimensions for the inverter (figure 20) and the dual gate inverter are listed in table 4.

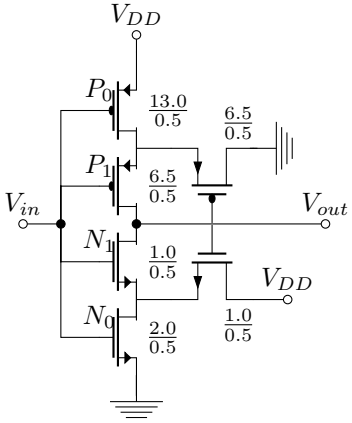
In order to design the ROs containg the classic Schmitt Trigger as basic cell we refereed to the work of section 2.3.2. Transistor N0 (P0) was designed to be 2 times stronger than transistors N1 (N1) and (P1). This design was preferred because the difference in gain when using optimal N0(P0) dimensions (described in section 2.3.2) would incur in little loss of gain (less than 1%). On the other hand, some area could

Table 4 – Dimensions of the Inverter and the Inverter Using Bulk Biasing Technique

	W[µm]	L[µm]
N1	1.0	0.5
P1	6.5	0.5

Source: the author

Figure 21 – Designed ST used in Different Cells



Source: the author

be saved by using a smaller transistor.

The N and P network were balanced to equalize the transistors force when operating at a 60 mV voltage supply. Table 5 describes the dimensions of the transistors used in the classic 6T ST (figure 21) and in the same Schmitt Trigger using dual gate transistors.

All the considerations in Chapter 2 were made with an unloaded RO. Since this work needs to measure the RO performance, the RO will need to be capable of working when loaded by the measurement equipment. This task is not evident when working at ultra-low voltage, since, besides the need of driving the measurement equipment, the RO would experience noise and interference levels that could be comparable to the signal amplitude (small SNR).

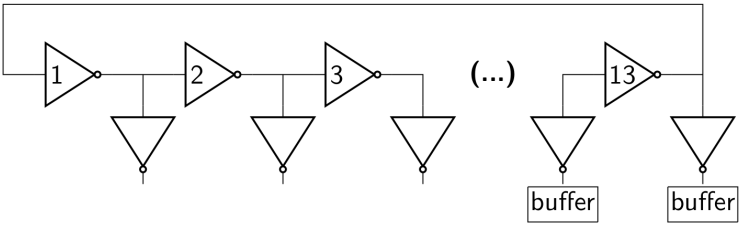
The oscillators were designed to have 16 pF of load capacitance.

Table 5 – Schmitt Trigger Using Simple CMOS Topology and Dual Gate Transistors Dimensions

	W[µm]	L[µm]
N0	2.0	0.5
N1	1.0	0.5
N2	1.0	0.5
P0	13.0	0.5
P1	6.5	0.5
P2	6.5	0.5

Source: the author

Figure 22 – RO auxiliary circuitry



Source: the author

This is equivalent to the oscilloscope probe capacitance. The output was the difference from 2 consecutive stages of the RO (since the 2 signals were inverted), reducing the noise and interference effects. In order to drive the 16pF capacitance a buffer was designed in each of the outputs. This buffer was supplied with the same voltage as the RO. The other outputs of the RO had a dummy cell as a load in order to balance the loads in the outputs of the oscillator. The idea is represented in figure 22.

After some simulations it was decided that the buffer should have 5 stages. Each stage would have transistors 2 times stronger than the previous stage. Another important point is that the cells of the buffer of each RO were the same as the basic cells of the RO being tested. This was important because if we used only inverters in the buffer, by

Figure 23 – Auxiliary Buffer to Drive the Oscilloscope Probe Capacitance

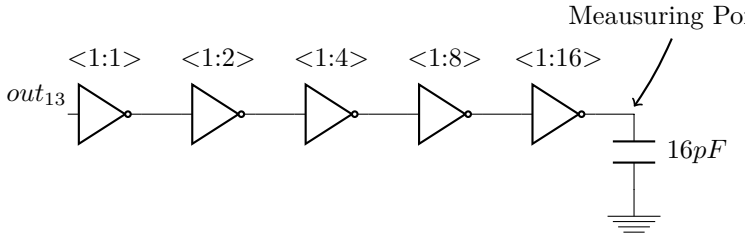


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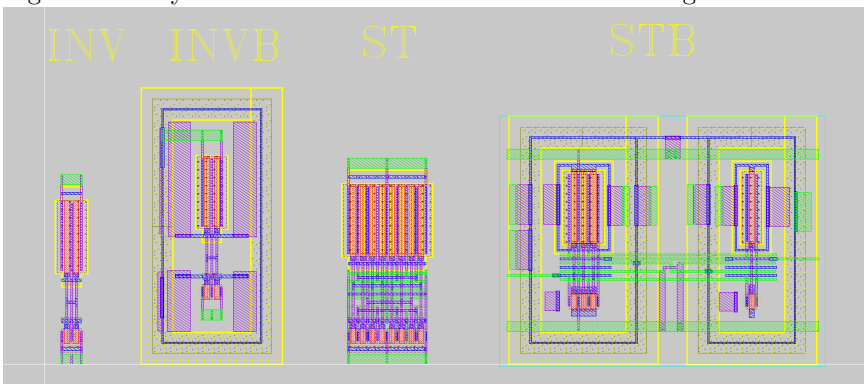
Figure 24 – Layout of each of the basic cells used in the ring oscillators



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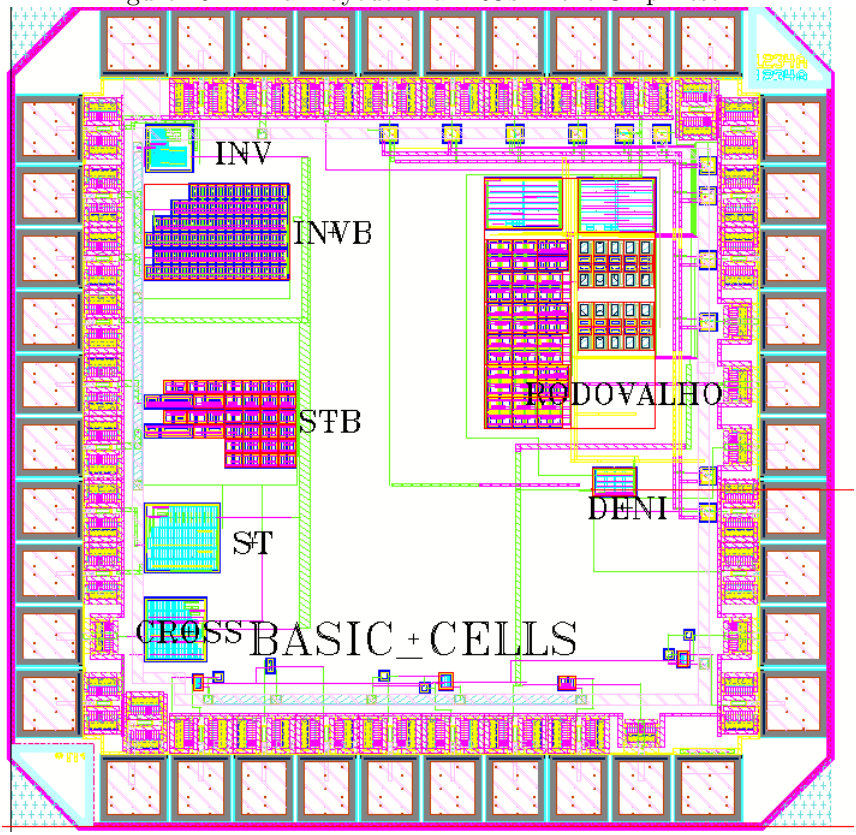
the time the inverter stopped working we wouldn't be able to know if the oscillator was still working. The buffer idea is depicted in figure 23.

The layout of each of the cells is presented in figure 24. The dimensions of the cells are 206 x 1837nm, 1371 x 2675nm, 772 x 2000nm and 2980 x 2400nm for the INV, INVB, ST and STB, respectively.

The final layout of the chip test is depict in figure 25. The die size is 1.5mm x 1.5mm. The figure gives an idea of the area penalty when using dual gate technique. Notice that the block near the "INV" label is the RO containing the classic inverter as basic cell. The "INVB" is the RO that uses the inverter with the dual gate technique, "ST "is the classic Schmitt Trigger and the "STB" is the classic Schmitt Trigger using the dual gate technique. The other blocks aren't described in this

Figure 25 – Final Layout of all ROs in the Chip Test



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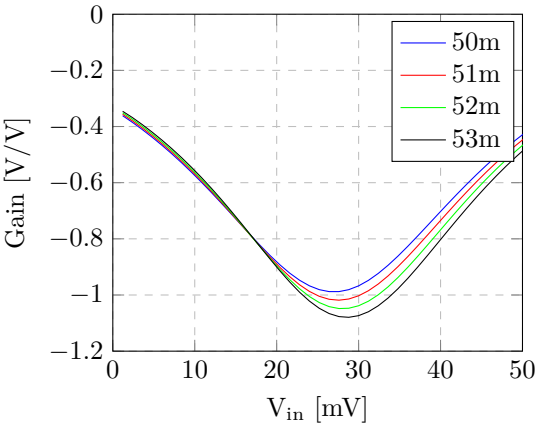
work.

3.2 SIMULATION RESULTS

Some DC and transient characteristics were simulated in order to assess the performance of the different unit cells and oscillators. Low-VT transistors modelled with BSIM 4.4 have been employed in the simulations. BSIM 4.4 was used because it is provided by the technology used in the chip test. The first point to be evaluated was the transfer function of the different cells. These simulations were impor-

Figure 26 – INV Gain - V_{DD} from 50 to 53 mV



Source: the author

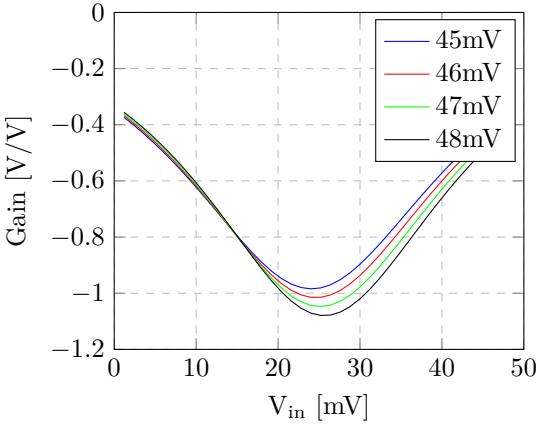
tant to check if the cells were balanced and to evaluate the gain at different supply voltages.

3.2.1 DC SIMULATION OF THE UNIT CELLS

The DC simulations where run for the 4 different cells (INV, INVB, ST and STB). First the transfer function (V_{in}xV_{out}) of these cells was evaluated using different supply voltages. Then, applying the derivative function we could assess the gain. The results are plotted in Figures 26 - 29.

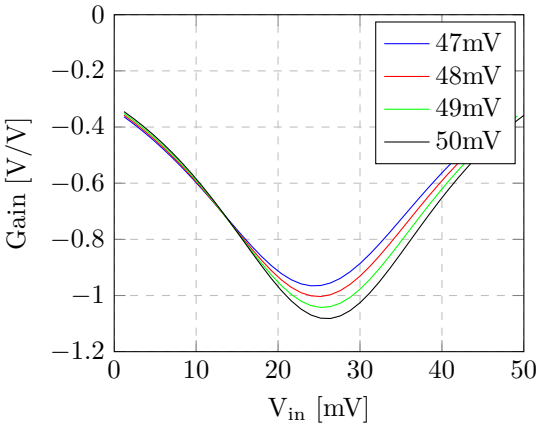
As can be observed from the plots, all the cells presented their maximum gain in the region where V_{in} was near $V_{DD}/2$. This is in good agreement with the criterion presented in section 2.2. In fact, the aspect ratios were balanced to produce this result. The supply voltage was different in each of the plots to make the evaluation of the minimum unit gain supply voltage easier. As expected, the STB presented the minimum supply voltage, followed by the INVB, ST and INV, respectively. As stated in section 2.4 the minimum gain to make a 13-stage RO work would be around 1.03 V/V. Table 6 displays the minimum supply voltage to make a RO when comparing it to the gain plot presented in figures 26 - 29.

Figure 27 – INVB Gain - V_{DD} from 45 to 48 mV



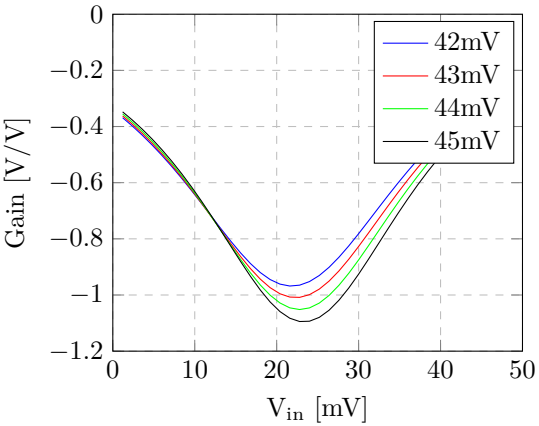
Source: the author

Figure 28 – ST Gain - V_{DD} from 47 to 50 mV



Source: the author

Figure 29 – STB Gain - V_{DD} from 42 to 45 mV



Source: the author

The next step would be to perform the transient simulation and check if the ROs were oscillating at the voltages described in table 6.

3.2.2 TRANSIENT SIMULATION OF THE ROS

Transient simulations were run for the 4 different ROs. All the simulations were made with unloaded ROs, i.e. without the 16 pF load in the output of the oscillator. It was expected that near the minimum V_{DD} for oscillation the output signal would not saturate. A step function was applied at V_{DD} and the amplitude of oscillation was evaluated after the RO achieved its steady-state response. Figure 30 represents the plot containing the amplitude of oscillation (peak-to-peak) for different V_{DD}.

The transient simulation is in close agreement with the DC simulation. The V_{DDmin} encountered in table 6 were the same minimum supply voltage that could start a RO according to figure 30. The amplitude of the STB was slightly bigger for small V_{DD}, but, as the supply voltage increased, the amplitude of oscillation of all RO saturate near V_{DD}.

Table 6 – Minimum Supply Voltage for a RO

Cell	V_{DDmin}[mV]	Gain[V/V]
INV	52	-1.048
INVB	47	-1.047
ST	49	-1.042
STB	44	-1.051

Source: the author

3.3 MEASUREMENTS AND ANALYSIS

After the chip test arrived from the foundry the measurements started to be done. We had a total of 40 samples of the chip so a statistical analysis could be done.

In order to assess the minimum supply voltage that would make that RO oscillate, a step voltage was applied at V_{DD}. A minimum of 10 mV of differential output was required in order to an oscillator to be considered oscillating.

Figures 31, 32, 33 and 34 show the distribution of the voltages in which the oscillation started for inverter (INV), dual gate inverter (INVB), classic Schmitt Trigger(ST) and dual gate Schmitt Trigger (STB), repectively. Table 7 summarizes the results.

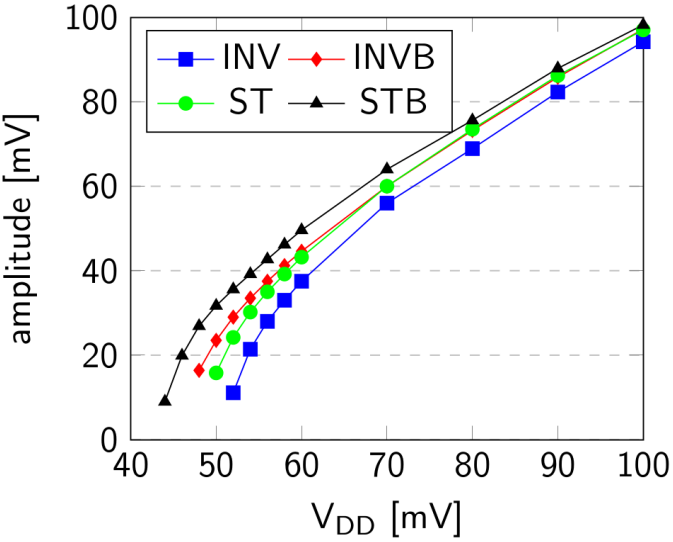
Table 7 – Minimim Measured Supply Voltage to Start Oscillating

	INV	INVB	ST	STB
μ[mV]	65.2	54.9	59.5	53.2
σ[mV]	2.3	1.6	1.8	1.3

Source: the author

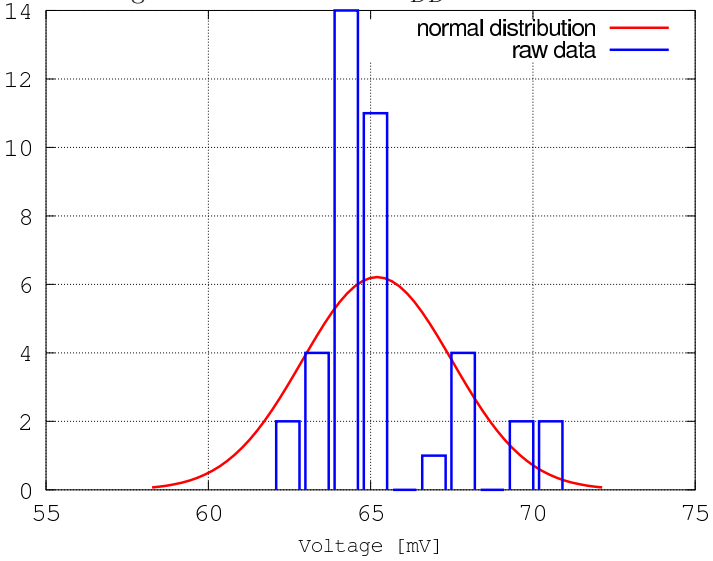
We can see from table 7 that the measured results were higher than the simulated results in table 6. Even trying to do the best layout, buffer and auxiliary circuitry to measure the ROs, some parasitic capacitance and resistance will be present in the cables, connectors,

Figure 30 – Simulation of the Basic Cells Amplitude of Oscillation



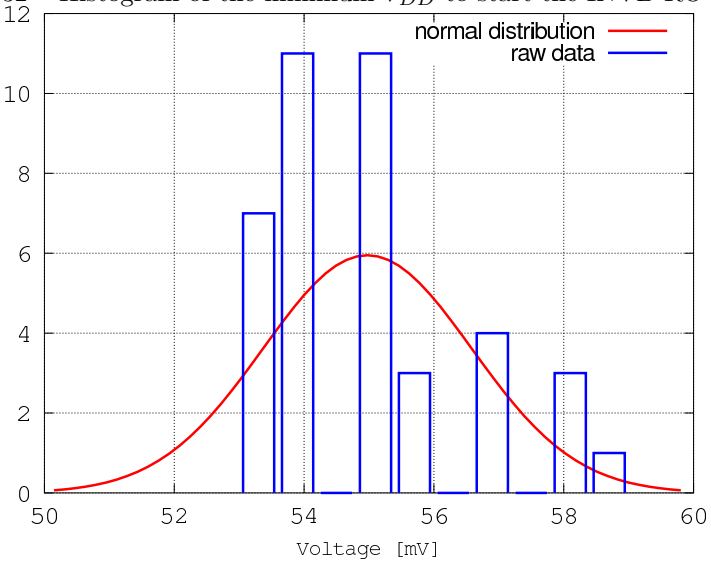
Source: the author

Figure 31 – Histogram of the minimum V_{DD} to start the INV RO



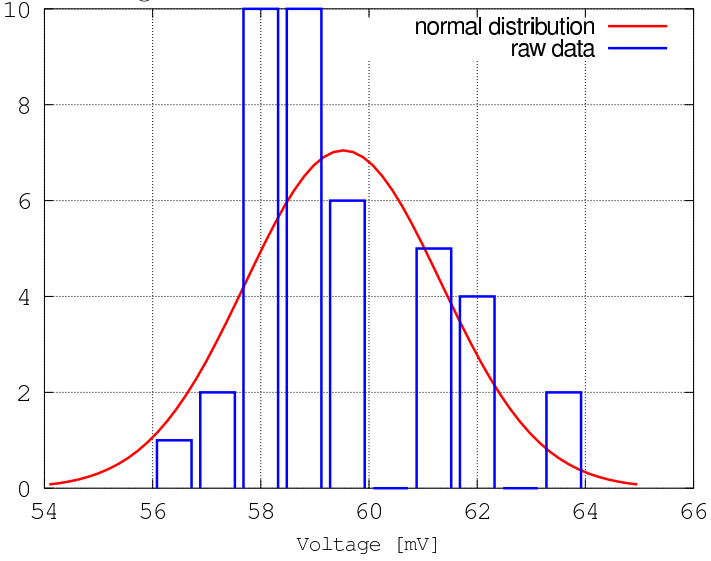
Source: the author

Figure 32 – Histogram of the minimum V_{DD} to start the INVB RO



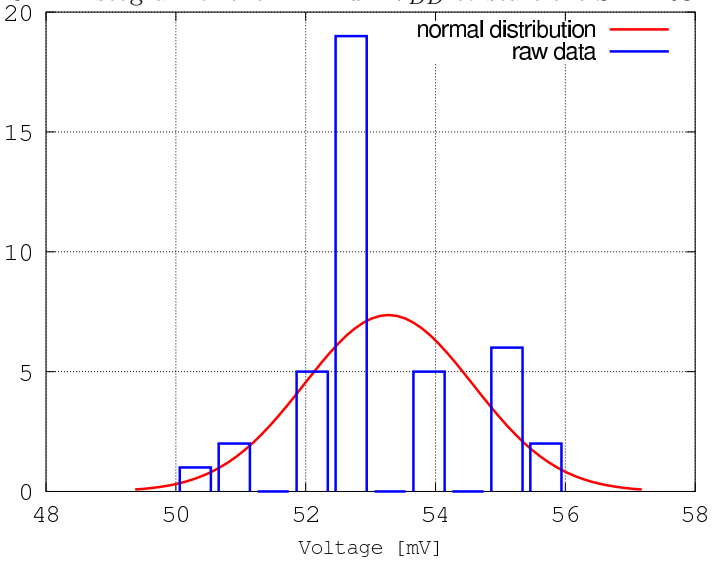
Source: the author

Figure 33 – Histogram of the minimum V_{DD} to start the ST RO



Source: the author

Figure 34 – Histogram of the minimum V_{DD} to start the STB RO



Source: the author

pads, bond-wire, vias, etc. Some loss is expected from this parasitics. Other than that, the loss caused by mismatch and process variations is even more important.

As can be noted from the measurements, the basic cells that used the bulk biasing technique presented the best performance when operating at small voltages. The standard deviation was similar in all the cases. Another point to be noted is that the Schmitt trigger (ST) presented a difference of 5.7 mV (almoust 10%) of mean minimum oscillation voltage when compared with the CMOS inverter (INV). When comparing the CMOS inverter to the STB the difference is 12 mV (18.4%).

The waveform of the different oscillators is depicted in figures 35 - 42. The blue and yellow waveforms correspond to the output of the buffers (Figure 22). The orange waveform corresponds to the difference of the buffers outputs.

Figures 35 and 36 present the best INV ROs oscillating at 61 mV and 80 mV, respectively. The yellow output presented an amplitude that was smaller than the blue one. This is probably an issue regarding the mismatch in the two buffers. When operating at 80 mV the signal

still did not have enough gain to saturate the output.

Figure 35 – INV RO oscillating at 61 mV

Source: the author

Figures 37 and 38 present the best INVB ROs oscillating at 53 mV and 80 mV, respectively. There was no clear waveform in the output of the buffers at 53 mV, because of the presence of a significant common mode interference. After the cancellation of this common mode interference the differential output could present the INVB oscillation. One possible reason for this common mode interference is bad isolation from the other oscillators. As there are four RO operating at low voltages in the same die, they interfere with each other. Nonetheless, the output signal was already saturating at 80 mV.

Figures 39 and 40 present the best ST ROs oscillating at 54 mV and 80 mV, respectively. There was no clear waveform in the output of the buffers again at 54 mV. We can see this time that the interference has a higher frequency than ST RO frequency. This interference is probably provenient from the INVB RO that oscillates at a frequency higher than the ST RO. Probably there is an interference signal due to the STB oscillator, but, as the STB is much slower, its waveform is not so evident. At 80 mV the ST RO was already saturating as well.

Figures 41 and 42 present the best STB ROs oscillating at 54 mV

Figure 36 – INV RO oscillating at 80 mV

Source: the author

and 80 mV, respectively. This time there was a clear higher frequency interference at 48 mV that was cancelled in the differential output. The interference probably came from the INVB RO since the INV and ST oscillators are not capable of oscillating at 48 mV (table 6).

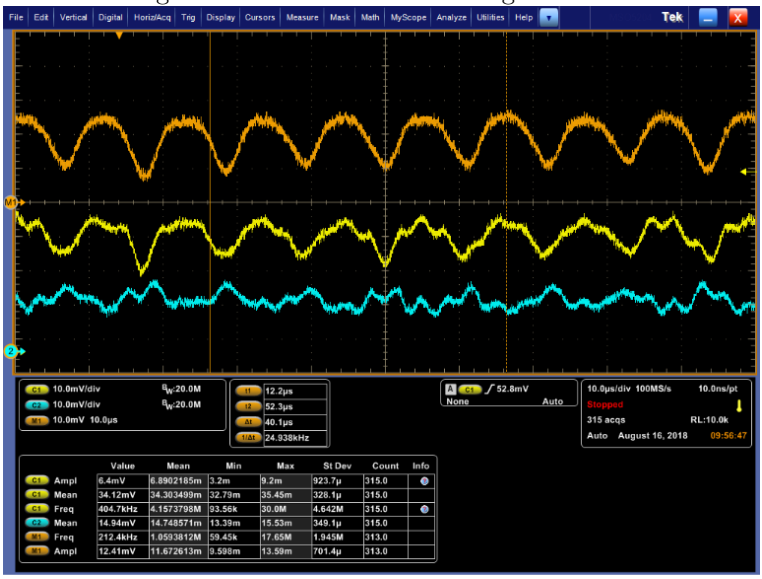
It is important to point out that, even when there was no signal in the output of the buffer, the RO could be working. Due to mismatch the RO can be oscillating and the buffer may not be able to drive the oscilloscope probe capacitance. Table 8 summarizes the minimum measured supply voltage for the different ROs.

Table 8 – Minimum Measured Supply Voltage to Start Oscillating (best sample)

	INV	INVB	ST	STB
V_{DDmin} [mV]	61	53	54	48

Source: the author

Figure 37 – INVB RO oscillating at 53 mV



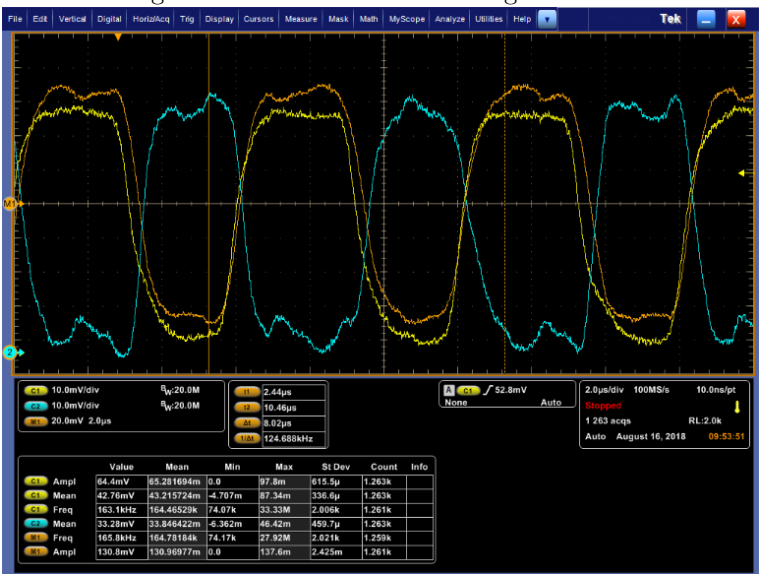
Source: the author

The frequency of oscillation was also measured in the 4 cases. Figure 43 presents the measurement of the frequency in each of the oscillators for different V_{DD}. The V_{DD} step was 10 mV. A comparison plot between all the results is presented in figure 43.

As expected the CMOS inverter presented the highest frequency of oscillation, since it has the smallest input and output capacitance. A significant frequency penalty was observed when using the dual gate technique (around 66% loss in the case of the inverter at 200 mV). The Schmitt trigger also presented a slow response, even slower than the inverter using the dual gate technique.

All this data is of great importance when designing an ultra-low voltage RO, but, in TEG EH systems, after the start-up RO, a DC-DC converter needs to work. This DC-DC converter will put the voltage generated by a TEG in a usable range for the other circuitry. A minimum voltage is necessary to make the DC-DC converter work. In cases where the voltage generated in the output of a RO is not be enough to start a DC-DC converter, the use of a bootstrapped RO may be convenient. A novel bootstrapped RO will be described in the next chapter.

Figure 38 – INVB RO Oscillating at 80 mV

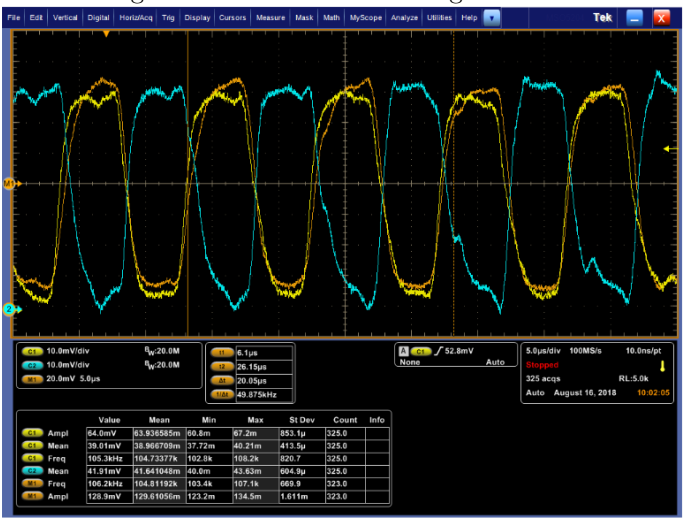


Source: the author

Figure 39 – ST RO Oscillating at 54 mV

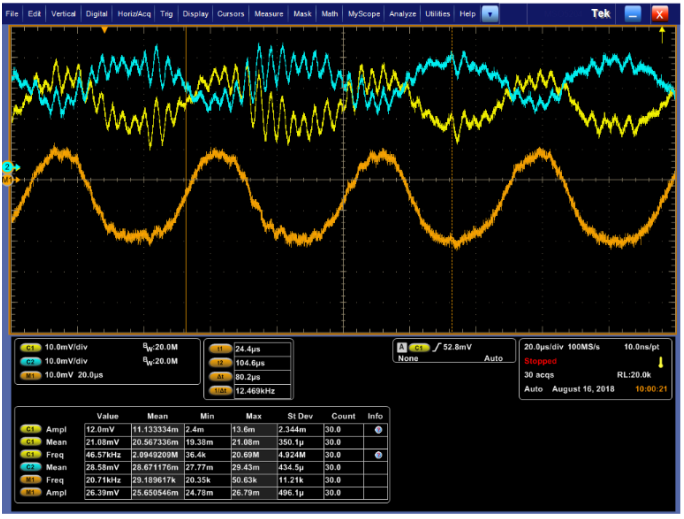
Source: the author

Figure 40 – ST RO Oscillating at 80 mV



Source: the author

Figure 41 – STB RO oscillating at 48 mV

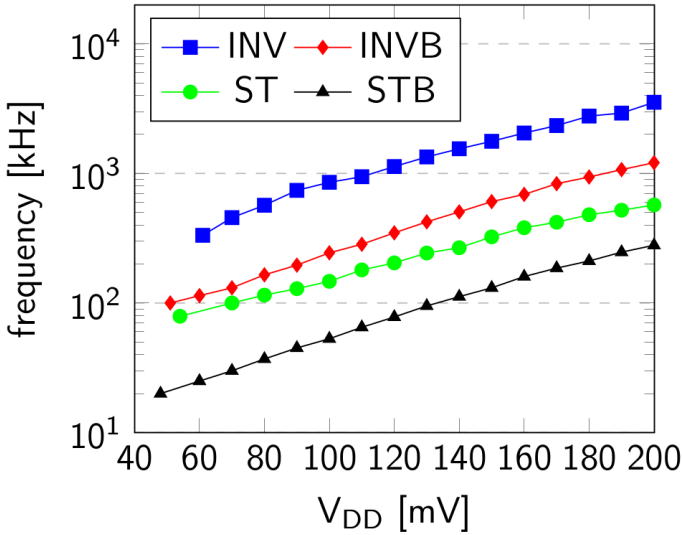


Source: the author

Figure 42 – STB RO oscillating at 80 mV

Source: the author

Figure 43 – Basic Cells Frequency Comparison



Source: the author

4 DESIGN OF A BOOTSTRAPPED START-UP BLOCK

In order to test the different RO bootstrapped start-up blocks a chip test was designed and was being manufactured by the time this work was written. The goal of the chip test was to be a proof of concept of the topology showed at section 2.6 and the one showed in section 4.1. The technology used has 180nm of minimum nominal channel length. The chip test was manufactured through the MOSIS program and future measurements are intended to be done in order validate the results of this work. The new proposed bootstrapped start-up topology will be presented in section 4.1. The design methodology will be described in section 4.2.

4.1 PROPOSED BOOTSTRAPPED START-UP BLOCK

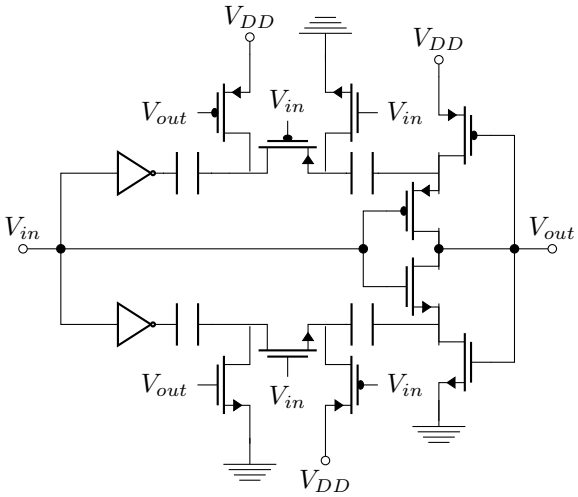
The working principle described in the circuit depicted at Figure 44 is very similar from the original bootstrap showed in figure 15. The difference is that now 4 elements can store charge (2 in the N network and 2 in the P network). This makes the circuit able to swing its output (ideally) from -2VDD to 3VDD. In this approach the area penalty would increase to 4 capacitors and 12 transistors at each stage.

The analysis of this topology can be done in the same manner as it was conducted in section 2.6. Considering the transistors as perfect switches we can draw the behavior of this cell in a RO.

Considering the bootstrap working in a RO, the input and the output would have oposite and alternating voltage levels. Assuming the voltage level to be low in the input and high in the output (assuming the opposite would lead to similar results) we would have the situation described in Figure 45. As we can see both capacitors are charged in the N network, while the capacitors in the P network would not be charged at first.

Moving further to the time when input and output change states, we have the situation depicted in figure 46. At this time the lower not port will force a 0 voltage in the left terminal of the capacitor connected to it. In order to maintain the capacitor voltage its right connector will need to change to a -1 voltage. The same process will happen to the following capacitor producing a voltage of -2 in its right terminal. The P network capacitors will be charged during this time. As transistor N1 is in its on state, the -2 voltage will pass to the output as depicted

Figure 44 – Proposed 5 V_{DD} Bootstrap Cell



Source: the author

in figure 47.

The analog "boost in voltage" happening in the P network is depicted in figures 48 and 49. This boost would produce an output of 3 V_{DD}

This circuit could be modified in order to create even greater output swings at the expense of area penalty and parasitic loss in the transistor resistances and capacitances. To acomplish this, more capacitors and transistors would need to be placed making the middle of the circuit look like a charge pump. V_{in} and V_{out} would work as the clock of the converter. Figure 50 depicts this concept for a bootstrap cell able to (ideally) have an output swing of 7 V_{DD}.

4.2 DESIGN METHODOLOGY OF THE CHIP TEST

To compare the different bootstrapped topologies, 3 circuits were designed: a simple CMOS inverter RO, a RO using the cell described at section 2.6 (3VDD bootstrap) and one RO using the cell described in section 4.1 (proposed 5VDD bootstrap).

The number of stages of each RO was choosen to be 13 following the same logic as in section 3.1. Using metal-insulator-metal (MIM) ca-

Figure 45 – Proposed 5 V_{DD} Bootstrap Cell - first N network charge

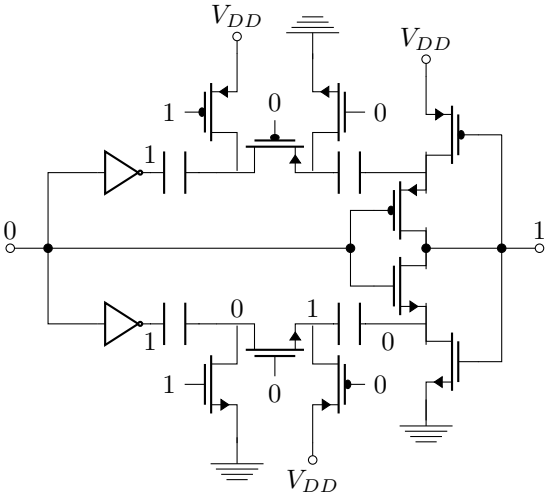


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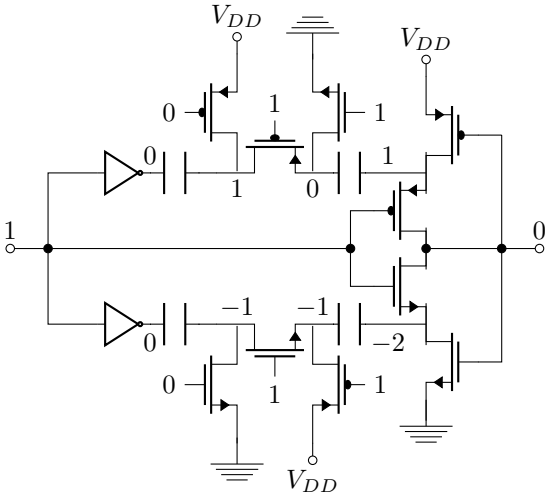
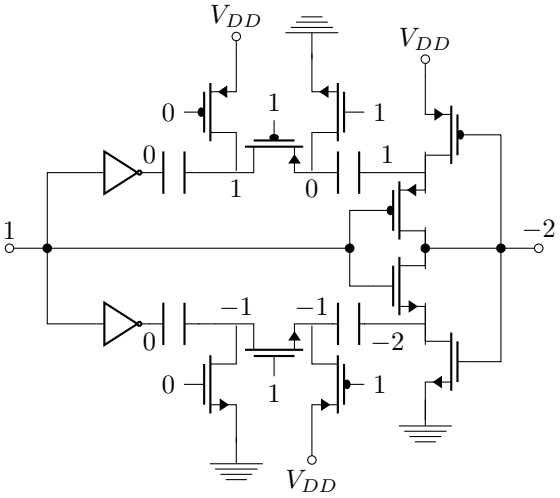
Figure 46 – Proposed Bootstrap Cell - first P network charge



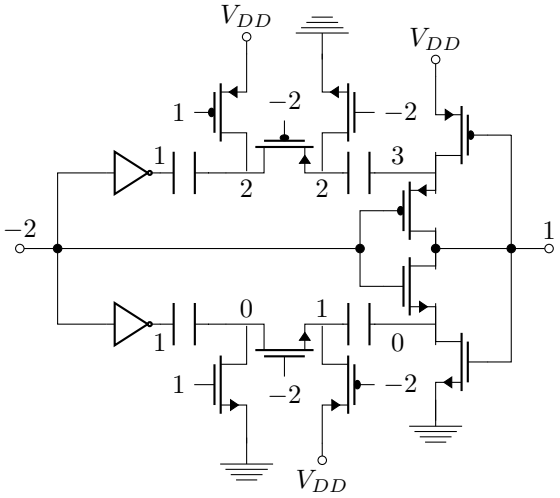
Source: the author

Figure 47 – Proposed Bootstrap Cell - second N network charge



Source: the author

Figure 48 – Proposed Bootstrap Cell - second P network charge



Source: the author

Figure 49 – Proposed Bootstrap Cell - Beginning the next cycle

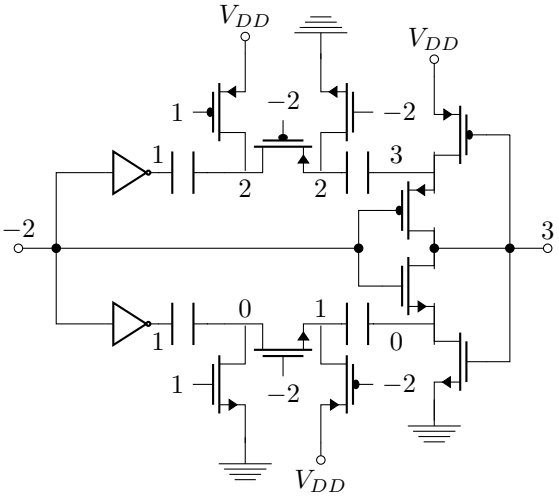


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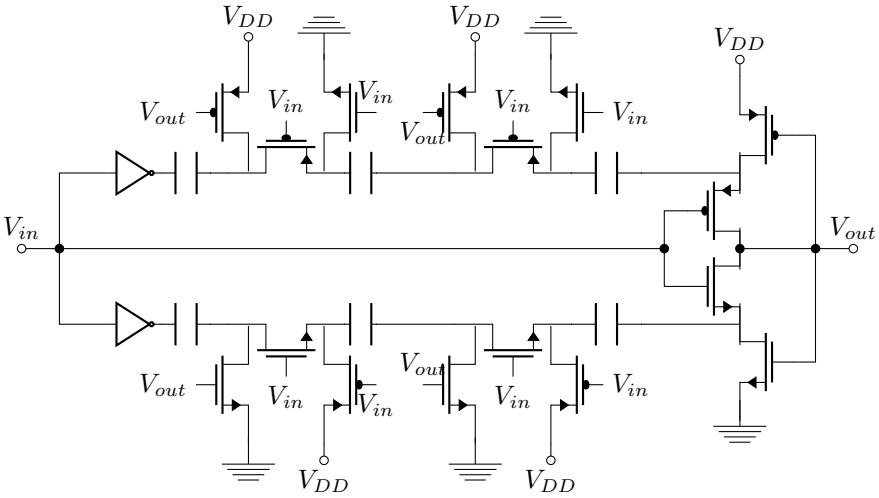
Figure 50 – 7 V_{DD} Bootstrap Cell



Source: the author

pacitors would increase the area and could even make the integration impossible due to the large number of capacitors needed. MOS capacitors where chosen instead, using the terminals of a MOS transistor to accomplish this. This technique is described in (19).

The size of the transistors made the overall circuit balanced and capable of driving the MOS capacitors. Their sizes are listed in Table 9. The circuit was simulated using a supply voltage of 100 mV. The simulated responses obtained are depicted in figure 51 and the results are summarized in table 10. As can be noted from the simulation, the increase in the bootstrap effect makes the oscillator to oscillate at higher frequencies. This effect was expected since the transistors connected to V_{out} would have greater inversion levels, increasing their drive capability.

Table 9 – Transistor sizes

	NMOS	PMOS	PMOS Capacitor
W[m]	530n	420n	20u
L[m]	300n	300n	5u

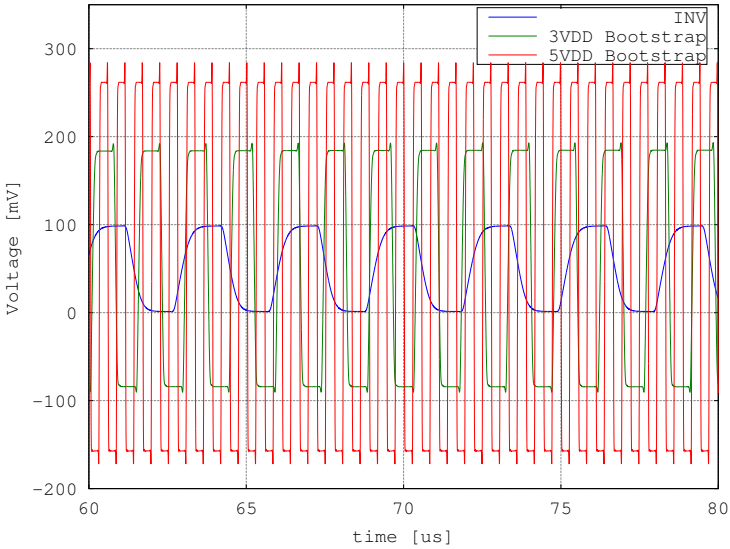
Source: the author

Table 10 – Frequency and Amplitude Simulations of Bootstrapped ROs

	Inverter	3 V_{DD}	5 V_{DD}
Frequency	11.0kHz	653kHz	1.09MHz
Amplitude	98.2mV	267mV	372mV

Source: the author

Figure 51 – Amplitude of Oscillation Comparison



Source: the author

5 CONCLUSIONS

Ring oscillators composed of Schmitt triggers or inverters with the transistor gates connected to the bulks are good choices for the start-up circuits of energy harvesters. In particular, the STB ROs described in this communication can reduce the minimum supply voltage by 5 to 6 mV in comparison with the stacked-inverter RO described in reference (20). This difference is important in the case of wearable electronics where the primary energy source is the human body, since typical primary voltages supplied by thermoelectric generators are of the order of tens of mV.

The ring oscillator model has proved to be efficient, predicting the supply voltage for oscillation with an error smaller than 1 mV in the minimum supply voltage to start oscillating. Also, the design guidelines followed in section 3, together with the experimental data, provide a variety of possible designs. These guidelines and experimental data can be used to optimize the design of a start-up RO, whether the necessity of the designer is only optimizing minimum start-up voltage or whether there are frequency an area constraints to be considered.

The number of stages in a RO was also discussed rising the conclusion that: using too much stages produces marginal lowering in the voltage supply to start the oscillator. As described in section 2.4, with 13 stages the decrease of less than 1% can be expected in the gain needed to start the RO.

The use of the bulk biasing technique should be analysed due to its high area penalty. The increase in capacitance should also be considered because it lowers the frequency of oscillation. Otherwise this technique is of great importance to increase the gain of a basic cell.

The proposed bootstrap topology increased the output swing of the RO design and proved to be an interesting choice when the RO cannot start a DC-DC converter.

REFERENCES

1 RAMADASS, Y. K. **Energy Processing Circuits for Low-Power Applications**. Department of Electrical Engineering and Computer Science, 2009.

2 FAN, P. M. et al. **Energy harvesting techniques: Energy sources, power management and conversion**. [S.l.], Aug 2015. 1-4 p.

3 BOSE, S.; JOHNSTON, M. L. A stacked-inverter ring oscillator for 50 mV fully-integrated cold-start of energy harvesters. In: **2018 IEEE International Symposium on Circuits and Systems (ISCAS)**. [S.l.: s.n.], 2018. p. 1–5. ISSN 2379-447X.

4 DAS, A.; GAO, Y.; KIM, T. T. An output feedback-based start-up technique with automatic disabling for battery-less energy harvesters. In: **2015 IEEE International Symposium on Circuits and Systems (ISCAS)**. [S.l.: s.n.], 2015. p. 233–236. ISSN 0271-4302.

5 WAN, Q.; MOK, P. K. T. A 14 nA quiescent current inductorless dual-input-triple-output thermoelectric energy harvesting system based on a reconfigurable TEG array. In: **2018 IEEE Custom Integrated Circuits Conference (CICC)**. [S.l.: s.n.], 2018. p. 1–4. ISSN 2152-3630.

6 CHEN, P. et al. A 95mV-startup step-up converter with voltage-tuned oscillator by fixed-charge programming and capacitor pass-on scheme. In: **2011 IEEE International Solid-State Circuits Conference**. [S.l.: s.n.], 2011. p. 216–218. ISSN 2376-8606.

7 ENZ, C. C.; VITTOZ, E. A. CMOS low-power analog circuit design. In: **Emerging Technologies: Designing Low Power Digital Systems**. [S.l.: s.n.], 1996. p. 79–133.

8 SWANSON, R. M.; MEINDL, J. D. Ion-implanted complementary MOS transistors in low-voltage circuits. **IEEE Journal of Solid-State Circuits**, v. 7, n. 2, p. 146–153, April 1972. ISSN 0018-9200.

9 MELEK, L. A. P.; SCHNEIDER, M. C.; GALUP-MONTORO, C. Operation of the classical CMOS schmitt trigger as an

ultra-low-voltage amplifier. **IEEE Transactions on Circuits and Systems II: Express Briefs**, v. 65, n. 9, p. 1239–1243, Sep. 2018. ISSN 1549-7747.

10 GALUP-MONTORO, C. et al. The advanced compact MOSFET (ACM) model for circuit analysis and design. In: **2007 IEEE Custom Integrated Circuits Conference**. [S.l.: s.n.], 2007. p. 519–526. ISSN 0886-5930.

11 PARK, C.-K. et al. A unified current-voltage model for long-channel nMOSFETs. **IEEE Transactions on Electron Devices**, v. 38, n. 2, p. 399–406, Feb 1991. ISSN 0018-9383.

12 GALUP-MONTORO, C.; SCHNEIDER, M. C. **MOSFET MODELLING FOR CIRCUIT ANALYSIS AND DESIGN**. International Serie on Advances in Solid State Electronic and Technology (ASSET), 2006.

13 MELEK, L. A. P. et al. Analysis and design of the classical CMOS schmitt trigger in subthreshold operation. **IEEE Transactions on Circuits and Systems I: Regular Papers**, v. 64, n. 4, p. 869–878, April 2017. ISSN 1549-8328.

14 JAEGER, R. C. **Microelectronic Circuit Design**. [S.l.], 1997. 1027-1928 p.

15 MAYMANDI-NEJAD, M.; SACHDEV, M. DTMOS technique for low-voltage analog circuits. **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, v. 14, n. 10, p. 1151–1156, Oct 2006. ISSN 1063-8210.

16 NIRANJAN, V.; KUMAR, A.; JAIN, S. B. Triple well subthreshold CMOS logic using body-bias technique. In: **2013 IEEE International Conference on Signal Processing, Computing and Control (ISPCC)**. [S.l.: s.n.], 2013. p. 1–6.

17 HO, Y.; YANG, Y.; SU, C. A 0.2–0.6 V ring oscillator design using bootstrap technique. In: **IEEE Asian Solid-State Circuits Conference 2011**. [S.l.: s.n.], 2011. p. 333–336.

18 SEO, J.-h. P. H.-S.; KONG, B.-S. Bootstrapped ring oscillator with feed forward inputs for ultra-low-voltage application. p. 333–336, 2015.

19 BEHR, A. T. et al. Harmonic distortion caused by capacitors implemented with MOSFET gates. **IEEE Journal of Solid-State Circuits**, v. 27, n. 10, p. 1470–1475, Oct 1992. ISSN 0018-9200.

20 BOSE, S.; JOHNSTON, M. L. Fully-integrated 57 mV cold start of a thermoelectric energy harvester using a cross-coupled complementary charge pump. In: **IEEE Custom Integrated Circuits Conference (CICC)**. [S.l.: s.n.], 2018.

21 MARINO. The effect of asynchronous inputs on sequential network reliability. **IEEE Transactions on Computers**, C-26, n. 11, p. 1082–1090, Nov 1977. ISSN 0018-9340.

22 STEININGER, A.; MAIER, J.; NAJVIRT, R. The metastable behavior of a schmitt-trigger. In: **2016 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)**. [S.l.: s.n.], 2016. p. 57–64.

6 APPENDIX - DYNAMIC MODEL OF THE SCHMITT TRIGGER

In the study of ROs one important concern of the designer is the dynamic characteristic of the basic cell. There is a gap in the literature regarding to this subject. A simple macro model was created in order to assess the Schmitt Trigger dynamic behavior. This model was based on the work of (21) The model consists of a transconductor with a fixed transconductance value and some passive elements to provide feedback and simulate the output parasitics. Figure 52 depicts the model.

From this model we can define some interesting parameters like transresistence (V_+/I_o) R_k and voltage gain (V_+/V_o) φ:

$$R_k = \frac{R_o R_B}{R_A + R_B + R_o} \tag{6.1}$$

$$\varphi = \frac{R_A + R_B}{R_B} \tag{6.2}$$

With this parameters we can define the transfers function I_o/V_{in} and V_o/V_{in}:

$$\frac{I_o}{V_{in}} = -\frac{G_m}{1 - G_m R_k} \tag{6.3}$$

$$\frac{V_o}{V_{in}} = -\frac{G_m R_k \varphi}{1 - G_m R_k} \tag{6.4}$$

In order to have a realistic model, the saturation effect of the transconductor must be considered. In this model the saturation of the transconductor will be V_{DD}. From this constraints we can divide its operation in 3 regions as depicted in figure 53.

Continuing with the analysis we would have 3 different ordinary differential equations (ODEs) to solve (one for each region). The solution for this ODEs considering $v_o(0)$ the initial voltage at the output is:

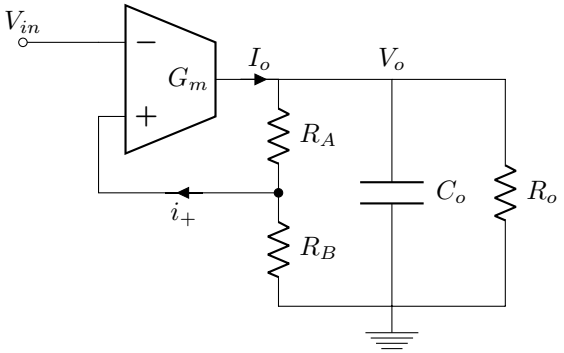
Region 1

$$v_o(t) = [v_o(0) - V_{DD}](e^{-t/\tau_s}) + V_{DD} \tag{6.5}$$

$$\tau_s = R_k \varphi C_o \tag{6.6}$$

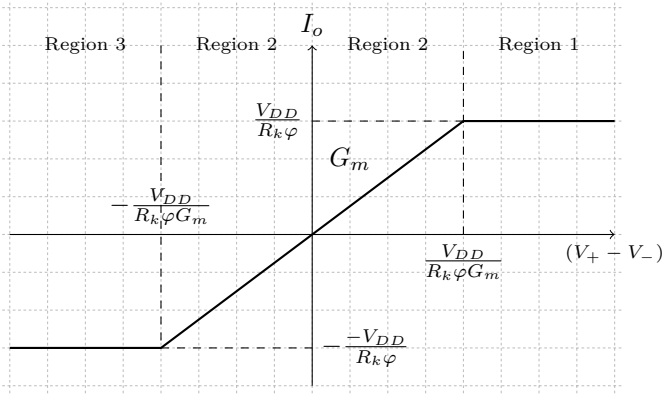
Region 2

Figure 52 – Schmitt Trigger Dynamic Model



Source: the author

Figure 53 – Transconductance Model



Source: the author

$$v_o(t) = [v_o(0) - V_{Meta}](e^{t/\tau_u}) + V_{Meta} \tag{6.7}$$

$$\tau_u = \frac{\tau_s}{R_k G_m - 1} \tag{6.8}$$

$$V_{Meta} = \frac{V_{in} G_m \varphi R_k}{R_k G_m - 1} \tag{6.9}$$

Regoin 3

$$v_o(t) = [v_o(0) + V_{DD}](e^{-t/\tau_s}) - V_{DD} \tag{6.10}$$

$$\tau_s = R_k \varphi C_o \tag{6.11}$$

As can be observed from the solutions, we have 2 stable solutions (regions 1 and 3) and 1 unstable solution (region 2). Regions 1 and 3 have the same time constant τ_s, but each of them approach different values ($V_{DD}$and -V_{DD}, respectively). Region 2 has a solution that diverges from an asymptote called V_{Meta} with a time constant τ_u. It is important to notice that the V_{Meta} asymptote is an unstable asymptote dependent on V_{in}. The closer the signal is from this asymptote the longer it will take to get to its stable state. The "velocity" can be described as in equation 6.12:

$$\frac{dv_o}{dt} = \frac{[v_o(0) - V_{Meta}]e^{\frac{t}{\tau_u}}}{\tau_u} \tag{6.12}$$

The threshold for the different regions can be calculated apllying the limit for saturation as in equation 6.13:

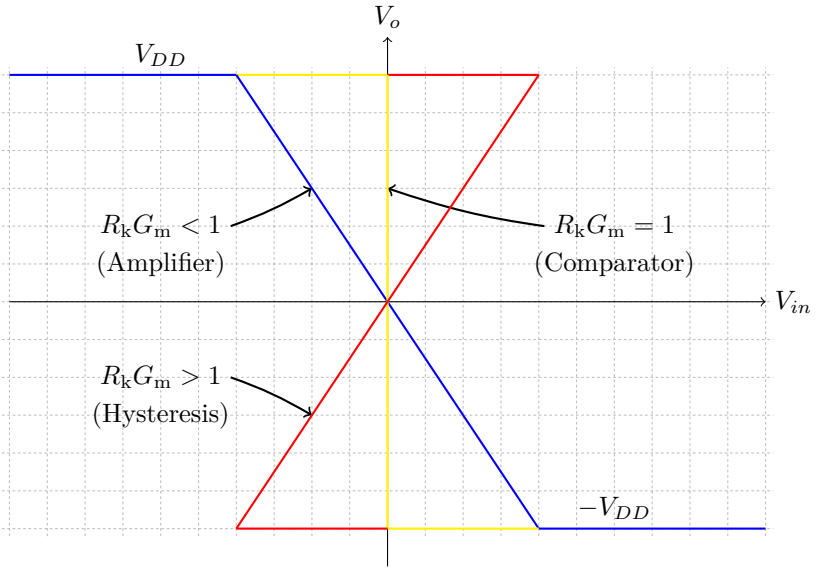
$$V_{TH\pm} = \pm \frac{V_{DD}}{\varphi}(1 - \frac{1}{R_k G_m}) \tag{6.13}$$

As expected we will only have hysteresis if the transconductance (G_m) is large enough. In other words, in order to have hysteresis the product G_m times R_k should be greater than 1. If this product is equal to 1 the circuit behaves as an ideal comparator, whereas when the product is smaller than 1 it behaves like an amplifier. Figure 54 depicts the 3 cases.

Using all of the equations in the hysteresis case we can draw a phase plane summarizing all the information of this section as in figure 55.

A test simulation was done following the approach of (22). The

Figure 54 – Transfer function for different Gm Values



Source: the author

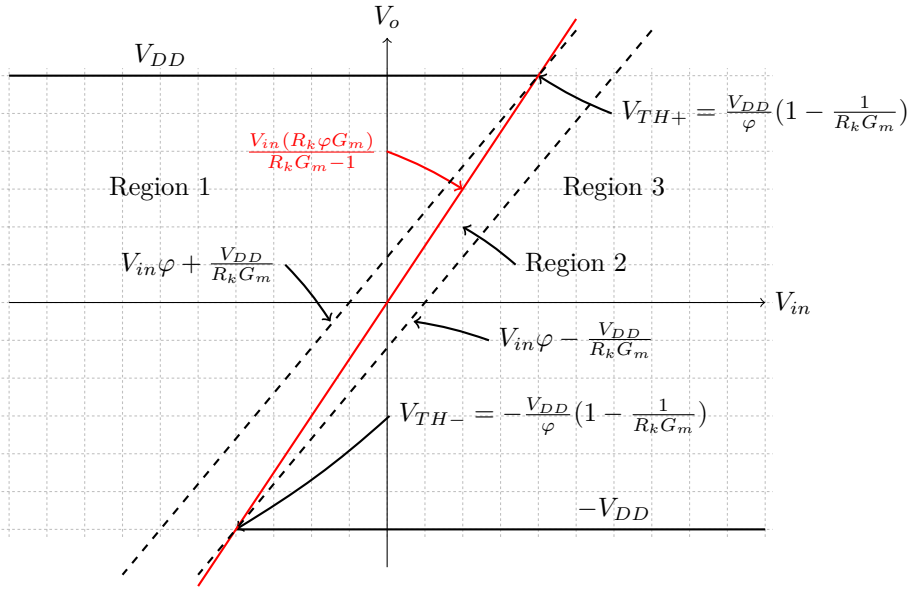
simulations were done using the model in the appendix with different input and initial output voltages. The values used in the simulation are show in table 11.

For an input voltage V_{in} of 1V and different values of initial output voltages the plot from figure 56 was obtained.

A similar simulation was done using an initial voltage of -5V and different vin values near the threshold voltage V_{TH+}. The plot is depict in figure 57.

From figures 56 and 57 it is possible to see a first moment when the curves present an exponential growth followed by an exponential decay in the second moment until reaching the steady-state response. This moments correspond to the circuit behavior in regions 2 and 3, respectively. Other thing to notice is that, the closer the circuit is from the state of metastability, the longer it takes to reach its steady-state.

Figure 55 – Dynamic Model Phase Plane



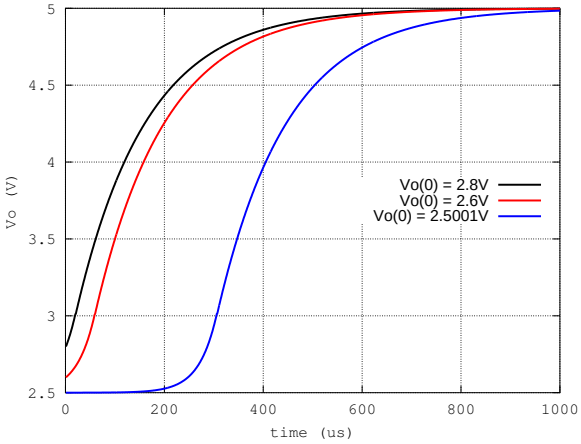
Source: the author

Table 11 – Macromodel Parameters

V_{DD}	G_m	R_A	R_B	R_O	C_O	V_{TH+}	V_{TH-}
5V	70mS	100Ω	100Ω	500Ω	1µ	2V	-2V

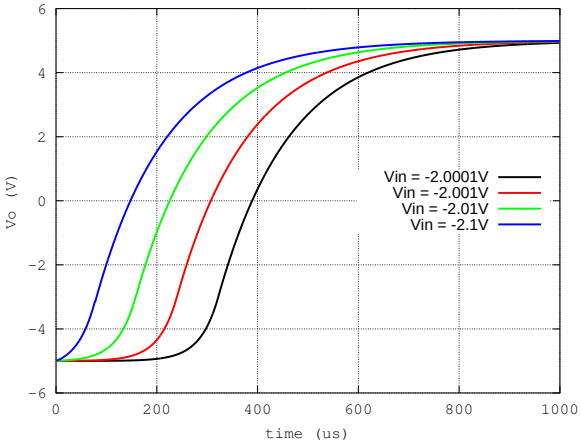
Source: the author

Figure 56 – ST Transient Response for Different Output Initial States



Source: the author

Figure 57 – ST Transient Response for Different Input Voltages



Source: the author