DESIGN OF AN ULTRA-LOW-POWER CURRENT SOURCE

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Contents

1. Introduction

- **References:**
  - **Voltage:** $V_{ref} \rightarrow \phi_t, V_{G0}$
  - **Current:** $I_{ref} \rightarrow V_{ref}/R, \mu C'_{ox} \phi_t^2$

Required for:

- A/D and D/A conversion
- Biasing (analog and digital circuits)

1. Introduction

Objective:

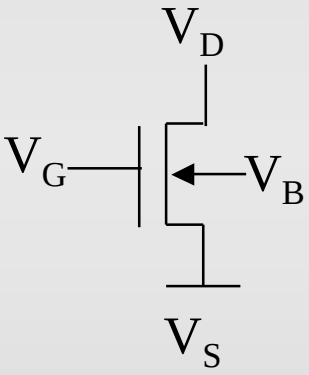
- **Design a CMOS current reference for low-voltage & ultra-low-power applications**

Characteristics of the current reference:

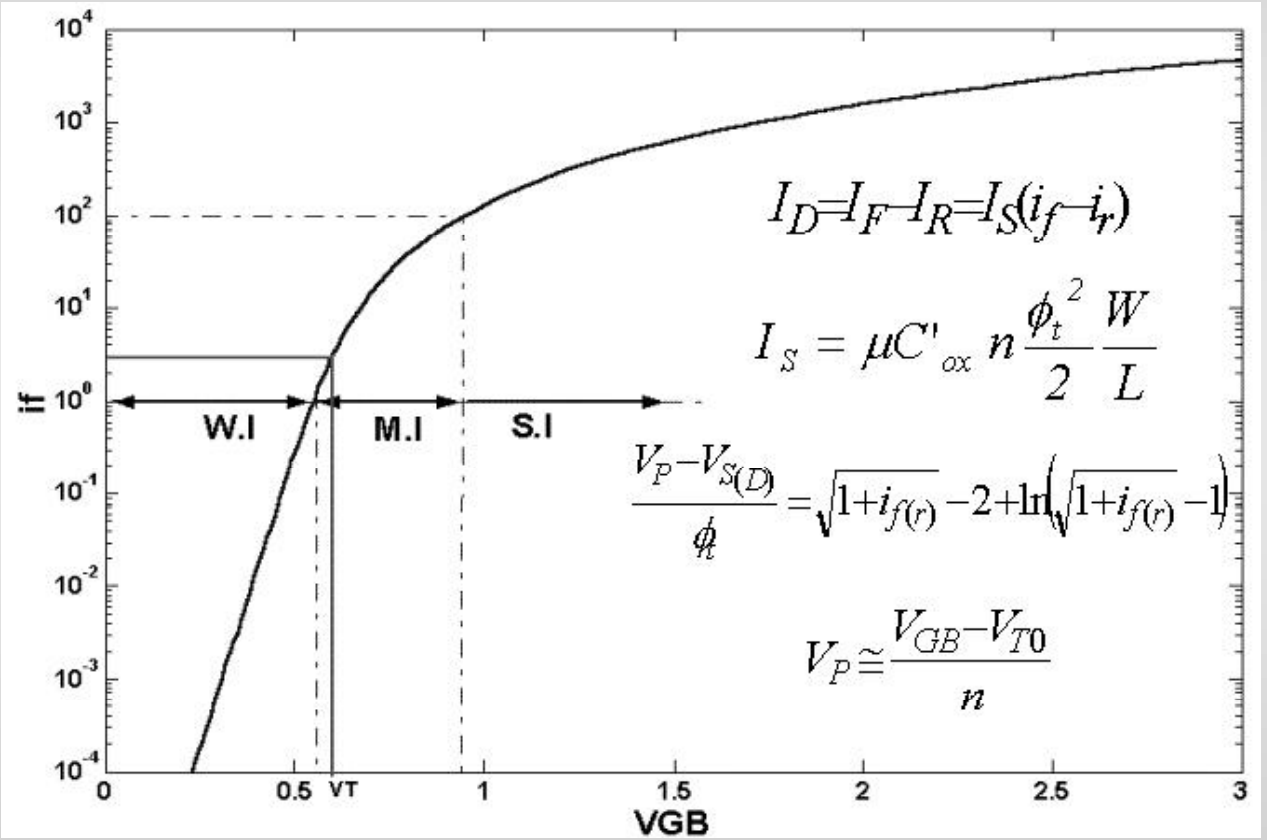
1. **Autonomous;**
2. **Low consumption;**
3. **Simple to design.**

2. Basic concepts

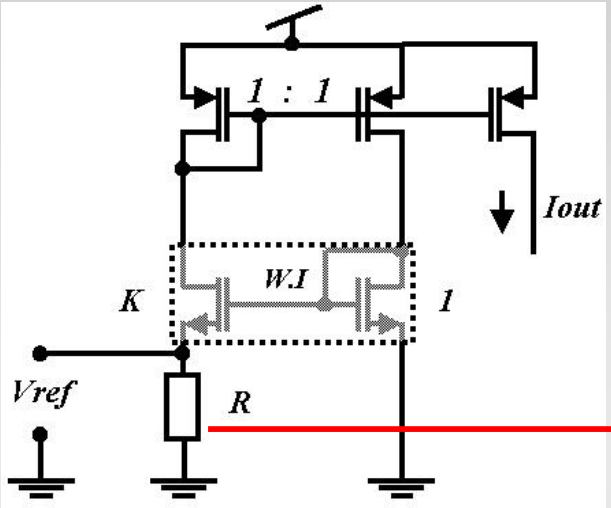
ACM model

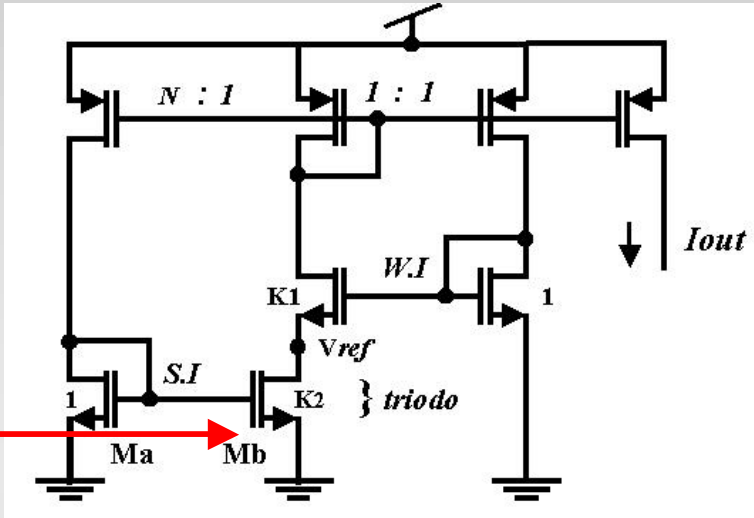


V_{SB}=0 &
saturation



3. Self-biased current references





[Vittoz ,1977]

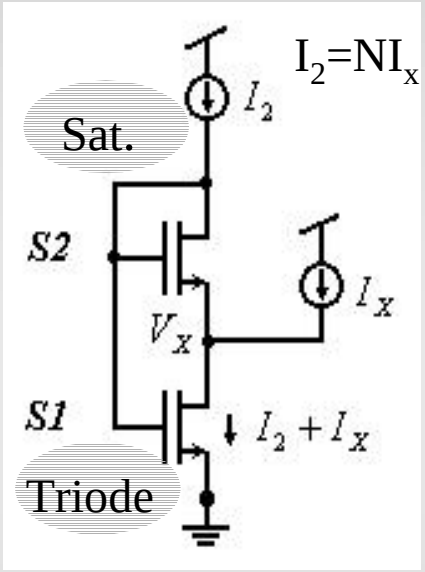
- $I_{ref} = (\phi_t / R).\ln K$
- I_{ref}=0.6nA(6nA)
- $\phi_t . \ln K = 60mV \rightarrow R = 100(10)M\Omega$

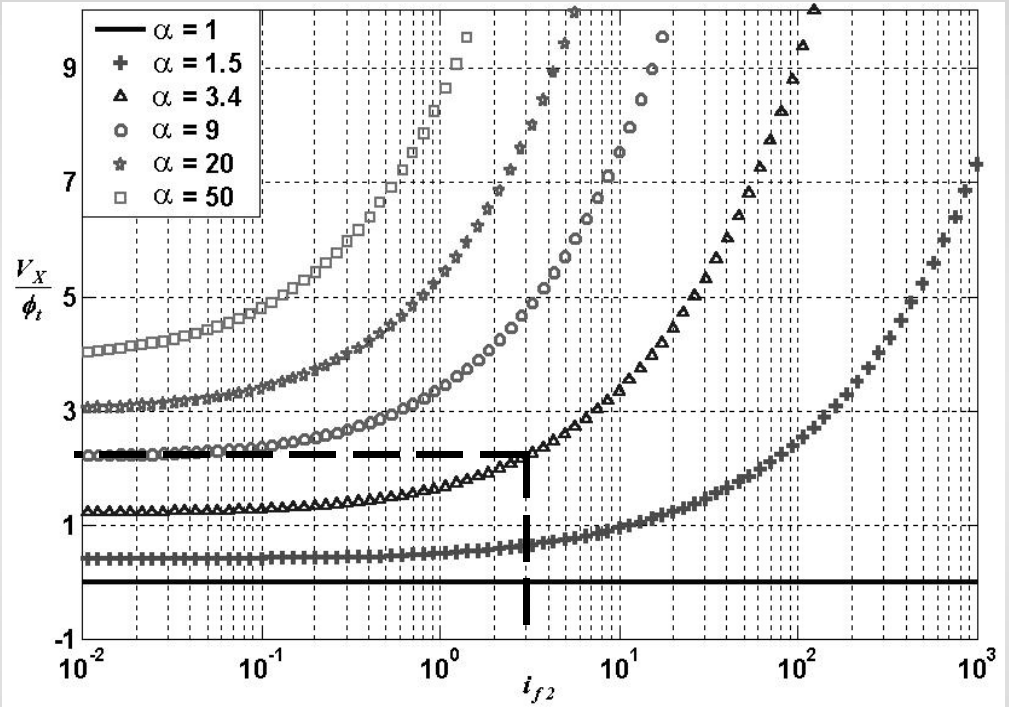
[Oguey ,1996]

- S.I. ($M_{a,b}$) not appropriate for LV
- $NK_2 > 1$
- $I_{ref} \propto \mu C'_{ox} n\phi_t^2$

4. Proposed self-biased current reference

SCM (Self-Cascode MOSFET)

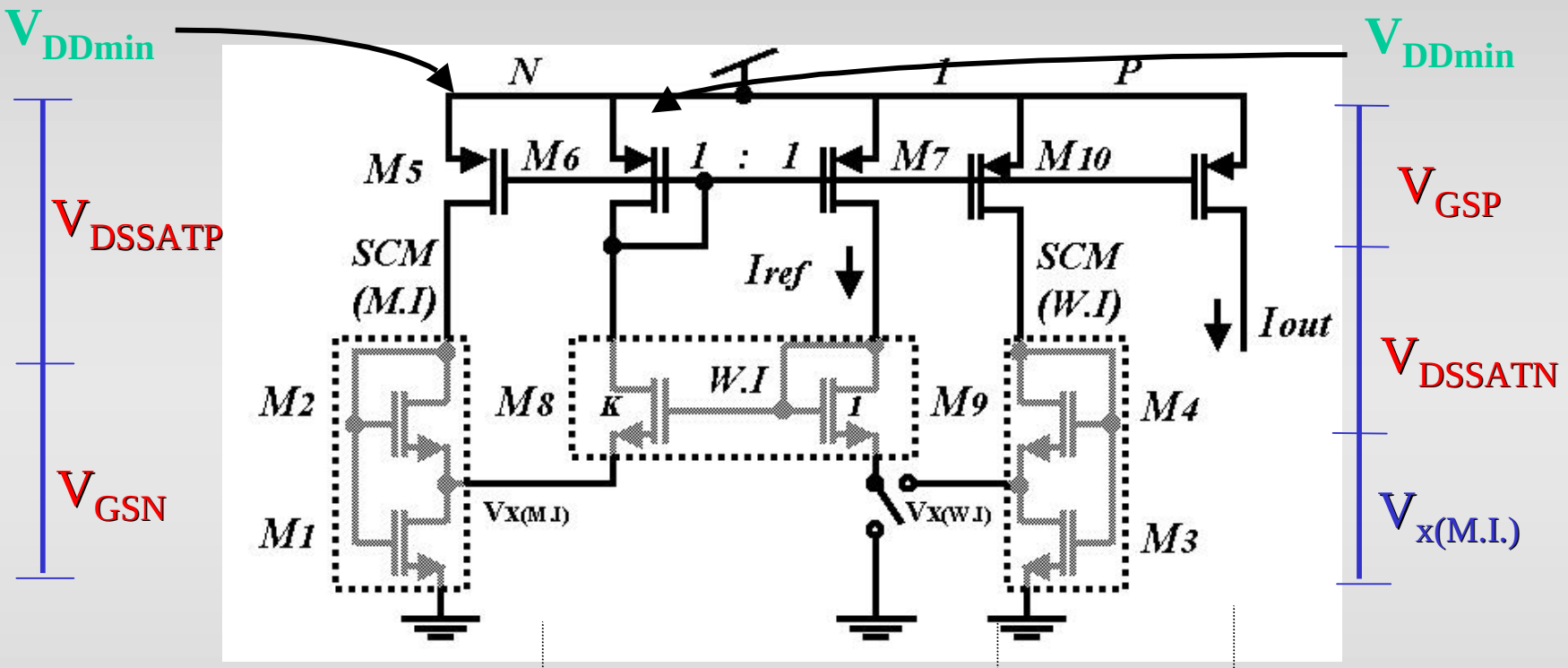




- W.I $\rightarrow V_X = \phi_t \ln\alpha$ - PTAT
- M.I, S.I $\rightarrow V_X = f(i_f, \alpha)$

$$\alpha = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right]$$

4. Proposed self-biased current reference



4. Proposed self-biased current reference

Design

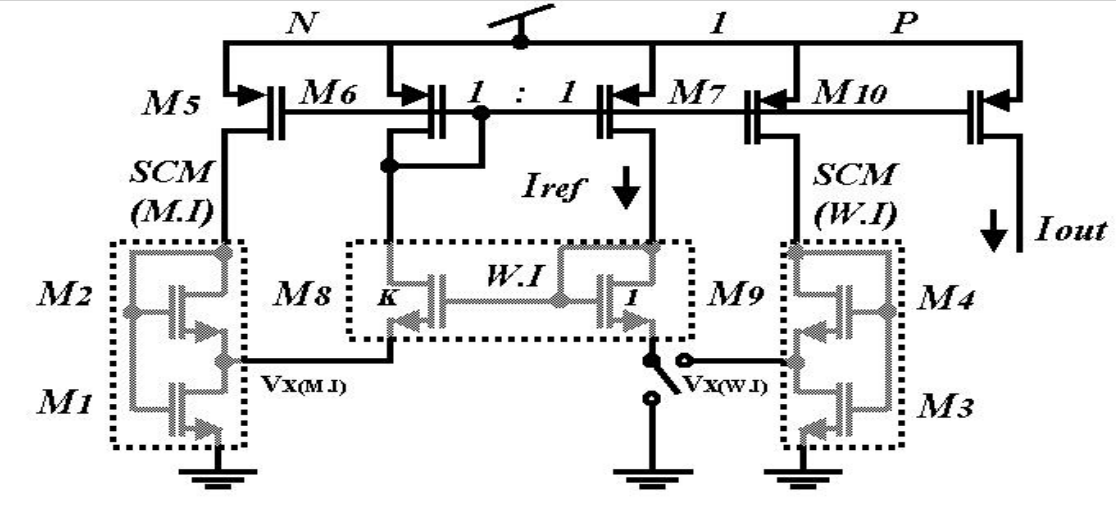
- I_{ref}=400pA, V_{DDmin}=1.2V (Possible?)
- V_X<100mV, e.g., V_X=57mV
- i_{f2}=3 - w.i. not allowed →current very sensitive to V_X
  - s.i. operation increases V_{GSN} & V_{DDmin}
- V_X=57mV and i_{f2}=3 result in α=3.4
- For the P-mirrors i_f<1 → V_{DSSATP}=100mV

5. Results

1.5 µm CMOS technology

Parameter	Simple topology, K=9		Symmetric topology, K=1		
	Sim.	Exp.	Sim.	Exp.	
V_{DDmin}	1.1	1.1	1.1	1.1	V
Power (at 1.1V)	1.5	1.5	2.0	2.0	nW
V_{ref} sensitivity to V_{DD}	0.9	1.6	0.7	1.3	%/V
V_{ref} sensitivity to T	+0.32	X	+0.32	X	%/ºC
I_{ref} sensitivity to V_{DD}	4.7	6.2	3.5	6.0	%/V
I_{ref} sensitivity to T	+0.047	X	+0.047	X	%/ºC

5. Results



TRANSISTOR SIZES FOR THE SYMMETRIC TOPOLOGY

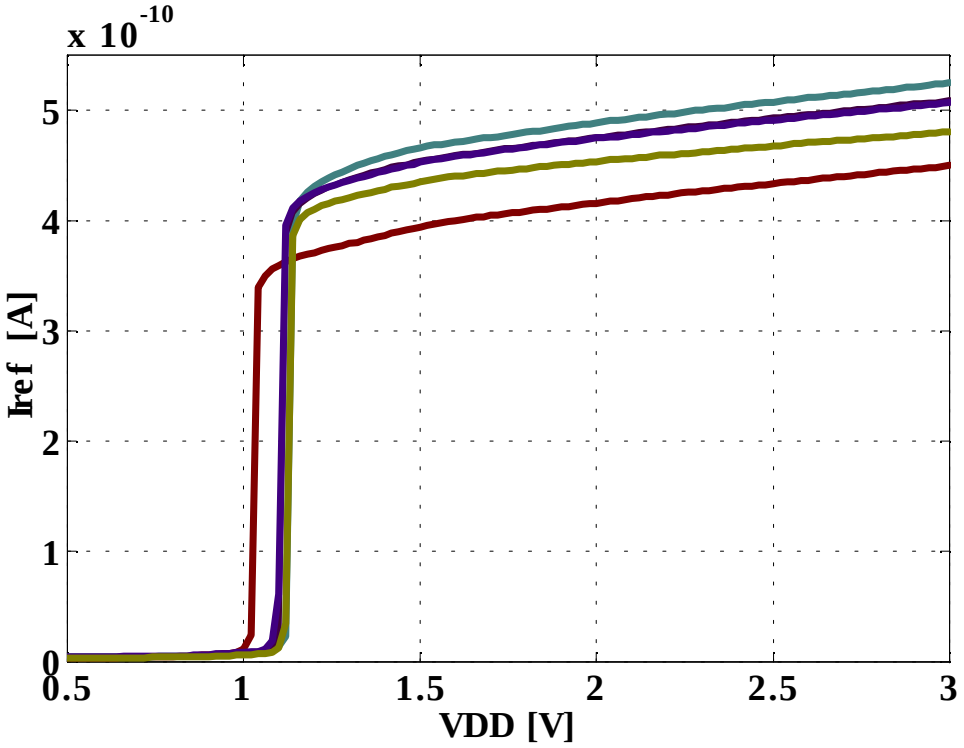
Transistor	W [μm]	L [μm]	i_f
M_1	4	18x60*	10.2
M_2	4	15x60 *	3
M_3	10	10	0.03
M_4	4x10	10	0.0033
$M_{5\text{-}7,\,10}$ &	4	16	0.16
$M_{8\text{-}9}$ &	10	10	0.016

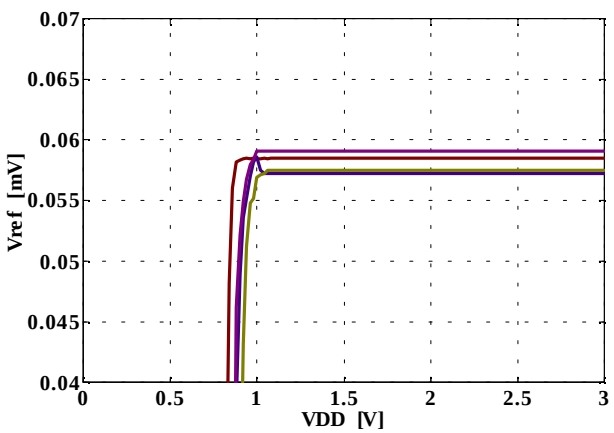
&Trapezoidal transistors. Dimensions of transistor connected to the source are W and L while the one connected to the drain is sized 5W and L.

* Series association of 18 (15) transistors having W=4μm and L=60μm.

5. Results

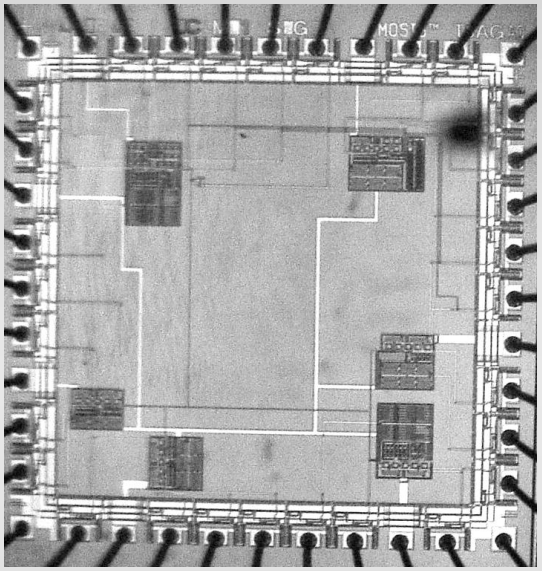
Experimental (1.5um)

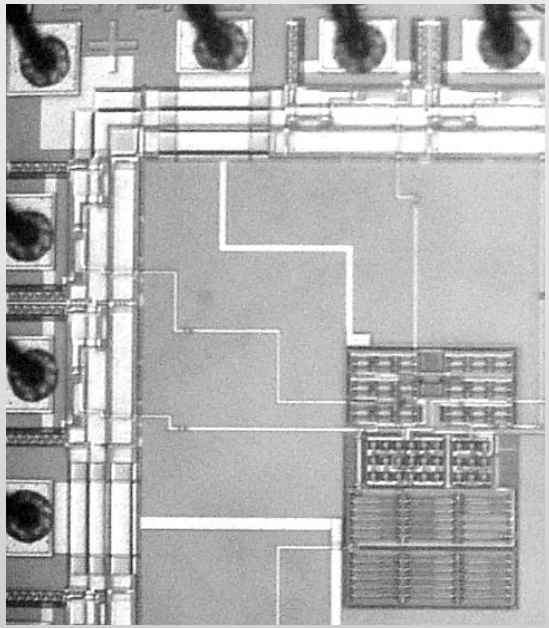


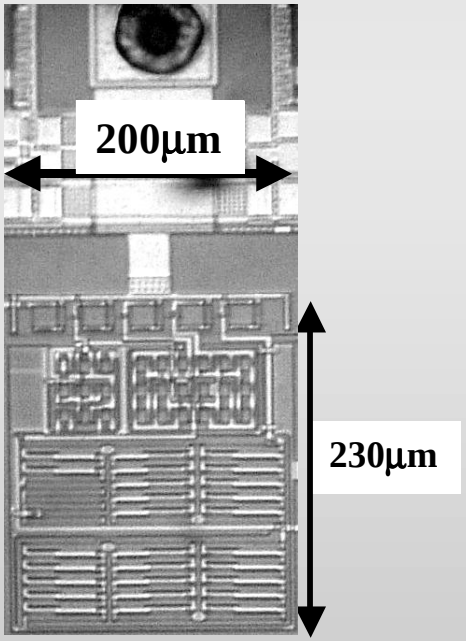


5. Results

Micrograph (1.5um)







6. Summary and conclusions

- Successful generation of current references of the order of 400 pA in AMIS 1.5µm (& TSMC 0.35µm);
- The consumption of the core cell is $4*I_{ref}$ or $3*I_{ref}$;
- Experimental results demonstrated the design correctness;
- Circuit operates from 1.1 V in 1.5 µm technology and potentially operates from 0.7 V in 0.18 µm technology;
- Performance of the self-biased current reference is better than other SBCS reported so far.

Acknowledgments

We are specially indebted to MOSIS for providing us access to silicon