CMOS Rectifier Design for Energy Harvesting based on Vibrations

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Abstract— **This paper describes an approach for harvesting electrical energy from mechanical vibrations with a low-cost piezoelectric element operating at low amplitude vibration (a < 2m/s^2 or voltage generated < 300mV). The converter consists of an ordinary piezoelectric buzzer and a steel ball bonded onto it. Furthermore, the design of the CMOS AC-DC based on the voltage multiplier and for which simulation and measurements results are discussed.**

I. INTRODUCTION

The micro-sensor networking has been identified as one of the 21 most important technologies of the 21st century [1] and as one of 10 emerging technologies that will change the world [2]. Cheap and smart devices networked through wireless links and the internet deployed in large numbers, provide unprecedented opportunities for monitoring and controlling homes, cities, and the environment [3].

One of the most challenging issues in this area is the development of energy sources that can supply enough power for wireless communication of sensed data. Investigation has focused on batteries and ambient power scavenging to provide power for sensor networks. A typical application is the monitoring of industrial machinery, where the vibrations are continuous..

For energy sources, such as batteries, solar cells and vibrations with lifetimes of 3 years or longer (as will usually be the case), solar energy and vibrations are the best options, because small size batteries can't provide enough energy for wireless sensor nodes (roughly, 100 microwatts average power dissipation) [4].

Commercial solar cells have around 20% of efficiency [5], but adequate light sources are not always available. Otherwise, piezoelectric vibration-based systems seem to be an attractive and practical solution, combining good power density and availability of primary source. Efficiency above 50% is easily obtained.

In the industrial environment, the vibrations have acceleration amplitude varying between 0.1m/s^2 and 10m/s^2 with frequencies between 50Hz and 120Hz (g=9,81m/s^2) [6]. Thus, the piezoelectric ceramics produce alternate voltages ranging from hundreds of milivolts to a few volts.

Previous works [7]-[9] have focused on IC power management and techniques to improve efficiency.

The main goal of this work is to focus in the operation for low amplitude vibrations (0.4g or smaller) harvesting electrical energy for (re)charging a battery or a capacitor.

II. CIRCUIT DESCRIPTION

The energy scavenging system includes an electric power generator (piezo transducer or buzzer), a storage device (capacitor), and an AC-DC converter. The system is electrically self-powered. An essential characteristic of this energy scavenging circuit is the capability of converting small energy amounts to suitable values of charge for charging a capacitor, which in turn is use it for powering electronic circuits. In this paper, we discuss and simulate a CMOS AC-DC converter with the functions mentioned above.

A. Generator : Mechanical Structure

A full custom design of a piezogenerator using special piezoceramics with high conversion factor is possible but it is a high cost solution. An alternative way is to use a cheap on-the-shelf device (buzzer) maximizing the conversion by using a mass bonded to the piezoceramic [10]. This configuration generates voltages of around hundreds of milivolts at low vibration amplitude (dozens to hundreds of milig).

A vibrating piezoelectric device generates an AC voltage while electrochemical battery or electronic devices require a DC voltage, hence the first stage needed in an energy harvesting circuit is an AC-DC converter connected to the output of the piezoelectric device.

B. Generator : Electrical Structure

The majority of industrial machinery produces vibrations with small amplitudes, thus the voltage generated by the

piezoelectric ceramic (buzzer) will also be small (150mV to 1V). This voltage is insufficient to power an integrated circuit. To resolve this problem, a voltage multiplier can be used to increase the voltage to values compatible with the integrated circuits.

These multipliers voltage can be designed using the classical structure (fig.1) [11]. The topology (a) is more useful to implementation in an integrated circuit, because the output current is independent of the number of stages, the efficiency can be archived with high parasitic capacitance. The parasitic capacitance can be reduce placing the bottom electrode of the capacitors C2, C2,n to ground and bottom electrode of the capacitors C1, C1,n to the generator, and so the input capacitance of the voltage multiplier will be greater, but it is not a problem, because the generator has capacitance of 65nF. The parasitic capacitance reduce the voltage in the nodes, and so the voltage in the output.

The principal problem of this topology is the threshold voltage of the diodes. Some techniques can be implemented, like as a floating gate structure [12] and threshold cancellation [13]-[15]. Threshold voltage cancellation techniques have an implementation simpler than the floating gate structures.

How the base of this voltage multiplier is a diode, is important to know their possibilities.

1) Voltage Multiplier

The number of stages depends on the technology used and desired output voltage. Recent technologies (0,13µm) have lower threshold voltage and so the number of stages will be less than in the CMOS 0,5µm. Moreover, the CMOS 0,13µm process is more expensive than 0,5µm process.

To save silicon area one possibility is to use MOS gate capacitor (MOSCAP) rather than poly-poly capacitor, but the design should consider the nonlinearity of capacitance.

The nonlinearity of the capacitance of the MOSCAP is an important factor, because in the operation range of this work (hundreds of milivolts) the value of the capacitance may vary around 40% to 80% of the desired value. So, the energy transferred from one stage to another will be affected [16] and the time response will change too.

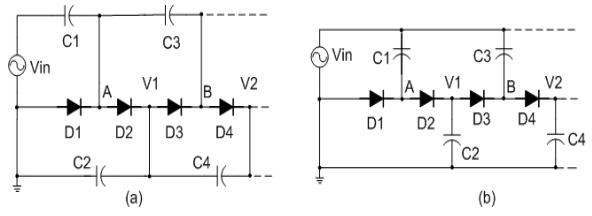


Figure 1. Classical voltage multiplier structure [11].

The structures of fig. 2 present different possibilities of ligations of the MOS transistor tied diode and were simulated in the Eldo Spice of Mentor Graphics suite.

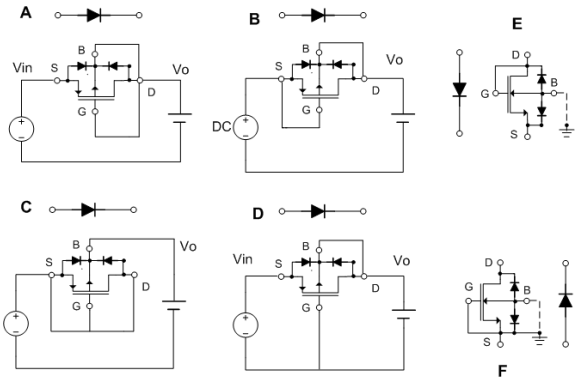


Figure 2. Diodes in the CMOS conventional process.

To know the contribution of the junction diode and the MOS diode (transistor tied diode) to drain current, the ACM [17] model was used with numerical software. In general, all diodes of the voltage multiplier will operate in the weak inversion, and the follows equations were written considering this condition.

Inspecting the topologies in fig. 2 we can observe that:

a) In the structure C, the drain current is composed only by current of the junction diode.

b) In the structure B, the drain current is composed by the currents of junction and MOS diodes. The structure B has a drawback in voltage multiplier application: if the input voltage (v_{SB}) is negative, current will flow from output to input, and this condition is undesirable.

c) The drain current of structure A and D is composed of the currents of junction diodes and MOS.

d) In the standard CMOS process, the NMOS transistor has the bulk terminal connected to the ground (fig. 2 A and B). If the source terminal not connected to the same potential, the threshold voltage will increase reducing the efficiency of converter. This is more evident with increasing the number of stages of the voltage multiplier(using the structure of fig. 2 E).

So, the structures A and D are more appropriated to application with low voltage, because the currents involved in the application of this work are very small (nA to µA) and any contribution in the drain current is important.

Then, we fixed this analysis in the structures A and D, because they are more appropriate for the desired application (150mV to 300mV) and it will be analyzed with more details.

The drain current of topology A, and D are expressed respectively by equations (1) and (2). The first part of these equations, are referent of junction current of junction diode and the second part to the MOS diode.

$$i_{D\_A} = I_{S\_JUNC} \cdot \left[\exp\left(\frac{V_{SB}}{n \cdot \phi_t} \right) - 1 \right] + \\ + 2 \cdot e^{1} \cdot I_{S\_MOS} \cdot \exp\left(\frac{V_T}{n \cdot \phi_t} \right) \cdot \left[\exp\left(\frac{V_{SB}}{\phi_t} \right) - 1 \right] \quad (1)$$

$$i_{D\_D} = I_{S\_JUNC} \cdot \left[\exp\left(\frac{V_{SB}}{n \cdot \phi_t} \right) - 1 \right] + \\ + 2 \cdot e^{1} \cdot I_{S\_MOS} \cdot \exp\left(\frac{V_T + Vbg}{n \cdot \phi_t} \right) \cdot \left[\exp\left(\frac{V_{SB}}{\phi_t} \right) - 1 \right] \quad (2)$$

Where: n is the slope factor, V_T is the threshold voltage, ϕ_t is the thermal coefficient, I_{S_MOS} and I_{S_JUNC} are the saturation current of MOS diode of junction diode respectively .

In the structure B (eq. 2), the term V_{SB} (= V_{in} - V_o) in the exponential reduce the current of MOS diode and so, the drain current. In the structure C (eq. 3), only the junction diode contributes in the drain current

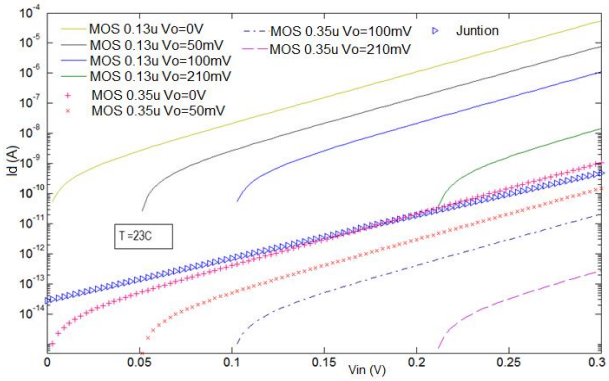


Figure 3. Id vs Vin of structure A in IBM 0.13µm and TSMC 0.35µm technologies T=23°C.

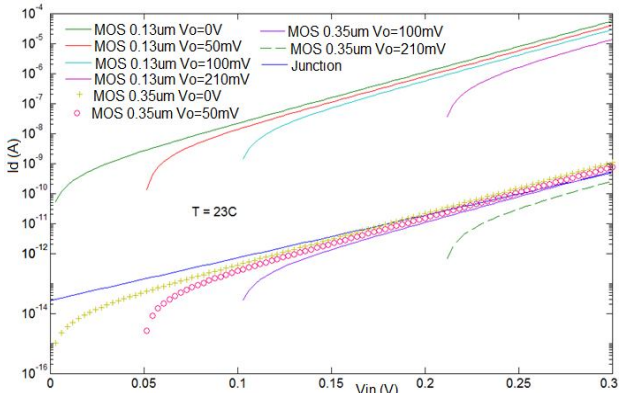
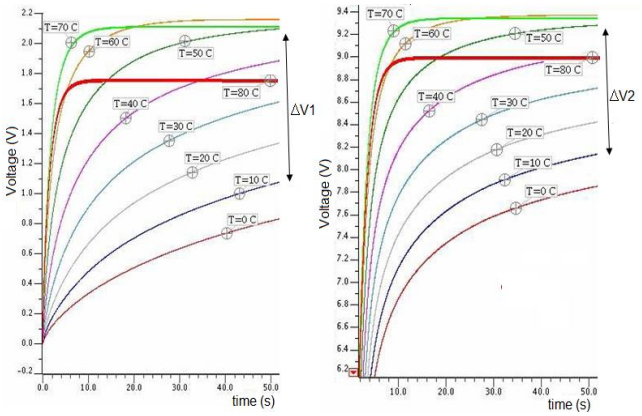


Figure 4. Id vs Vin of structure D in IBM 0.13µm and TSMC 0.35µm technologies for T=23°C.

Fig.3 and fig.4 show the effect of the technology in the drain current. For IBM 0.13µm the drain current reaches 55µA and in the TSMC 0.35µm reaches 1.2nA. The junction diode contributes with 350pA. These figures show that the topology D is better than topology A. However, with the increase of input voltage, the reverse current of the MOS transistor tied diode increase too. The topology D is adequate to operate up to 300mV of input voltage. Above this voltage, the structure A is most appropriate, because the reverse current is very lower than the direct current. By example, for input voltage of 300mV, the structure A has a ratio of direct and reverse currents of 40 times, while the structure D has a ratio of 5 times. This means that, the structure D has a ripple voltage greater than the structure A.

These data are important, in choice which technology is adequate to the desired application. The principal effect of the technology is the reduction of the threshold voltage. However, the temperature is an important variable, principally in the weak inversion.



(a) Vo multip 11 est. vs temp. TSMC 0.35µm Vin=150mV.

(b) Vo multip 11 est. vs temp TSMC 0.35µm Vin=500mV.

Figure 5. Temperature effect in a 11 stages multiplier.

The figure 5 shows the effect of the temperature in an 11 stages multiplier simulated in the TSMC 0.35µm. In the case (a) (Vin=150mV), the effect of the temperature is much more important than with Vin=500mV (ΔV1=100% and ΔV2=20%), in the range 10°C-50°C, which is a range of temperature variation in a industrial environment.

2) Voltage multiplier – Topology with MOS transistor

The figure 6 shows the voltage multiplier topology with the respective MOS transistor tied diode.

The dashed area is the fundamental part of multiplier, because the voltage multiplied by another stages, depends on of first stage. So, is important to analyze the possibility to improve efficiency to this stage.

We perform a comparison with three different structures to the base of multiplier (MP1 and MN1), showed in the figure 7.

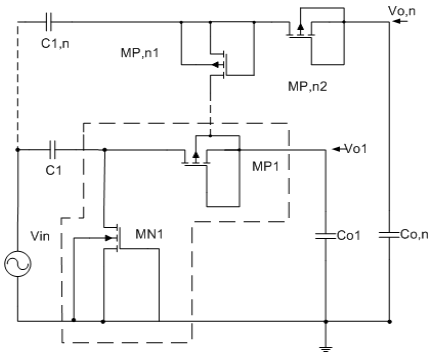


Figure 6. Topology of voltage multiplier with MOS transistor tied diode.

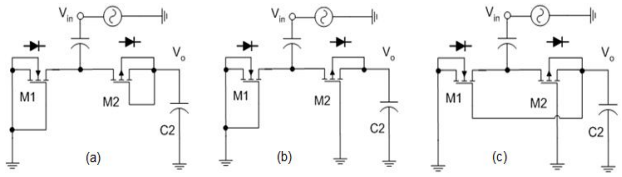


Figure 7. Three differents aproches to the base of multiplier.

Table I shows the simulated voltage of the topologies of the figure 7. In this table, we can see that up 300mV, the topologies (b) and (c) [4] have the higher DC voltage. The circuit was simulated in Eldo Spice of Mentor Graphics for technology TSMC 0.35µm, with W=120µm and L=0.5µm and capacitors of 30pF.

TABLE I. SIMULATED VOLTAGE OF TOPOLOGIES OF FIG. 7

Vin (Vac peak)	Vo(DC) (a)	Vo(DC) (b)	Vo(DC) (c) [13]
100m	72m	114m	114m
150m	111m	199m	175m
300m	197m	230-250m	182m
500m	376-371	250-494m	214-227m

One of the important tradeoffs in the design of the voltage multiplier is the size of the transistor versus parasitic capacitances. The channel width can be reduced to a few times the minimum width to reduce parasitic capacitance. However, the reduction in channel width causes a decrease the charge current capability of the diode-connected transistors, and so increasing the numbers of stages.

As the number of rectifier stages increases, the capacitive component of the multiplier input impedance increases thus reducing the reactive component of the multiplier input impedance. With this, the maximum voltage gain that can be achieved is also decreased at the same rate since the resistive component in the input impedance stays fairly constant

We simulated transistor with W=30µm - 960µm, and the unique perceived effect was the reduction of time of charge of capacitors, without significant variation in the output voltage. We simulate to respect of dimension of capacitor too. So, we founded the components that maximize the ratio of silicon area and performance. The results are: transistor W=120µm and L=0.5µm and capacitor with 10pF in the TSMC 0.35µm technology.

III. MEASUREMENTS - GENERATOR

The energy converter consists of a steel ball attached onto an ordinary piezoelectric buzzer. The mass bonded weighs 65grams and the buzzer has the following dimensions: metal diameter (dm=50mm), metal thickness (hm=0.3mm), piezo diameter (dp=28mm) and piezo thickness (hp=0.20mm).

The mechanical vibrations were generated by a moving electromagnetic shaker (manufacturer Bruel and Kjcer) with a sinusoidal voltage.

Fig. 8 presents the setup of measurement of the buzzer. Fig.9 present the measured power generated by the piezogenerator as function of the resistive load and acceleration of vibrations. These data are important to determinate the number of stages of voltage multiplier to determinate application.

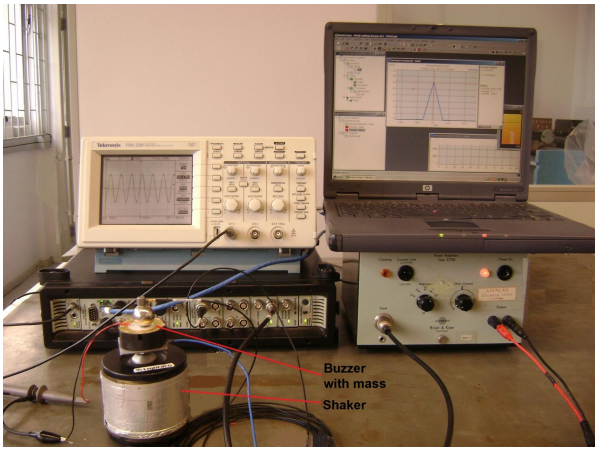


Figure 8. Measurements setup of the buzzer.

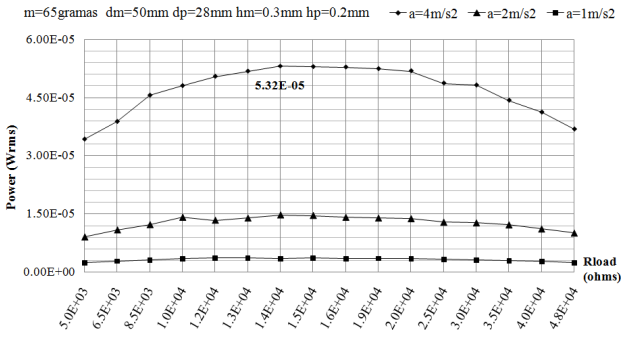


Figure 9. Measured power generated by the piezogenerator vs resistive load and acceleration.

Fig. 9 shows important information: the power falls with the square of acceleration as expected [4]. This data is

important to be used with the voltage by buzzer generated (and number of stages of the voltage multiplier), to define what kind of industrial machinery can be monitored using vibrational energy through buzzers.

Considering that the buzzer is operating at resonance frequency, and using the electromechanical model [19]. The voltage generated by buzzer is:

$$Vo = \frac{-j \cdot m \cdot a \cdot N^{*} \cdot R_L}{Z_m \cdot (w \cdot R_L \cdot C_P) - j \cdot (R_L \cdot N^{*2} + Z_m)} \quad (3)$$

N* is the transformer coefficient [20], *m* is the mass added, Z_m is the mechanical impedance [19], C_P is the buzzer capacitance [20], R_L is the load resistance. The buzzer characteristics were cited above.

Fig. 10 shows a good agreement between the model of eq. 3 and the measurements. This data is important to define the number f stage of the voltage multiplier by function of load and desired output voltage

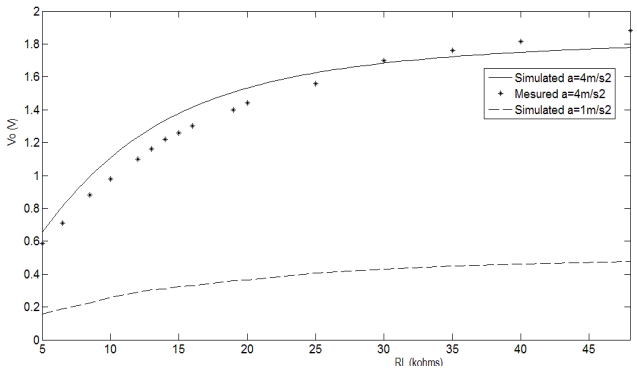


Figure 10. Voltage output measured and simulated of multiplier eq. (3).

IV. MEASUREMENTS – VOLTAGE MULTIPLIER

This session will present the comparative measurements between multipliers designed in technologies AMIS 0.5µm and TSMC 0.35 µm.

Table II presents the measurements of the output voltage of two multipliers designed in technologies AMIS 0.5µm and TSMC 0.35 µm. Table II also shows for AMIS 0.5µm technology, the multiplier starts to operate from a voltage generator up to 400mVac peak. On the other hand, the multiplier designed in the technology TSMC 0.35µm, begins to operate at voltages above 150mVac peak.

The match between the output generator and the input voltage multiplier will not discuss in this work, but roughly (neglects losses and capacitive effects) its can be founded by [18] and its shows in Eq.4.

$$R_{IN\_MULTIPLIER} = R_D / N = R_{LOAD} / (2xN) \quad (4)$$

N = number of stages R_D = Diode Resistance.

Eq.3 shows that input impedance of voltage multiplier decrease with the increment of number of stages and so its affect the power transfer.

From Eq. 4 and to maximize power transfer: ($R_{IN\_MULTIPLIER}$ = Rpiezo= resonant impedance of the piezoceramic), the optimum load resistance will be:

$$R_{LOAD} = 2xNxR_{PIEZO} \quad (5)$$

From fig. 9 we can note that the resistance that provides more power is equal to 13kΩ. Thus, using the eq. (4) the optimum load resistance will be:

$$R_{LOAD\_IDEAL} = 2xNx13k\Omega = Nx26k\Omega \quad (6)$$

TABLE II. MEASURED DC OUTPUT VOLTAGE OF A TWO STAGES MULTIPLIERS FABRICATED IN AMIS 0.5µ AND TSMC 0.35µ TECHNOLOGIES.

Vgenerator (Vpeak AC)	Vo2(Vdc) AMIS 0.5µm	Vo2(Vdc) AMIS 0.5µm	Vo2(Vdc) TSMC 0.35µm	Vo4(Vdc) TSMC 0.35µm
0.1	NPM *	NPM *	0.15	0.25
0.15	NPM *	NPM *	0.202	0.41
0.2	NPM *	NPM *	0.23	0.49
0.3	NPM *	NPM *	0.38	0.7
0.4	0.55	0.78	0.51	1.02
0.5	0.65	1.1	0.65	1.3
0.8	1.0	2.0	--	--

NPM* = not possible to measure.

The voltage multiplier has been simulated and designed with Mentor Graphics Design suite, using AMIS 0.5µm CMOS process, AMS 0.35µm and TSMC 0.35µm processes. The layout of the voltage multiplier with 25 stages AMI 0.5µm is shown in fig.11. The fig. 12 shows the layout sent to fabrication in AMS 0.35µm technology.

Using an AMI 0.5µm CMOS process are necessary 25 stages to achieve the desired output voltage. Moreover, in AMS 0.35µm CMOS process, are necessary 11 stages only.

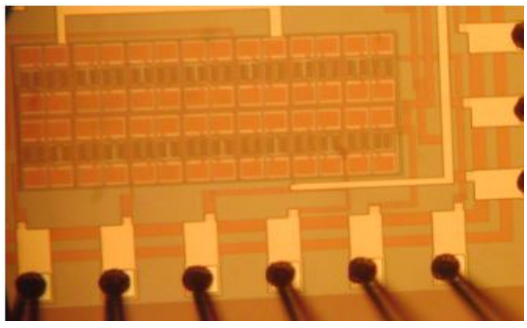


Figure 11. Microphotograph of a 25 stages voltge multiplier fabricated in AMI 0.5µm process.

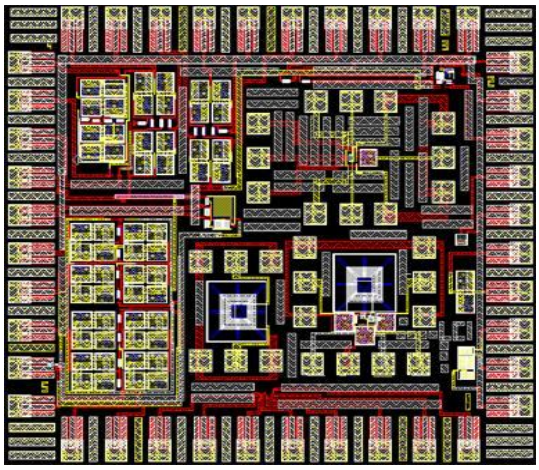


Figure 12. CMOS voltage multiplier, control and test structures designed with AMS 0.35µm process.

V. CONCLUSIONS

In this paper was analyzed the output performance of an energy harvester consisting of a piezoelectric generator and a voltage multiplier. The piezoelectric generator is assembled with a low-cost piezoelectric buzzer and uses mechanical vibrations as input. Its response was measured as a function of the input vibration amplitude and output load. Several voltage multipliers topologies were simulated for optimization of devices sizes and number of stages.

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