A Gm-C BUMP EQUALIZER FOR LOW-VOLTAGE LOW-POWER APPLICATIONS

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ABSTRACT

A low-voltage low-power 2nd-order CMOS pseudo-differential bump-equalizer is presented. Its topology comprises a bandpass section with adjustable center frequency and quality factor, together with a programmable current amplifier. The basic building blocks are triode-operating transconductors, tunable by means of either a DC voltage or a digitally controlled current divider. The bump-equalizer as part of a battery-operated hearing aid device is designed for a 1.4V-supply and a 0.35µm CMOS fabrication process. The circuit performance is supported by a set of simulation results, which indicates a center frequency from 600Hz to 2.4kHz, 1≤Q≤5, and an adjustable gain within ±6dB at center frequency. The filter dynamic range lies around 40dB. Quiescent consumption is kept below 12µW for any configuration of the filter.

1. INTRODUCTION

Graphic equalizers are filters aimed to change the amount of equalization without altering the shape of the transfer characteristic [1]. Particularly, bump-equalizers [1] - [3] are applied in audio systems to provide hearing-impaired people with improved sound quality by equalization of the frequency response. Implementations of bump-equalizers using either MOSFET-C [1] or switched-capacitor techniques [2], [3] have already been reported.

This work focuses on the design of a parametric equalizer intended for hearing-aid applications. The 2nd-order low-voltage low-power (LVLP) continuous time bump-equalizer comprises a bandpass section and a programmable current amplifier. The main building block is an OTA, whose small-signal transconductance depends linearly on the drain-to-source voltage of the input MOSFET operating in the triode region [4], [5]. One of the most appealing features of our filter is that the building blocks, namely the programmable current mirror, the Q-control block, and the common-mode feedback circuit are derived from the basic transconductor topology. Moreover, the tuning strategy is very simple – an external DC voltage directly tunes the bump-equalizer center frequency f_o, while two digital words control the Q-factor and the bump/dip coefficient.

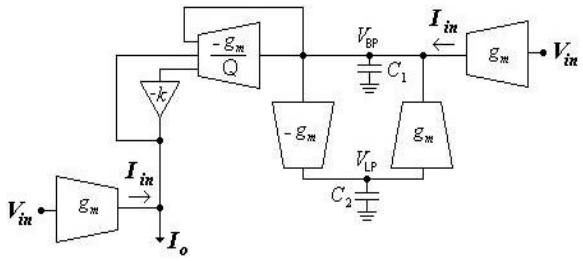

Figure 1 - Block diagram of the bump equalizer.

This communication is organized as follows. Section 2 describes the bump-equalizer structure. Fundamentals of the transconductor as well as topologies of elementary building blocks of the filter are presented in Section 3. Simulation data are presented in section 4. Concluding remarks are summarized in Section 5.

2. BUMP-EQUALIZER TOPOLOGY

Figure 1 shows the block diagram of the proposed gm-C bump-equalizer, made up of a classical two-integrator loop filter followed by a programmable current mirror that adjusts the bump/dip factor *k* and a summing node at the output. For $C_1=C_2=C$, the filter transfer function is

$$\frac{I_o(s)}{V_{in}(s)} = g_m \frac{s^2 + k\frac{g_m/C}{Q}s + \left(\frac{g_m}{C}\right)^2}{s^2 + \frac{g_m/C}{Q}s + \left(\frac{g_m}{C}\right)^2} \qquad (1)$$

Even though Figure 1 shows a single-ended topology, we have implemented a fully differential version of the bump equalizer. The implementation of the building blocks in Figure 1 will be discussed in the next section.

3. BASIC BUILDING BLOCKS

3.1) Transconductor circuit

The simplified schematic of the pseudo-differential transconductor is shown in Figure 2 [4], [5]. Table I lists the transistor drawn sizes with respective drain currents.

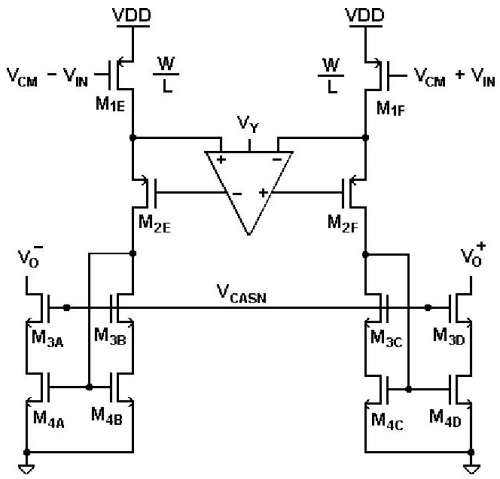

Figure 2 – Transconductor circuit.

Table I – Transconductor transistor-sizing and drain current for V_{TUNE}= 100mV. Simulated g_m= 96nA/V.

Transistor	W (μm)	L (μm)	I_D (ηA)
M1	1.05	40.6	15.4
M2	1.05	2.1	15.4
M3, M4	1.4	2.8	15.4

Regulation amplifiers [5] with a high voltage-gain maintain M_{1E} and M_{1F} in the triode region by setting their drain voltages at V_Y. Such a bias condition gives a linear dependence of the small-signal transconductance g_m with V_{TUNE} according to

$$g_m = \frac{\partial I_D}{\delta V_{in}} = \frac{W_1}{L_1}\mu_p C_{ox}^{'} V_{TUNE} \qquad (2)$$

where the tuning voltage $V_{TUNE} = V_{DD} - V_Y$.

Both offset-voltage of the regulation amplifier and noise level impose a lower bound for V_{TUNE}, which is safely kept over 30mV in our design. In some blocks of the equalizer, we have used current mirrors to invert the output currents of the transconductor cell, as shown in Figure 2. The high-swing MOS cascode bias circuit described in [6] has been used to generate V_{CASN}. The CMFB circuit (Figure 3) provides the bias currents at the output nodes of the transconductor cell. The g_m-stage output conductance is inherently low since a cascode current mirror with moderately long-channel devices has been employed.

3.2) Common-mode feedback circuit

The CMFB circuit depicted in Figure 3 is a replica of the adopted transconductor. The CMFB circuit output is connected to the transconductor output to provide the DC current for correct operation of transconductors and operates as follows. The gate voltage V_{CM} determines the DC output current I_{CM} of the transconductor in Figure 2. The DC current of the CMFB circuit in Figure 3 is determined by the arithmetic mean of V_o^+ and V_o^-. Since KCL imposes the same current I_{CM} for both the transconductor and CMFB circuit outputs, then the arithmetic mean of V_o^+ and V_o^- equals V_{CM}.

Note that one controls the center frequency g_m/C by changing g_m through V_Y in both transconductor and CMFB block, the latter responsible for the generation of the bias current. Therefore, V_{CM} deviations against g_m variations are kept at a minimum.

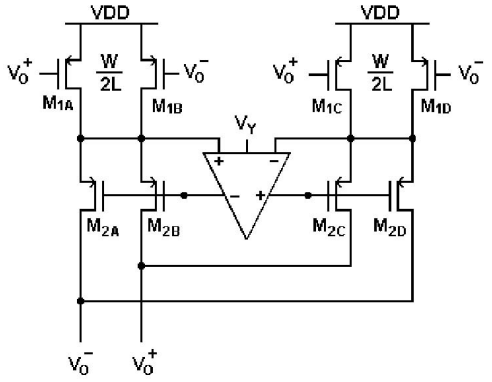

Figure 3 - Common-mode feedback (CMFB) circuit

3.3) Q-control circuit

A straightforward way to control the Q-factor is simply to deviate a fraction of the transconductor output current from the output node to V_{SS}, as illustrated in Figure 4, where M_{Q1}, M_{Q2}, M_{Q3}, M_{Q4}, and M_{Q5} are equally sized transistors. Denoting g_{m1G} the transconductance of M_{1G}, the output current equals $g_{m1G} \cdot v_{in}$ if all switches are open.

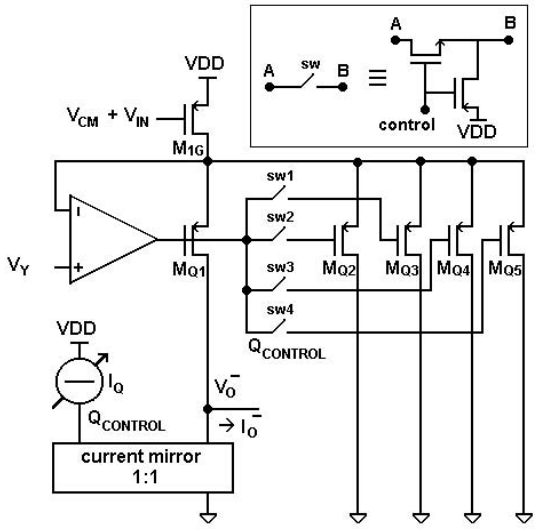

Figure 4 - Q-control transconductor

For the sake of simplicity both of the Q-control and *k* block are represented as single-ended topologies.

In the Q-control block, the switches are closed according to a thermometer code; therefore, if one switch is closed, the output current is $g_{mM1G}v_{in}/2$, if two switches are closed, the output current is $g_{mM1G}v_{in}/3$ and so on. The variable current source I_Q has a switching scheme similar to the one shown in Figure 4 in order to provide the Q-control transconductor with the appropriate bias current, which must change in accordance with the desired Q.

3.4) Programmable current mirror (k-block)

The programmable current gain block (*–k*) is a combination of a cascode current mirror followed by I-to-V and V-to-I converters, as illustrated in Figure 5. The output current of the *–k* block is determined by a set of switches whose ON/OFF states determine *k*.

When all switches are open the mirror gain is +6dB due to the fact that the W/L ratio of transistor M_{1J} is twice as large as the W/L ratio of input transistor of the transconductor in Figure 4. In the k-control block, the switches are closed according to a 1-of-n code. Transistors M_{k1}, M_{k2}, M_{k3}, and M_{k4} were sized so that the closure of sw1, sw2, sw3, and sw4 would produce, respectively, a +3dB, 0dB, -3dB, and –6dB gain at the center frequency. The dimensions of the transistors involved in the k-control are listed in Table II.

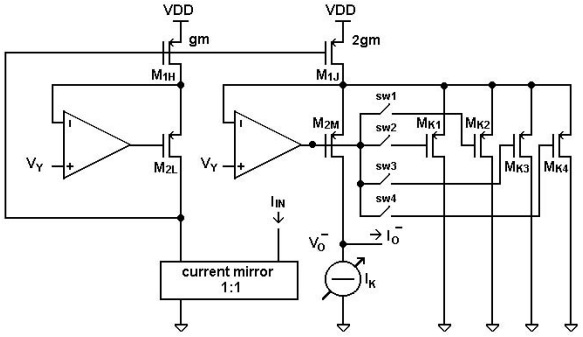

Figure 5 - Programmable current mirror (k-block)

Table II – Dimensions of k-control transistors.

Transistor	W (µm)	L (µm)
M_{1H}	1.05	40.6
M_{1J}	2.1	40.6
M_{2M}	2.1	2.1
M_{K1}	2.1	4.8
M_{K2}	2.1	2.1
M_{K3}	3.4	2.1
M_{K4}	6	2.1

4. SIMULATION RESULTS

A test chip for the g_m-C bump equalizer was designed based on a 0.35µm CMOS process. The regulation amplifier for all filter blocks was realized by a fully differential folded-cascode OTA, similar to the one reported in [5] but with n-channel input differential pair. A high-swing MOS cascode bias circuit [6] complies with the requirement of a low-voltage supply. Both capacitors C_1 and C_2 are 10 pF. Simulation was carried out with SMASH simulator and Bsim3v3 MOSFET model.

Figure 6 features the simulated frequency response of the bump-equalizer for different center-frequency values (V_{TUNE} at 40, 68, 113, and 200mV). The nominal Q corresponds to 1, whereas the nominal dip factor was set to –6dB. Figure 7 presents the frequency response of the equalizer for Q= 1, 2, 3, 4, and 5. The center frequency is 1.4 kHz (V_{TUNE} = 100mV), and the gain at the center frequency is -6dB. Finally, Figure 8 displays the simulation results for programmable gains of 6, 3, 0, -3, and - 6dB.

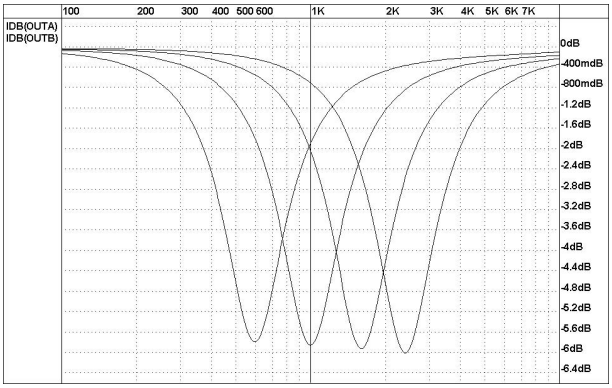

Figure 6 - Simulation results for center frequency programmability (Q = 1). f_0 = 0.6, 1, 1.6, and 2.6kHz; V_{TUNE} = 40, 68, 113, and 200mV respectively.

Upon the condition f_0=1kHz, Q=1, and k=+6dB, noise and harmonic distortion simulations using the SMASH simulator resulted in a dynamic range of 42dB, as shown in Figure 9. The noise power is the result of the integration of the power spectral density over the audio-frequency range.

Keeping f_0 constant at 1kHz, different programming setups of the filter resulted in the dynamic ranges presented in Table III. The quiescent power consumption depends slightly on the center frequency of the filter (V_{TUNE}), and varies from 11 to 12 µW.

Table III – Dynamic range (DR) for different values of gain and quality factor (f_0 constant at 1kHz).

Q	K (dB)	DR (dB)
1	+6	42
1	-6	32
5	+6	35
5	-6	35

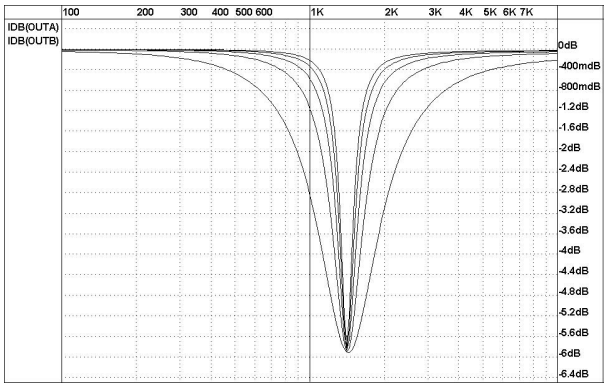

Figure 7 - Bandwidth programmability for Q=1, 2, 3, 4, and 5.

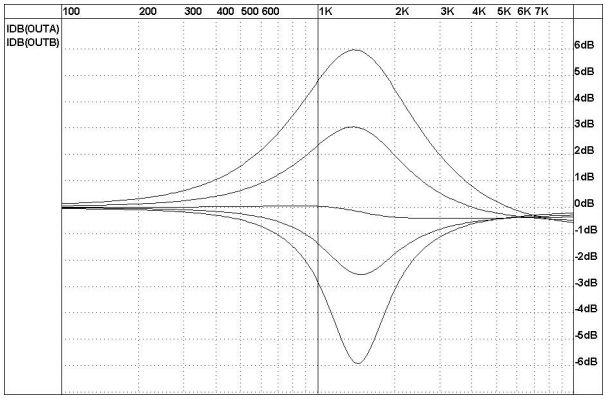

Figure 8 -Simulations results for bump/dip gain programmability k=6dB, 3dB, -3dB, -6dB.

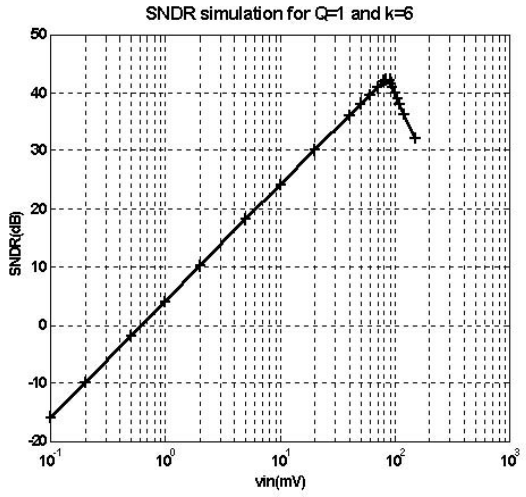

Figure 9 – SNDR simulation for Q=1 and a 6dB bump.

5. SUMMARY AND CONCLUDING REMARKS

A LVLP pseudo-differential continuous-time, 2nd-order bump-equalizer topology was introduced. The circuit was designed according to a standard 0.35µm n-well CMOS fabrication process and a single 1.4V-supply.

As a possible application of the proposed topology, a bump-equalizer as part of a battery-operated integrated circuit for a hearing-aid device can be implemented. Circuit simulations supported with Smash and Bsim3v3 models met the specified project parameters for quality-factor, center frequency and gain. The equalizer maximal quiescent consumption is only 12 µW. The filter dynamic range lies around 40dB. The layout is now being prepared so that the equalizer can be prototyped and characterized.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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