# Resizing Rules for the Reuse of MOS Analog Designs

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**Abstract**

*This paper presents a redesign procedure for analog circuits based on a scalable model of the MOSFET. A set of very simple expressions allows the calculation of transistor dimensions and bias for a given circuit in a new generation technology, starting from the circuit designed in an earlier technology.*

## Introduction

The advent of deep submicron processes has enabled the system-on-chip (SOC) design and enlarged the gap between design complexity and designers productivity. Time-to-market pressure makes this gap more challenging, and consequently, a more efficient design methodology is mandatory. Systematic design reuse is expected to be a practical solution for the design of SOC [1-2], and various forms of the reusable functional blocks also called cores or intellectual property (IP) are available. IP providers offer soft, firm and hard cores for digital circuits [1-2]. The first are delivered in a hardware description language and the last are mask layouts designed for a specific technology. For analog functions, potentially reusable blocks are available only as hard cores [3-4]. A basic difference between digital and analog circuits is that, for conventional digital circuits, transistor geometry is usually the only degree of freedom for design, while for analog circuits, bias is an additional and fundamental variable [5]. In one of the most common analog blocks, the amplifier, transistors can operate in the strong, moderate or weak inversion regions, depending on the design specifications [5-6]. For digital circuits the primary tradeoff is between speed and power dissipation, but analog circuits are designed considering other specifications such as signal-to-noise ratio (SNR) and gain. Since CMOS technology is scaled to improve the integration of digital circuits, the migration of an analog design to a new technology is not obvious and usually involves a complete redesign [4, 7]. In this paper we use a physics-based MOSFET model [8] to develop a methodology for the technology migration of analog circuits. We derive simple formulas that allow us to calculate transistor dimensions and bias for a given circuit in a new generation technology, starting from the circuit designed in an earlier technology. The MOSFET model employed here is particularly suited for the (re) sizing of transistors because it has one equation for all the operation regions, uses normalized variables and few physical parameters.

## MOSFET model

The model in [8] was developed considering the needs of analog designers: it uses the current as the main variable and has accurate expressions for the small-signal parameters in all the operation regions. The following set of equations developed in [8] can be readily used for MOSFETs operating in saturation:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_d}} \qquad (1.a)$$

$$i_d = \frac{I_D}{I_S} \qquad (1.b)$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \qquad (1.c)$$

The transconductance-to-current ratio of MOSFETs given by (1.a) is a universal relationship for MOSFETs, being independent of technology, dimensions and temperature. $I_S$, the normalization current, depends on the aspect ratio (W/L) and technological parameters: mobility $\mu$, and oxide capacitance per unit area $C'_{ox}$. $\phi_t$ is the thermal voltage and n is the slope factor, which is slightly greater than one and almost bias-independent [8]. $i_d$ is the normalized drain current [8] or inversion level [9]. As a rule of thumb, values of $i_d$ greater than 100 characterize strong inversion, the transistor operates in weak inversion up to $i_d$=1 and intermediate values of $i_d$ from 1 to 100 indicate moderate inversion.

The intrinsic cutoff frequency of a MOSFET [11] in saturation

$$f_T = g_m/2\pi(C_{gs}+C_{gb}) \qquad (2a)$$

is approximated in [8] by

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$$f_T \cong \frac{g_m}{2\pi\left(\frac{1}{2}C_{ox}' WL\right)} \quad (2b)$$

or, equivalently

$$f_T \cong \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_d}-1\right) \quad (2c)$$

The simple result in (2b) states that, for a constant $g_m$, $f_T$ and area are inversely proportional to each other. Therefore, an important figure of merit of transistors is the ratio of the transconductance to the gate area ($g_m$/WL), which can be denominated area efficiency and is equivalent to the unit gain frequency. This definition is complementary to the definition of current efficiency ($g_m/I_D$) [6].

Finally, an approximate formula for the source-to-drain saturation voltage as function of the inversion level is given by

$$\frac{V_{DSsat}}{\phi_t} \cong \left(\sqrt{1+i_d}-1\right)+4 \quad (3)$$

The very simple set of equations (1-3) models relevant aspects of analog circuits.

Even though the ratio $g_m/I_D$ given by (1.a) has been demonstrated to be valid for long-channel devices where the transversal field dependence of mobility has been neglected, it still holds if degradation of mobility due to vertical field is taken into account. Also, velocity saturation is not relevant in most of the cases because operation of the MOSFET deep in strong inversion is very unlikely in analog circuits, particularly for those operating at low supply voltage.

The maximum voltage gain attainable with a single transistor is limited by the source-to-drain conductance, which is approximately proportional to the ratio of the drain current to the channel length [5, 9]. Thus, $G_v$, the absolute value of the attainable voltage gain of the common-source amplifier can be written as

$$G_v = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D} V_E L \quad (4a)$$

where $V_E$ is the Early voltage per unit length[5, 9]. From (1a) and (4b) it follows that

$$G_v = \frac{2}{n\phi_t\left(1+\sqrt{1+i_d}\right)} V_E L \quad (4b)$$

$V_E$ tends to increase somewhat in strong inversion ([9], Chap. 2 in [10]) and is also slightly dependent of L (Fig. 1). However, as shown in Fig. (1), a constant $V_E$ is a good approximation if the use of short-channel transistors in weak inversion is avoided, a usual practice in analog design [5, 6].

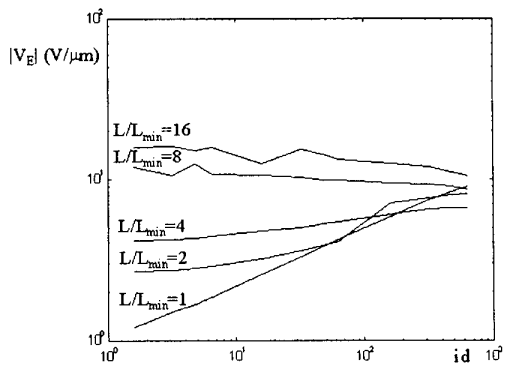


**Fig. 1 Early voltage per unit length $V_E$ vs. inversion level $i_d$ for nMOS transistors from a 1.2μm technology**

## Effects of scaling on analog circuits

In digital circuits, MOS transistors are usually minimum channel length and the channel width W is the only design parameter. On the other hand, in analog circuits each transistor is usually designed considering three independent parameters: the channel width W, the channel length L and the bias current $I_D$ [5]. For analog circuits, the gain-bandwidth product (GB) and the signal-to-noise ratio SNR are two of the most basic specifications. Thus, to analyze the scaling of analog circuits we will consider that GB and SNR are specs to be maintained and that the power-supply is reduced by the scaling factor K [12].

Considering only thermal noise for a purely capacitive load C, the signal-to-noise ratio (7) is

$$SNR = V_{pp}^2 C/8kT \quad (5)$$

where $V_{pp}$ is the peak-to-peak signal swing, T the absolute temperature and k is the Boltzmann constant.

In a single stage amplifier GB is proportional to the ratio of the transconductance to the load capacitance [12]

$$GB = g_m/2\pi C \quad (6)$$

For simplicity, we will first assume $V_{pp}=V_{DD}$ and contant-field scaling of the technology (Table I), but these restrictions will be removed in the next section.

From (5) and (6) it follows that to keep the same SNR and bandwidth if the supply voltage is reduced by the scaling factor K, C and $g_m$ must be multiplied by $K^2$.

To a first order approximation, $V_E$ scales with the square root of the substrate doping concentration $\sqrt{N_{sub}}$ [11]. Values of $V_E$ for 3μm bulk [5] and silicon-on-insulator technologies [6], as well as for a 1.2μm process (Fig. 1) are in the range 5-10V/μm, supporting the fact that $V_E$ is insensitive to technology. Therefore, we will consider $V_E$ constant in this section. The analyses that follow are concerned with three strategies that can be used to keep the same GB and SNR.

Table I Constant-field scaling (11)

| Quantity | Scaling factor K (K>1) |
|---|---|
| Power supply voltage ($V_{DD}$) | $K^{-1}$ |
| Device lateral dimensions (L, W) | $K^{-1}$ |
| Capacitances per unit area (C') | K |
| Doping concentration ($N_{sub}$) | K |
| Early voltage per unit length ($V_E$) | $K^{1/2}$ |

### A. Full scaling: L→L/K, W→W/K

In conventional full scaling the lateral dimensions of the transistor are reduced by the scaling factor K (Table II). From (2b) it follows that the transition frequency increases by $K^3$. Comparing (2b) with (2c) it follows that

$$\left(\sqrt{1+i_d}-1\right)\rightarrow K\left(\sqrt{1+i_d}-1\right) \quad (7)$$

Thus, inversion level increases for full scaling at constant SNR, and the gain is not preserved as can be verified from (4b). The first column of Table II condenses the well-known fact that analog circuit performance is degraded by full scaling [7, 12].

### B. Constant-area scaling: L→L/K, W→KW

From (2b) it follows that the transition frequency increases by K. Comparing (2b) with (2c) it follows that

$$\left(\sqrt{1+i_d}-1\right)\rightarrow \left(\sqrt{1+i_d}-1\right)/K \quad (8)$$

In opposition to full scaling, the inversion level decreases for constant area scaling. The drain current is multiplied by K in strong inversion (SI) and by $K^2$ in weak inversion (WI), as can be easily verified from (1.a). Thus, constant-area scaling at constant SNR and bandwidth keep the power consumption unaltered in strong inversion [7]

As it follows from (4a) gain is kept constant in strong inversion but is reduced by K in weak inversion. Consequently, constant-area scaling is not adequate for weak and for the lower end of moderate inversion, but in these cases the transistors can be resized maintaining the inversion level constant as shown in the following paragraph.

### C. Constant-inversion level scaling

To maintain the gain, it follows from (4b) that the channel length must be kept constant. The current must be multiplied by $K^2$ and W by K as can be easily deduced from (4a) and (1b-c). Consequently, power consumption and active area augment by K. Since weak and moderate inversion designs are power efficient [6, 9], this is not a severe drawback.

Table II Effects of scaling on analog circuits (K>1)

| Quantity | Full scaling | Constant area scaling | Constant inversion level scaling |
|---|---|---|---|
| L | $K^{-1}$ | $K^{-1}$ | 1 |
| W | $K^{-1}$ | K | K |
| $I_D$ (SI) | $K^3$ | K | $K^2$ |
| $I_D$ (WI) | $K^2$ | $K^2$ | $K^2$ |
| $i_d$ (SI) | $K^2$ | $K^{-2}$ | 1 |
| $i_d$ (WI) | K | $K^{-1}$ | 1 |
| $f_T$ | $K^3$ | K | 1 |
| $G_V$ (SI) | $K^{-2}$ | 1 | 1 |
| $G_V$ (WI) | $K^{-1}$ | $K^{-1}$ | 1 |

## Resizing rules

The resizing rules include non-scaling factors, the effect of the circuit topology on the signal swing and low frequency noise. To keep the transistors operating in saturation, the signal swing must be limited. The maximum voltage swing is obtained subtracting from $V_{DD}$ as many $V_{dssat}$ and $V_t$ voltage drops as required by the topology of the circuit [13].

Table III. Resizing rules for MOS transistors considering a generalized scaling

$V_{pp}\rightarrow K_V^{-1}V_{pp}$, $C'_{ox}\rightarrow K_{ox}C'_{ox}$, $L\rightarrow K_L^{-1}L$, , $V_E\rightarrow K_EV_E$

| Quantity | Constant area (SI) | Constant inversion level (WI) |
|---|---|---|
| $V_{PP}$ | $K_V^{-1}$ | $K_V^{-1}$ |
| $V_E$ | $K_E$ | $K_E$ |
| L | $K_L^{-1}$ | $K_E^{-1}$ |
| W | $K_L$ | $K_V^2K_E^{-1}K_{ox}^{-1}$ |
| $I_D$ | $K_V^2K_EK_L^{-1}$ | $K_V^2$ |
| $f_T$ | $K_V^2K_L^{-1}$ | $K_E^2$ |

Consequently, the signal swing scales in practice by a factor $K_V>K$ when the supply voltage scales by K. To preserve the dynamic range, the capacitances must by scaled by $K_V^2$ and, to maintain the bandwidth, the transconductances must also be scaled by $K_V^2$. To keep the gain constant, the scaling of the Early voltages can also be included in the resizing factors as shown in table III.

Full scaling will not be considered here because it degrades the analog performance. The choice between constant area and constant inversion level scaling depends on the operating point of the transistor. Transistors

operating in the weak inversion or lower moderate inversion region must be scaled at constant inversion level, while transistors operating in strong inversion are more conveniently scaled at constant area and power consumption.

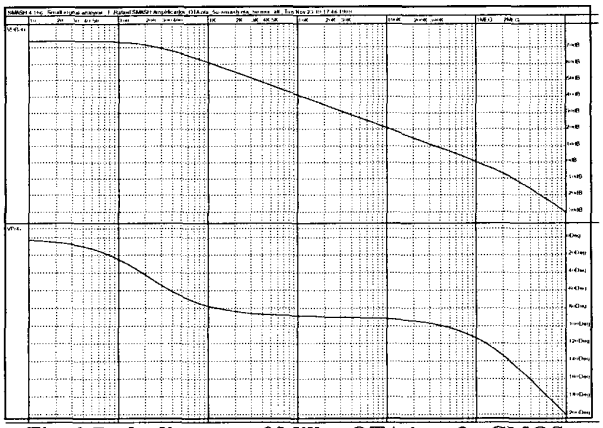

**Fig. 2 Bode diagram of Miller OTA in a 3μ CMOS technology**

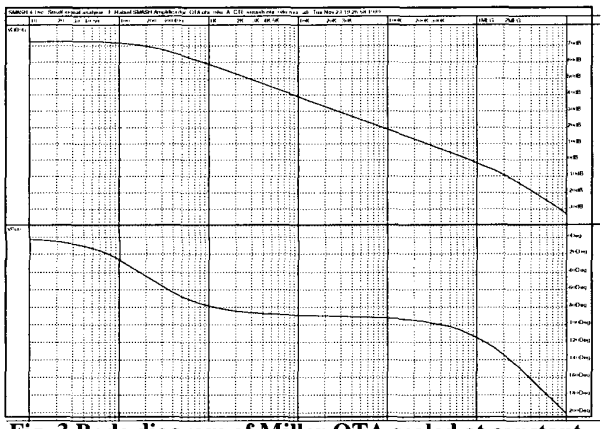

**Fig. 3 Bode diagram of Miller OTA scaled at constant area in a .8μ CMOS technology**

## Example

The Miller OTA described on page 490 of ref.[5] has been designed for a 3μm technology and 5V power supply. We present here the resizing of this OTA for a .8μm technology and 2V power supply. Because the transistors operate in the higher end of moderate inversion, both constant area scaling and constant inversion levels can be applied.

The scaling factors are: $K_V$=2.7; $K_L$=3.75; $K_{ox}$=2.7 and $K_E$=1. The comparison of Fig. (2) and Fig. (3), shows that the open gain characteristics are almost the same for both amplifiers.

**Table IV. Simulated performance for the Miller CMOS OTA**

| | Original design | Constant area scaling | Constant inversion level scaling |
|---|---|---|---|
| Supply voltages | 5V | 2V | 2V |
| Open-loop gain | 74dB | 73dB | 63dB |
| Unity gain frequency | 1MHz | 830kH | 745kH |
| Phase margin | 66° | 69° | 68° |
| Total current | 30μA | 39μA | 190μA |

**Table V. Dimensions of the transistors of the Miller OTA of Fig. 6.4 of ref. [5]**

| | Original design | Constant area scaling | Constant inversion level scaling |
|---|---|---|---|
| T1 | 26/16 | 98/4 | 70/16 |
| T2 | 26/16 | 98/4 | 70/16 |
| T3 | 10/10 | 38/2.4 | 26/10.4 |
| T4 | 10/10 | 38/2.4 | 26/10.4 |
| T5 | 55/5 | 206/1.6 | 147/4.8 |
| T6 | 115/5 | 431/1.6 | 308/4.8 |
| T7 | 13/10 | 49/2.4 | 35/10.4 |
| T8 | 13/10 | 49/2.4 | 35/10.4 |

Mismatch and low frequency 1/f noise are inversely proportional to the area of the devices [7, 14]. Because in the proposed resizing rules area is preserved or augmented, matching and 1/f noise are maintained in first approximation. If the parameters characterizing low frequency noise and/or matching are different in the new technology, it is always possible to increase the area to satisfy the specs related to random fluctuations [15]. In the W-scaling proposed in [15], C, W and $I_D$ are scaled by the same factor, keeping constant both frequency response and gain. In fact, the W-scaling proposed in [15] is a particular case of the constant inversion level scaling proposed in this paper.

## Effects of scaling on switch and sample and hold

The conduction gap of analog switches is one of the most significant obstacles for low-voltage operated analog circuits [9]. Among the techniques to deal with this problem, constant voltage operated switches [16] is particularly suited for reuse. Using the bias circuit proposed in [16], the on-conductance of the switches is given by:

$$g_{ON} = \frac{W}{\sqrt{2}L}\mu C_{ox}(V_{DD} - V_{TO}) \quad (9)$$

To scale a sample and hold circuit while maintaining speed, the time constant $C_L/g_{on}$, where $C_L$ is the holding capacitance, must be kept constant.

The channel length is scaled (L→L/K) and the aspect ratio W/L of the switches is easily determined from (9). As demonstrated in [7], if the operating speed is maintained in the scaled circuit, the error due to charge injection is reduced by the scaling factor K.

## Conclusions

A methodology to reuse analog MOS circuits has been developed. It is supported by a current-based MOSFET model, which has accurate single-piece equations and uses normalized variables and few physical parameters. Simple formulas allow the calculation of transistor dimensions and bias for a given circuit in a current technology, starting from the circuit designed in a previous technology. The proposed methodology has been applied to the redesign of an operational amplifier and corroborated by simulations.

## Acknowledgment

The authors would like to thank the financial support of CNPq, from the Brazilian Ministry of Science and Technology.

## References

[1] Reusable Application-Specific Intellectual Property Developers, [Online] Available WWW: http://www.rapid.org.

[2] VSI Alliance, [Online] Available WWW: http://www.vsi.org.

[3] R. A. Quinnell, "Survey: Analog and mixed-signal cores" [Online] Available WWW: http://www.s2mag.com/editorial/1999.

[4] K. Francken and G. Gielen, "Methodology for analog technology porting including performance tuning", *Proceedings of IEEE ISCAS*, vol. I, pp. 415-418, 1999.

[5] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, New York: McGraw-Hill, 1994.

[6] F. Silveira, D. Flandre and P. G. A. Jespers , " A $g_m/I_D$ methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA"; *IEEE J. Solid-State Circuits*, vol.31, no. 9, pp. 1314-1319, September 1996.

[7] E. A. Vittoz, "Future of analog in the VLSI environment", *Proceedings of IEEE ISCAS*, pp. 1372-1375, 1990.

[8] A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "An MOS transistor model for analog circuit design", *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510-1519, October 1998.

[9] E. A. Vittoz, "Micropower techniques" in *Design of MOS VLSI Circuits for Telecommunications*, J. Franca and Y. Tsividis (eds.), Upper Saddle River: Prentice-Hall, 1993.

[10] E. Sánchez-Sinencio and A. G. Andreou (eds.), *Low-Voltage/ Low Power Integrated Circuits and Systems*, New York: IEEE Press, 1999.

[11] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, second edition, New York: McGraw-Hill, 1999

[12] H-T Ng, R. M. Ziazadeh and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation", *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 339-347, March 1999.

[13] K. Bult, "Analog broadband communication circuits in pure digital deep sub-micron CMOS", *1999 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 76-77, 1999.

[14] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors", *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1440, October 1989.

[15] B. Nauta, "Analog CMOS low-power design considerations", *Digests Low power-low voltage workshop at ESSCIRC' 96*, Switzerland, 1996.

[16] R. T. Gonçalves, S. Noceti Filho, M. C. Schneider and C. Galup-Montoro, "Digitally programmable switched current filters", *Proceedings of IEEE ISCAS*, vol. 1, pp. 258-261, 1996.