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SIZING OF MOS TRANSISTORS FOR AMPLIFIER DESIGN

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ABSTRACT

This paper presents a design procedure for amplifiers based on a universal model of the MOSFET, valid from weak to strong inversion. A set of very simple expressions allows quick design by hand as well as an evaluation of the design in terms of power consumption and silicon real estate. It is shown that there is an optimum bias in moderate inversion for which the attainable DC gain is maximum. The design and measurements of a common-source amplifier illustrate the appropriateness of the proposed methodology.

1. INTRODUCTION

In high frequency analog circuits, MOS transistors are often biased in strong inversion [1]. On the other hand, the current efficiency, given by the transconductance-to- drain current ratio (g_m/I_D), is maximum when MOS transistors operate in weak inversion [2]. Usually, the design trade-off for MOS amplifiers is formulated in terms of the gate voltage overdrive V_{GS}-V_{TH}. Common values of V_{GS}-V_{TH} for analog design lie on the range from 100 to 500mV [3][4]. A major difficulty to set precisely the gate voltage overdrive is due to the uncertainty in V_{TH}, whose batch-to-batch 3σ spread can be as high as 150mV [9]. An alternative approach to bias analog circuits is the current-based design that avoids the difficulties in setting a precise bias voltage for the gate. Using this methodology it is shown that the best compromise between consumption and speed is achieved in moderate inversion [5][6]. As a consequence, conventional MOSFET models developed for either weak inversion or strong inversion are not well suited for optimizing analog design.

In analog circuits, the choice of the channel length of the MOS transistor results from a balance between voltage gain and frequency response. While the transition frequency is maximum for minimum channel length, the attainable voltage gain is roughly proportional to the channel length [2].

In this paper we present a design methodology for MOS amplifiers using the universal MOSFET model developed in [7], which employs the bias current as the key variable. The design procedure proposed in this paper accounts for the specifications of capacitive load (C_L), gain-bandwidth product (GB), DC voltage gain (A_{VO}) and voltage swing. It allows the designer to choose the bias current and transistor dimensions from closed expressions. The design approach proposed here, which has been applied to the design of common-source amplifiers, can be extended to more complex topologies such as differential and operational amplifiers.

2. MOSFET MODEL

The following set of equations developed in [7] can be readily used for the design of MOSFETs operating in saturation:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_d}} \qquad (1.a)$$

$$i_d = \frac{I_D}{I_S} \qquad (1.b)$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \qquad (1.c)$$

The transconductance-to-current ratio of MOSFETs given by (1.a) is a universal relationship for MOSFETs, being independent of technology, dimensions and temperature. I_S, the normalization current, depends on the aspect ratio (W/L) and technological parameters: mobility μ and oxide capacitance per unit area C'_{ox}. ϕ_t is the thermal voltage and n is the slope factor, which is slightly greater than one and almost bias-independent [7]. i_d is the normalized drain current [7]. Recalling that $\phi_t g_m/I_C=1$ for bipolar transistors, the collector current I_C is solely defined for a given g_m. However, in a MOSFET design, the specification of g_m allows the designer to choose from a range of currents, according to (1).

The intrinsic cutoff frequency of a MOSFET in saturation

$$f_T = g_m/2\pi(C_{gs}+C_{gb}) \qquad (2a)$$

is approximated in [7] by

$$f_T \cong \frac{g_m}{2\pi\left(\frac{1}{2}C'_{ox}WL\right)} = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_d}-1\right) \qquad (2b)$$

and will be used throughout this paper. This very simple results states that for a constant g_m, f_T and area are inversely proportional to each other. An important figure of merit of transistors is the ratio of the transconductance to the gate area (g_m/WL), which can be denominated area efficiency. This definition is complementary to the definition of current efficiency (g_m/I_D). In our approximate model, the transition frequency and the area efficiency have the same meaning, as readily seen in (2b).

Finally, an approximate formula for the source-to-drain saturation voltage as function of the inversion level is given by

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$$\frac{V_{DSsat}}{\phi_t} \cong \left(\sqrt{1+i_d}-1\right)+4 \qquad (3)$$

The very simple set of equations (1-3) model relevant aspects of amplifier design.

Even though the ratio g_m/I_D given by (1.a) has been demonstrated to be valid for long-channel devices where the transversal field dependence of mobility has been neglected, it still holds if degradation of mobility due to vertical field is taken into account. Also, velocity saturation is not relevant in most of the cases because operation of the MOSFET deep in strong inversion is very improbable, particularly at low supply voltage.

In order to avoid the non-quasi-static effects to have an appreciable influence on the frequency response of the amplifier, the value of gain-bandwidth product should be a fraction of the transition frequency. Thus, from now on, we will assume that the transition frequency is at least equal to four times the value of gain-bandwidth product (GB).

3. THE BASIC MOSFET AMPLIFIER

The maximum voltage gain achievable with a single transistor is limited by the source-to-drain conductance, which is approximately proportional to the ratio of the drain current to the channel length [2]. Thus, A_{vo}, the absolute value of the attainable voltage gain of the common source amplifier shown in Fig. 1 can be written as

$$A_{vo} = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D} V_A L \qquad (4)$$

where V_A is the Early voltage per unit length [3]. In this work we suppose that V_A is constant even though it tends to increase somewhat in strong inversion ([2], Chap. 2 in [8]) and is also slightly dependent of L.

In the ideal common-source amplifier shown in Fig. 1, the transconductance required for the specified GB and load capacitance is

$$g_m = 2\pi GBC_L \qquad (5)$$

In the derivation that follow we are going to assume that the transconductance is fixed and given by (5). The effect of the drain parasitic capacitance on the design is considered in the Appendix.

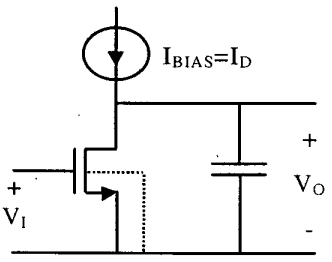

Figure 1. Common-source amplifier.

4. DESIGN SPACE FOR THE MOS APLIFIER

The methodologies presented in [5, 6] to design amplifiers are based on either measured or calculated curves of g_m/I_D in MOSFETs. These methodologies do not provide design equations that take into account the channel length. In the present work, starting from the voltage gain as an initial specification, we provide design equations that include the channel length. Only three technology-dependent parameters are used in our methodology: the sheet normalization current $I_{S\square}$ (I_S for W=L), the Early voltage per unit length V_A, and the oxide capacitance per unit area C'_{ox}.

The channel length required to achieve the voltage gain A_{VO} is readily calculated from (1) and (4):

$$L = \frac{n\phi_t A_{V0}}{V_A} \frac{1+\sqrt{1+i_d}}{2} \qquad (6)$$

The straight lines in Fig. 2, which are a plot of (6), show the linear dependence of the channel length on the voltage gain, for constant normalized current.

Combining (2b) and (6) one obtains

$$(A_{V0})^2 f_T = \frac{\mu\phi_t}{2\pi}\left(\frac{V_A}{n\phi_t}\right)^2 \cdot \frac{8\left(\sqrt{1+i_d}-1\right)}{\left(\sqrt{1+i_d}+1\right)^2} \qquad (7)$$

Expression (7) shows that for all transistors of a given technology, the product of the transition frequency f_T and the squared attainable voltage gain $(A_{V0})^2$ is independent of geometry, depends only on the inversion level i_d, and is maximum for i_d=8. In other words, for all transistors with the same f_T, the choice of i_d=8 allows for the maximum voltage gain.

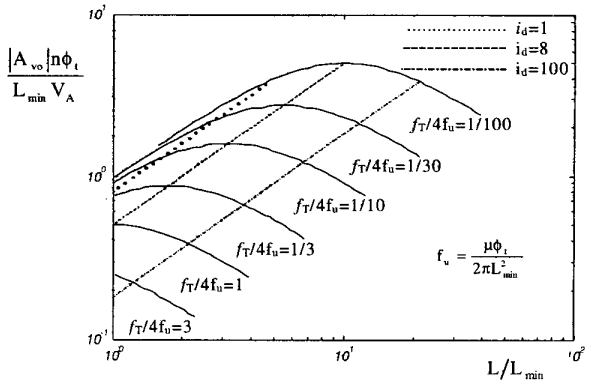

Figure 2. The relationship between attainable DC gain and channel length, with the inversion level or transition frequency as parameters.

Let us now use Fig. 2 to discuss how to design a single-stage amplifier. Assume the specifications for the dc gain and gain-bandwidth product to be A_{VO} and GB. As mentioned before, the MOSFET transition frequency has to be, at least, four times larger than GB. Therefore, a single-stage amplifier that meets the specs is realizable if the curve f_T=4GB intersects the horizontal line corresponding to the desired dc gain, A_{VO}, for $L>L_{min}$. Obviously, if we choose simultaneously high gain (horizontal lines in the uppermost part of the plane) and high GB (constant f_T curves in the bottom part of the plane) the single-stage solution may not exist. To explore the design space it is interesting to observe that the constant f_T curves are also the locus of constant area (WL) transistors that meet the specification of g_m, which is determined from the product C_LGB (5). On the other hand, the constant i_d curves are the loci of constant current I_D transistors conforming to the specification of g_m.

If the specs can be met, the maximum gain is obtained either for f_T=4GB and i_d=8 as long as $L>L_{min}$ or f_T=4GB and $L= L_{min}$ when the channel length corresponding to i_d=8 is below the minimum channel length. The minimum current is obtained also on the f_T=4GB curve, at the minimum channel length necessary to obtain the specified gain. The minimum area is obtained by choosing the curve of maximum f_T that satisfies the specs. For low frequency designs, the transistor with smallest area that meets the specs corresponds to the maximum (i_d=8) on the f_T curve whose maximum is the desired dc gain, A_{VO}. In any cases, the sizing of the transistor complies with the inequalities of Table I.

Table I.. Limits of the design space of single stage MOS amplifier for f_T>4GB

$I_D>n\phi_T(2\pi GBC_L)$	From (1.a)
$WL<C_L/(2.C'_{ox})$	From (2b) and (5)
$i_d>[(4GB/(2\mu\phi_T/2\pi L^2)+1]^2-1$	From (2b)

As an example, consider the design of single-stage amplifiers for C_L=1pF. Assume L_{min}=1μm, C'_{ox}=2fF/μm^2, μ_n=500cm^2/V.s, V_A=5V/μm, n=1.25, ϕ_t=25mV and GB's given in Table II-IV, which show the results obtained using expressions (1-7).

Table II describes a low frequency design. The transistors lengths are all greater than the minimum length. The area of the low f_T (500kHz) transistors is 25 times greater than the area of the high f_T (12.5MHz) transistor. The low current design (deep in weak inversion) has half the current of the moderate inversion solution but a much larger area. In practice, a value of i_d close to 1 can be a good choice if low power is required. Tables III and IV show specs and designs for medium and high frequency, respectively. It is clear that, for high frequency, the options open to design are not as many as in low frequency. For high frequency design, the maximum value of i_d is limited by the required signal swing and the available supply voltage.

Table II. Basic parameters of single stage amplifiers. GB=100kHz, C_L=1pF, Avo>300V/V

	f_T (MHz)	W/L (μm/μm)	I_D(nA)	A_{vo}	i_d	V_{DSsat} (mv)
High Gain	0.5	5/40	40	3200	8	150
Small Area	12.5	1/8	40	640	8	150
Low Current	0.5	100/2	20	320	0.01	100

Table III. Basic parameters of single stage amplifiers. GB=10MHz, C_L=1pF, A_{vo}>100V/V

	f_T (MHz)	W/L (μm/μm)	I_D(μA)	A_{vo}	i_d	V_{DSsat} (mv)
High Gain	50	50/4	4	320	8	150
Small Area/ Low Current	450	22/1	3	102	3.5	130

Table IV. Basic parameters of single stage amplifiers. GB=1GHz, C_L=1pF, A_{vo}>10V/V

	f_T (GHz)	W/L (μm/μm)	I_D(mA)	A_{vo}	i_d	V_{DSsat} (mv)
High Gain	4	250/1	1.2	27	120	350
Small Area/ High Current	12	83/1	3.1	10	960	850

5. EXPERIMENTAL RESULTS

Fig. 3 shows the normalized theoretical and measurement-based gain. The measurement-based points have been determined for i_d=1.6, 3.2, 4.8, 6.4, 16, 32, 48, 64, 160, 320, 480 and 640, and have been interpolated from experimental results. The maximum of the experimental curves is for i_d around 80. The difference between the value i_d=80 and the theoretical value of i_d for which maxima occur (i_d=8) is justified by noting that the Early voltage V_A is a slightly increasing function of the normalized current. Therefore, the experimental value of id for which the maximum occurs is higher than the theoretical value.

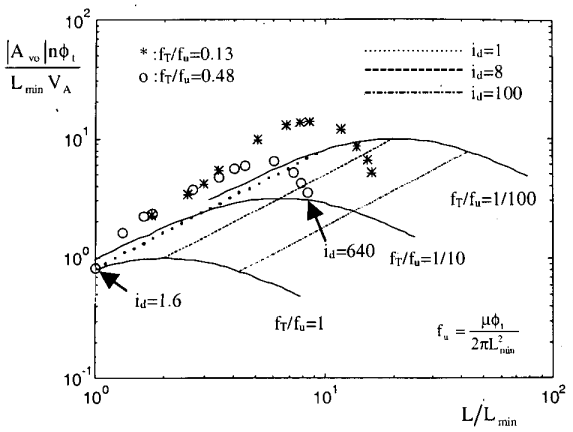

Figure 3. Theoretical (-) and measurement-based points (° and *). L_{min}=1.2μm.

6. CONCLUSIONS

A methodology to design MOS amplifiers has been developed. It is supported by a current-based MOSFET model which has accurate and continuous equations from weak inversion to strong inversion. The design approach is suitable for both low power design or for area optimization. We proposed a very simple design methodology which allows for maximum gain either with the transistor operating in moderate inversion or using minimum channel length for high frequency amplifiers. The proposed methodology has been applied to the design of a common-source amplifier and corroborated with experimental results.

Appendix
The effect of parasitic capacitance

If the parasitic drain capacitance per unit width C'_J is taken into account in the amplifier of Fig. 1, then (5) must be rewritten as

$$g_m = 2\pi GB(C_L + W\ C'_J) \qquad (A1)$$

From (2) and (A1)

$$W = \left(\frac{2C_L}{L C'_{ox}}\frac{GB}{f_T}\right) \Big/ \left(1 - \frac{2C'_J}{L C'_{ox}}\frac{GB}{f_T}\right) \qquad (A2)$$

(A2) shows that typically, for L equal to the minimum channel length, f_T should be at least four times higher than GB to avoid the parasitic diffusion and overlap capacitances of the MOSFET to be of the same order of C_L. In effect, considering f_T=4GB, L=1μm, C'ox=2fF/μm^2 and C'_J=1fF/μm, (A2) gives for the channel width W a value 30% greater than the basic relation (5). A high parasitic capacitance would contribute to increase the transistor width by a large amount. It is important to remark that a minimum value of the ratio of the transition frequency to the gain bandwidth product (e.g. 4) has two objectives. The first one is to prevent the non-quasi-static effects (related to L) to affect the frequency response of the amplifier up to GB. The second one is to avoid the parasitic capacitances (proportional to W) to be comparable to the load capacitance.

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