A HIGH-SWING MOS CASCODE BIAS CIRCUIT FOR OPERATION AT ANY CURRENT LEVEL

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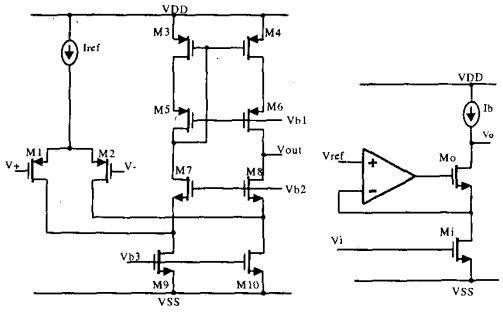
ABSTRACT

In this paper, we propose a very simple bias circuit that allows for maximum output voltage swing of MOSFET cascode stages. The proposal is valid for any current density and is technology-independent. Starting from the saturation voltage and from the current density of the cascode stage we determine the aspect ratio of the transistors in the bias circuit in order to maximize the output voltage swing. Experimental results validate the strategy for designing the bias network.

1. INTRODUCTION

Cascode current mirrors (CCM) have a much higher output resistance than simple current mirrors yet at the expense of the output voltage swing. Self-biased CCMs [2][3] have as their main drawback a very serious loss of signal swing. Cascode stages with fixed bias [4][5][6][7], such as those shown in Fig. 1 [8][9], can be optimized for high output voltage swing. In order to maximize the output voltage swing, the values of the bias voltages V_{b1}, V_{b2} and V_{ref} should be such that M4, M10 and M_i, respectively, operate at the edge of saturation.

The very simple circuits in [7] were proposed to bias cascode mirrors either for strong inversion or for weak inversion. The cascode biasing circuit proposed in [4] can operate at any current level with a minimal output saturation voltage but spends a lot of silicon area and is not suitable for high frequency applications.



(a) (b)

Figure 1. (a) Folded cascode input stage [9], (b) Cascoded gain stage with gain enhancement [8].

In this paper we extend for moderate and strong inversion one of the biasing circuits presented in [7], which was proposed for operation in weak inversion. The bias circuit proposed here is useful for both amplifier configurations shown in Fig. 1. In the first part of the paper we revisit the MOSFET model from [1][10] and introduce a definition of the saturation voltage based on practical aspects of circuit design. Additionally, the small-signal output resistance is discussed and associated with the saturation voltage of the driver transistor in the CCM. The analysis of the biasing topology is discussed next. Design equations as well as experimental results are eventually presented.

2. THE SATURATION VOLTAGE

According to the MOSFET model in [1][10], the drain current can be decomposed into the forward (I_F) and reverse (I_R) currents:

$$I_D = I_F - I_R \tag{1}$$

where $I_F(I_R)$ is dependent of the gate and source (drain) voltages. In forward saturation $I_F \gg I_R$ and $I_D \cong I_F$.

The MOSFET output characteristic [1][10] is modeled in normalized form as:

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{2}$$

where

$$i_{f(r)} = \frac{I_{F(R)}}{I_S}, \quad I_S = I_{SQ}\left(\frac{W}{L}\right), \quad I_{SQ} = \mu.n.C'_{ox}.\frac{\phi_t^2}{2} \tag{3}$$

I_S is the normalization current, I_{SQ} is the sheet normalization current, $i_{f(r)}$ is the normalized forward (reverse) current, ϕ_t is the thermal voltage and "n" is the slope factor. More details about equations (1) through (3) can be found in [1][10].

In order to introduce a definition of the saturation voltage that is useful for circuit designers, we first define the maximum allowable voltage gain of the common gate amplifier $A=g_{ms}/g_{md}$, where g_{ms} is the source transconductance while g_{md} is the MOSFET output conductance. Indeed, "A" is equal to the ratio of the slope of the

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transistor output characteristic at the origin (V_D=V_S) to the slope of the characteristic at the quiescent operating point, as shown in Fig. 2.

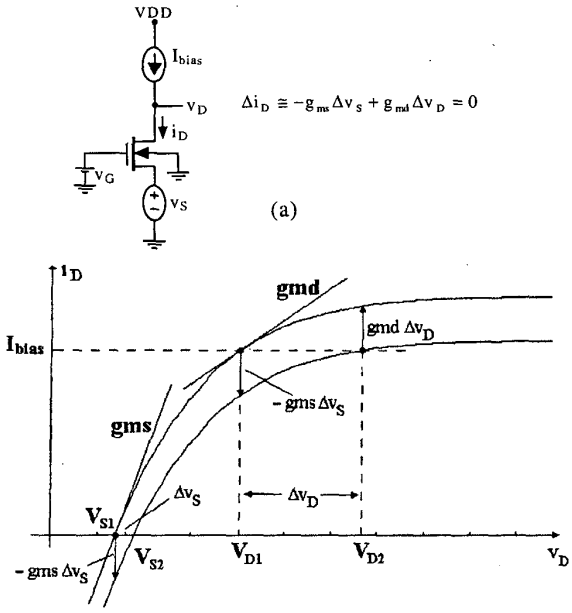

Figure 2. (a) Common-gate amplifier, (b) Definition of the MOSFET source transconductance (gms) and output conductance (gmd).

Clearly, the so-called saturation voltage should be associated with a large value of "A". Considering that

$$g_{ms(d)}\phi_t = 2I_S\left(\sqrt{1+i_{f(r)}}-1\right) \qquad (4.a)$$

as given in [10], one can easily derive from (2) the value of the saturation voltage V_{DSSAT} [1] as:

$$\frac{V_{DSSAT}}{\phi_t} = \ln(A)+\left(1-\frac{1}{A}\right)\left(\sqrt{1+i_f}-1\right) \qquad (4.b)$$

For large values of "A", $i_f >> i_r$ and, consequently, the normalized drain current $i_d = i_f - i_r \cong i_f$. Therefore, one can substitute i_d for i_f in (4.b).

The definition of the saturation voltage as shown in (4.b) is very appropriate for building blocks such as current mirrors where voltage swing and voltage gain are essential specifications. Fig. 3 illustrates the dependence of the saturation voltage on the inversion level. For strong-inversion $V_{DSSAT} \cong \phi_t\sqrt{i_f}$, while for weak-inversion $V_{DSSAT} \cong \phi_t.\ln(A)$.

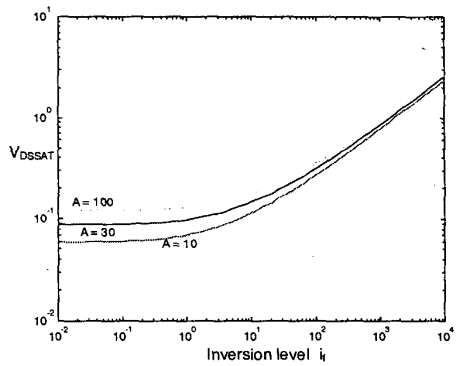

Figure 3. Saturation voltage as a function of the inversion level, gain A as parameter and ϕ_t=26mV.

3. THE OUTPUT RESISTANCE

Cascode stages are capable of exhibiting very high output resistance and a gain-bandwidth product almost equal to that of a single stage [8]. With the aid of Fig. 4(a), one can readily determine the output impedance at the drain of M4:

$$\frac{v_{out}}{i_{out}} \cong \frac{g_{ms4}/g_{md4}}{g_{md2}} \qquad (5.a)$$

The result in (5.a) can be readily interpreted by noting that the drain voltage of M2 is equal to the output voltage divided by the voltage gain of the common-gate configuration. Assuming both M2 and M4 to be operating in saturation and to have the same aspect ratios, then $g_{ms4} \cong g_{ms2}$ (see equation (4.a)). Therefore, (5.a) can be written as:

$$\frac{v_{out}}{i_{out}} \cong \frac{g_{ms2}/g_{md2}}{g_{md4}} = \frac{A}{g_{md4}} \qquad (5.b)$$

where "A", the voltage gain of M2 depends on the drain-source voltage, and thus on the bias voltage V_B. Therefore, V_B should be sufficiently high to allow for a high "A" but not too much high to avoid a reduction in the output voltage swing. The following section shows how to design the circuit in Fig. 4(b) to bias M2 at the edge of saturation.

4. BIAS NETWORK

In the topology of the CCM shown in Fig. 4(a) all transistors share a common substrate. The value of V_B must ensure the operation of M2 in saturation for the highest value of I_{in}. If V_B is adequately chosen, the output voltage of this circuit can be as low as $2V_{DSSAT}$. Biasing the transistors deep in weak inversion allows for low voltage operation and low power consumption but the frequency response is very poor. A balance between frequency response and voltage swing is achieved in moderate inversion.

The structure proposed to generate an appropriate bias voltage for current mirrors shown in Fig. 4(b) [7] is quite simple but was introduced for operation in weak inversion.

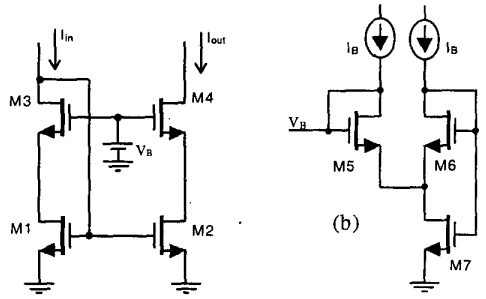

Figure 4. (a) Low-voltage CCM, (b) Biasing circuit [7]

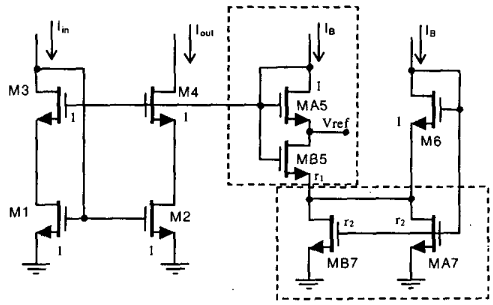

Figure 5. High-swing cascode current mirror CCM.

Our purpose in this work is to extend the application of the circuit in Fig. 4(b) to any current level. To have a better grasp of the bias network of Fig. 4(b), we have split transistors M5 and M7 into a series association of transistors (MA5 and MB5) and a parallel association of identical transistors (MA7 and MB7), respectively, as shown in Fig. 5. The series association of MA5 and MB5 provides the network of Fig. 1(b) with the appropriate voltage (V_{ref}) for maximum output swing. The aspect ratios of the transistors in the current mirror are assumed to be equal and are taken as the reference value. We have chosen the aspect ratios of MA5 and M6 to be equal to the reference value and the bias currents through both MA5 and M6 to be equal to the input current. Therefore, the gate-source voltage of MA5 is equal to the gate-source voltage of M4. Consequently, the sum of the drain-source voltages across MB5 and MB7 equals the drain-source voltage across M2. From now on, to simplify matters, we will assume that the sheet normalization current I_{SQ} is equal for all transistors, even though it is slightly dependent of the gate voltage [1]. Consequently, we consider the normalized forward currents of M4, MA5 and M6 to be identical because the three transistors have the same geometry and they are biased at the same current and operate in saturation. Making the aspect ratios $r_1=r_2=r$ and defining $\alpha=(r+1)/r$, one can readily conclude that $i_{rMB5}=i_{rMB7}=i_f$, and $i_{fMB5}=i_{fMB7}=\alpha.i_f$ Here, i_f refers to the inversion level of the CCM transistors, which is almost equal for both M2 and M4 as long as M2 and M4 operate in saturation. From the previous considerations we can derive the following equation from (2):

$$\frac{V_{DSMB5}+V_{DSMB7}}{2.\phi_t}=\sqrt{1+\alpha.i_f}-\sqrt{1+i_f}+\ln\left(\frac{\sqrt{1+\alpha.i_f}-1}{\sqrt{1+i_f}-1}\right) \quad (6)$$

Deep in weak inversion ($i_f<<1$) the right hand side of (6) can be written as $\ln(\alpha)$ whereas deep in strong inversion ($i_f>>1$) it can be approximated by $\left(\sqrt{\alpha}-1\right)\sqrt{i_f}$.

In order to bias M2 at the edge of saturation, the sum of the drain-source voltages of MB5 and MB7 should be equal to the saturation voltage (V_{DSSAT}) of M2. Equating (4.b) to (6) allows one to determine the curves shown in Fig. 6 for different gains. Note from (6) that the choice of "α", which defines the aspect ratio "r", depends on the inversion level but is independent of the technological parameters. Note also that "r" ranges from 0.1 to 0.8 approximately. In strong inversion, the optimum value of r is 0.8 $\left(\sqrt{\alpha}=1.5\right)$. On the other hand, in weak inversion "r" varies from 0.1 to 0.5, depending on the value chosen for the voltage gain.

Even though the present analysis has been performed for long-channel devices, we can apply it to short-channel devices as long as A is not higher than the maximum achievable gain of the short-channel device. Our analysis has not taken into account transistor or current mismatching. In a practical circuit, the aspect ratio r could be slightly decreased in order to add a small safety margin to the drain-source voltage of M2 that would compensate for transistor mismatching. The price to be paid would be a slightly smaller output voltage swing of the CCM.

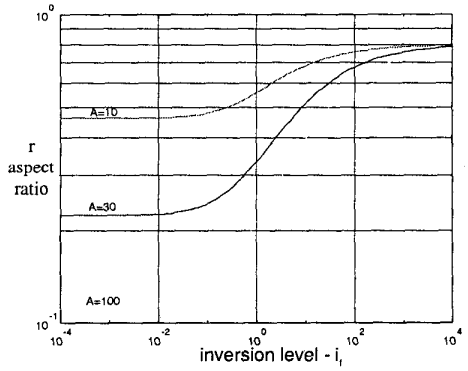

Figure 6. Relationship between normalized aspect ratio and inversion level.

5. EXPERIMENTAL RESULTS

To validate the design methodology, simple, self-biasing cascode (self-CCM) and low-voltage cascode (LV-CCM) current mirrors have been implemented and tested. N-channel transistors ($V_T \approx$ 0.6V) from a 2μm CMOS technology have been used in the current mirrors. All transistors in the simple mirrors and CCM's have the same aspect ratios.

Figs. 7 through 9 present details of the output characteristics of the current mirrors. Values of r=1/3, 1/2 and 2/3, respectively, have been chosen according to Fig. 6, for i_f=1, 10 and 100 and A=30.

Note that the LV-CCM's reach saturation at a drain-source voltage roughly twice the saturation voltage of the simple current mirror. The self-biased CCM saturates at a much larger voltage than the "optimally" biased CCM.

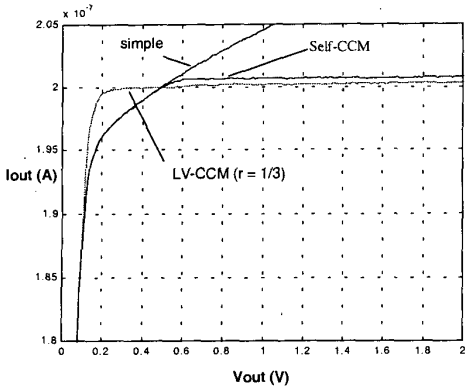

Figure 7. Detail of experimental output characteristics of the current mirrors in weak inversion (i_f=1).

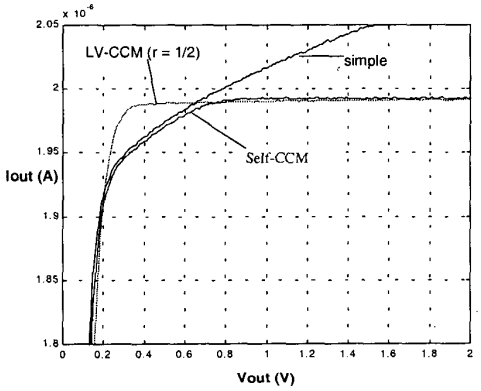

Figure 8. Detail of experimental output characteristics of the current mirrors in moderate inversion (i_f=10).

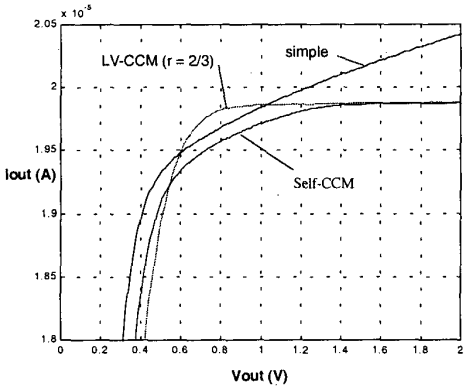

Figure 9. Detail of experimental output characteristics of the current mirrors in strong inversion (i_f=100).

6. CONCLUSIONS

A very simple bias circuit, valid for any current density, which allows for maximum output voltage swing of cascode stages has been presented and analyzed. Starting from the multiplication factor of the output impedance required for the cascode stage relative to the single stage and from the output swing it is possible to determine the "optimally" biased network. Experimental results corroborated the design methodology of the bias network. The biasing circuit is very useful for low-voltage design

Acknowledgment

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