A FULLY BALANCED PROGRAMMABLE SAMPLE-HOLD AMPLIFIER FOR LOW-VOLTAGE APPLICATIONS

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ABSTRACT

In this paper, we propose a CMOS fully balanced sample-hold amplifier. The proposed circuit is based on the technique described in [1], which is appropriate for low voltage operation. The programmability of the sample-hold circuit is achieved via the MOSFET Only Current Divider (MOCD) [2]. We present a new method for sign-bit realization using the two output currents of the MOCD. The programmable S/H circuit is designed to be fabricated in a 0.8μm CMOS technology with ±0.75V power supply.

1. INTRODUCTION

The switched-current (SI) technique has been considered as a practical way for the implementation of analog sampled-data systems in digital CMOS technology [3]. Unfortunately, the conventional SI technique presents the same limitation of switched-capacitor (SC) circuits with respect to the conduction gap of the switches when operated at low supply voltages [4]. To overcome the conduction gap of the switches, the technique proposed in [1], which is going to be denominated switched-MOST, has been developed. In this circuit technique, the switches operate at constant channel voltage (equal to V_{BIAS}). The realization of sample-hold circuits for both the conventional SI and the switched-MOST [1] techniques are shown in Fig. 1. The bias voltage for the switched-MOST, generated at the intermediate node of the series association of two identical NMOS transistors shown in Fig. 1.c [1] has two important properties: (1) it allows for equal positive and negative current swing; (2) it lies within the conduction range of NMOS switches. Thus, the constant voltage switching of the sample-hold is well suited to low voltage applications, since it avoids the conduction gap of the switches as well as the signal dependent charge injection. Based on the circuit shown in Fig. 1.b, we propose a fully balanced programmable sample-hold.

Fully Balanced Circuit Architectures (FBCAs) are widely used in analog-signal-processing applications because FBCAs ensure high power supply rejection, improve linearity and increase the dynamic range. Also, in sampled-data circuits (switched-capacitor, switched-current or switched MOST) FBCAs reduce the effects of clock feedthrough and charge injection. The S/H proposed in this work employs an FBCA to achieve high accuracy in low voltage application.

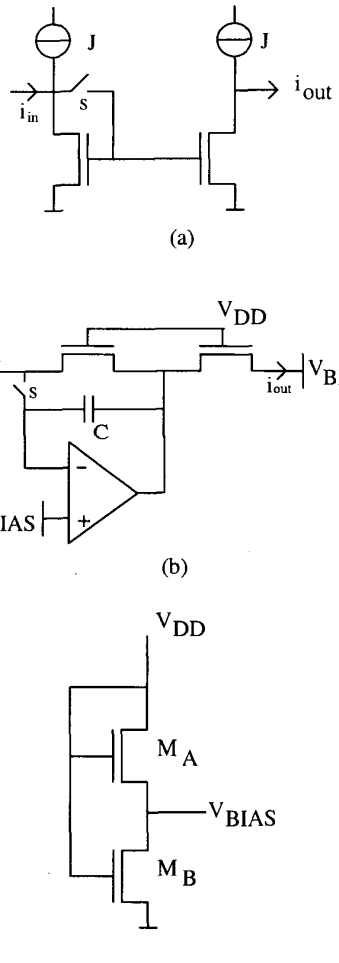

Figure 1. (a) Switched-current, (b) Switched-MOST [1], (c) Circuit for generation of V_{BIAS} [1]

The S/H circuit is described in Section 2. The binary- weighted MOCD that allows the gain of the S/H amplifier to be digitally programmed is illustrated in Section 3 along with a strategy to

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implement the sign-bit coefficient. Section 4 presents simulation results of the proposed S/H circuit and Section 5 provides some conclusions on this work.

2. FULLY BALANCED SAMPLE-HOLD CIRCUIT

A fully balanced S/H that employs the basic circuit described in [1] has been designed. The fully balanced (FB) sample-hold is shown in Fig. 2. In this S/H, the currents (I and -I) are processed in two steps:

- Track mode : the input currents are fed to the cell when both switches are closed. The currents are memorized as voltages across the holding capacitors. As much as in the conventional SI circuits, linear capacitors are not needed to store the data.
- Hold mode: when the switches open, the voltages are held on the capacitors. These voltages cause the output currents to be equal and opposite to the input currents as long as M_1, M_{L1} and M_{L2} have the same aspect ratios.

The voltage V_{CM} is equal to the voltage V_{BIAS}, which is generated according to the scheme in Fig. 1.c. In the sampled-data structure shown in Fig. 2, all the switches operate at a constant DC voltage, equal to V_{CM}, thus causing both the charge injection and switch turn-on time [5] to be signal independent. The "conduction gap", a key limitation of the switches in conventional SI and SC techniques at low voltage supply is avoided as previously described. In our design NMOS switches have been used consistently with the NMOS transistors employed as I-V converters. The dotted section in Fig.2 is the Common Mode Feedback (CMF) block.

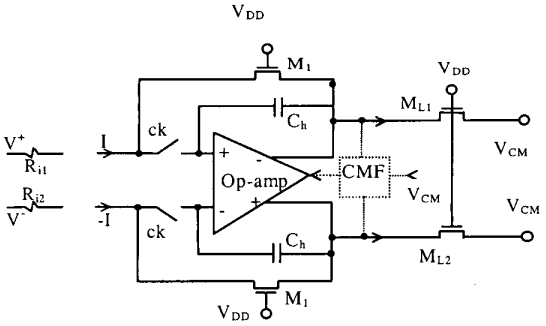

Figure 2. Proposed fully balanced sample-hold circuit.

The fully balanced (FB) differential op-amp to be used in the S/H circuit has been designed according to the methodology in [6]. The FB op-amp schematic is presented in appendix A. The proposed S/H has been designed for 500 kHz sampling rate with MOST parameters of the 0.8μm CMOS technology from AMS.

3. MOCD CIRCUIT ARCHITECTURE AND SIGN-BIT REALIZATION

3.1 The MOCD Schematic

The MOCD ladder circuit is based on the current division technique reported in [2].The schematic of the MOCD together with its symbol are shown in Fig. 3. The output currents at the SUM and DUMP lines are digitally controlled fractions of the input current.

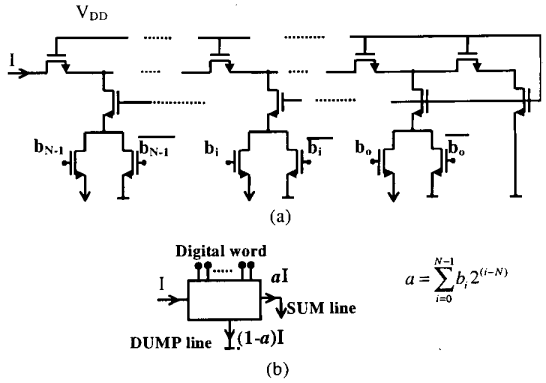

Figure 3. The MOCD circuit scheme and its symbol.

3.2 Implementation of the Negative Coefficient.

Programmable (sign and value) taps are necessary for fully programmable filters. The attenuation factor of the MOCD can be controlled digitally as shown in Fig. 3. The sign-bit control can be achieved by including an extra input transistor to the MOCD, as in [7]. This extra transistor allows for the proper selection of the input current (+I or –I) according to the sign-bit (1 or 0). The method described in [7] to invert the output currents of the MOCD's is relatively slow due to the need to invert the current of the MOCD's , thus requiring the internal nodes of the MOCD's to be charged to a complementary set of voltages.

Here, we propose a new method for the sign-bit realization, which is suitable for a fully balanced circuit. It uses the two output currents of the MOCD by adding the SUM current of one MOCD to the DUMP current of the other one, as shown in Fig. 4.a. The positive output current I_{o+} is

$$I_{o+} = (2a-1)I = \beta I \qquad (1)$$

The attenuation factor (a) of the MOCD changes from zero to one when the digital word (<bi>) is changed from 00 to FF (8 bit's MOCD). The variation of the coefficient β against the digital word is illustrated in Fig. 4.b. This method avoids the need to invert the current of the MOCD's, thus keeping the node voltages of the MOCD's at fixed values for constant input current. Therefore, the approach proposed here to realize the sign-bit is faster than the one in [7].

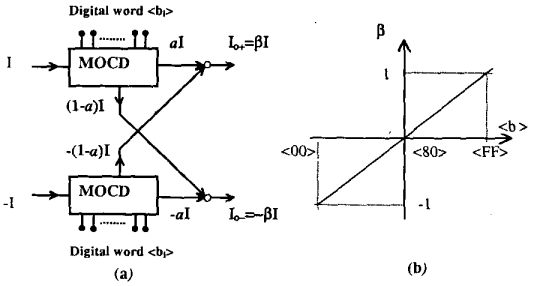

Figure 4. Proposed method for sign bit realization.

4. SIMULATION OF THE SAMPLE-HOLD

The proposed fully balanced sample-hold circuit has been designed and simulated at 500kHz sampling rate. The complete circuit has been simulated with 3μm/0.8μm NMOS switches, the aspect ratios of M_1, M_{L1}, and M_{L2} equal to 3μm/4μm and 0.5pF holding capacitors. Linear resistors have been used for the V-I conversion at the S/H input, as shown in Fig. 2. The step response, which is depicted in Fig.5, shows that the 1% settling error is less than 1μs. Fig. 6 displays the sinusoidal response of the S/H cell, which shows another advantage of switched MOST circuits over conventional SI circuits - the absence of the large glitches inherent to conventional SI circuits.

5. CONCLUSIONS

A fully programmable balanced switched-MOSFET sample-hold cell has been proposed and designed. The proposed S/H circuit achieves high accuracy due to the reduction of the effects of charge injection. The programmability of the S/H is obtained using the MOSFET current division technique. A new method for sign-bit realization has been suggested and analyzed. The S/H dissipates 10μW from a 1.5V supply. The S/H amplifiers proposed here can be used to implement programmable IIR and FIR [8] filters at low power supply.

Acknowledgment

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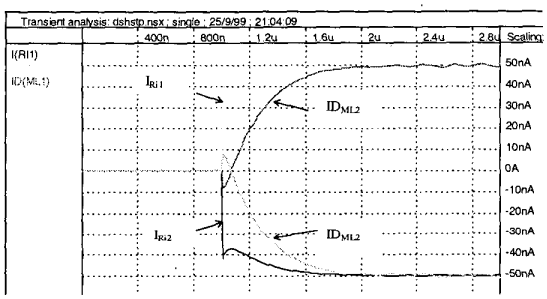

Figure 5. Step reponse of the sample-hold in Fig. 2.

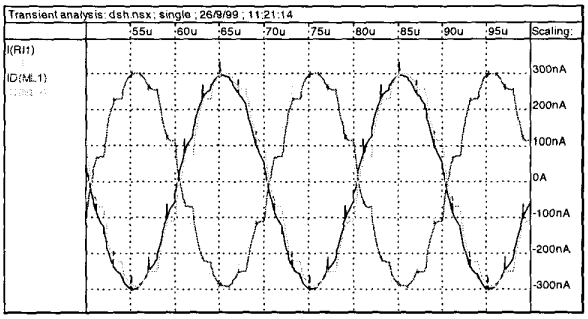

Figure 6. The sinusoidal response of the proposed S/H circuit.

7. Appendix A

The complete fully balanced op-amp schematic used in this work is depicted in Fig. A-1. Since the signals are no longer referred to ground, as in single-ended circuits, the operating point of the

amplifier cannot be stabilized. A Common Mode Feedback Loop block has to be added to overcome this problem. In our design, a MOSFET network M_{5c} and M_{6c}, instead of a resistive network, is employed to "sense" the common mode voltage. The op-amp design methodology described in [6] has been used to define transistor dimensions. Table A-1 summarizes the parameters and specs of the op-amp in Fig. A-1.

Table A-1. (L=2μm).

Op-amp parameter	
C_L (pF)	2
I_B (μA)	0.55
I_{total}(μA)	7
$W_{1,2,1c,\ 2c}$ (μm)	2.4
$W_{3,4}$(μm)	2.6
$W_{5,9}$ (μm)	10
$W_{6,10}$ (μm)	20
$W_{5c,\ 6c}$ (μm)/L(μm)	1 / 4
W_8 (μm)	2.6
$W_{7,7c}$(μm)	2.6
$W_{3c,4c}$ (μm)	2.6
A_o (dB)	60
GB (M Hz)	1.0
Phase margin	75°
C_{c1} and C_{c2}	0.5pF

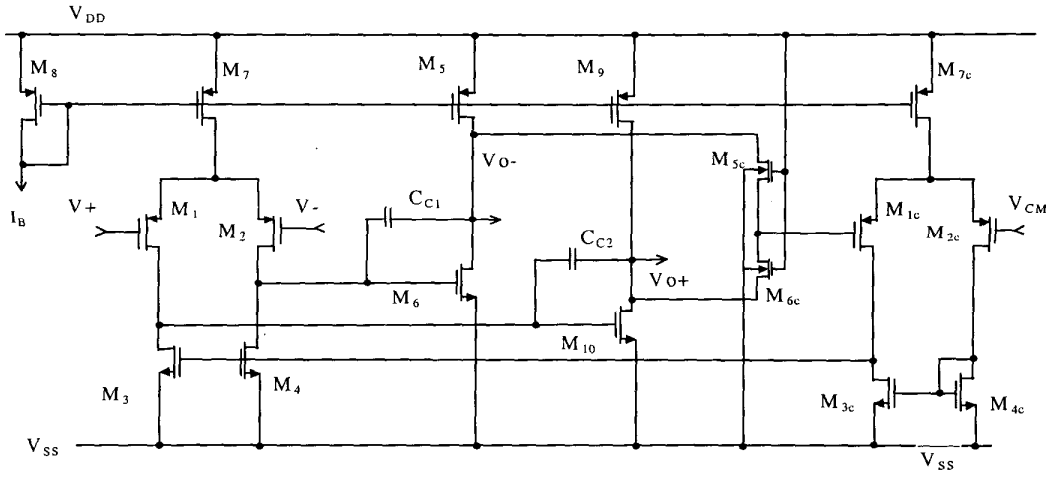

Figure A-1. Fully balanced differential op-amp schematic.