An Overview of the Current Steering Logic (CSL) : from the Gate to the Applications

R. T. L. Sáez[1], M. Kayal[1], M. Declercq[1] & M. C. Schneider[2]

[1] Swiss Federal Institute of Technology (EPFL), Electronics Laboratory
[1]LEG/ELB-Ecublens, CH-1015 Lausanne, Switzerland
[2]Universidade Federal de Santa Catarina, Departamento de Engenharia Elétrica
[2]C.P. 476, 88049-Florianópolis SC, Brasil
E_mail: maher.kayal@epfl.ch, Tel:+41-21-693 39 81, Fax: +41-21-693 36 40

Abstract

This paper focuses on a description of a CMOS Current Steering Logic (CSL) approach, intended to work in low voltage mixed-mode environment. Performance criteria as well as a design methodology are reviewed. The design flow adopted to implement CSL gate layouts is discussed. Finally, a CSL library has been developed and validated by the implementation of an algorithm used in an offset compensation scheme for a CMOS operational amplifier.

Introduction

The MOS feature size is in the age of sub-micron technologies and is expected to go under a quarter micron by the end of this century. A direct consequence of this development is a significant reduction of the power supply voltage. Purely digital circuits are rapidly adapting to the emergent paradigms created by technology trend. The impact on analog circuits is not quite clear. However mixed-mode circuits present an additional complication owning to the interference of digital circuits on analog cells. This kind of interference is called digital switching noise and has always been a concern in mixed mode-design [1]. Nevertheless, only recently designers' skills are being formalized by theoretical and experimental work and CAD tools [2] [3].

It has been shown that digital switching noise can limit the performance of analog cells in mixed-mode circuits [4]. To overcome this problem, many techniques based on current steering have been introduced. Basically, these techniques differ from each other in signal representation, i.e., differential (Figure 1-a) or single-ended (Figure 1-b). A previous work [5] has shown that CSL technique is faster than the differential Folded Source Coupled Logic (FSCL) under low voltage and low power conditions. Although CSL is more adaptable to the emerging technology constraints. Nevertheless, its analog nature requires further investigation on aspects like mismatching and temperature effects under the expected environmental conditions.

This paper presents an overview of the CSL approach from the basic gate formulation to an application in an offset compensation scheme, including a description of a CSL library intended for low voltage environment.

CSL Inverter Analysis

A. Static and dynamic characteristics.

In the CSL inverter of Figure 1-b, the current I is shared between the logic device M_L and the diode connected device M_D.

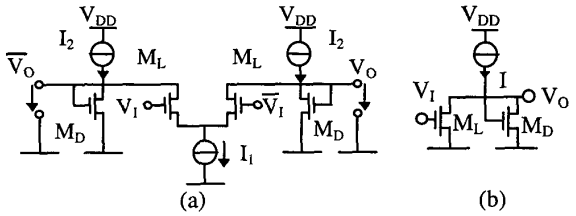

Figure 1.CMOS (a) FSCL inverter (b) CSL inverter

Static characteristics depend on Gv, which is equal to the ratio $(W/L)_L/(W/L)_D$. The values of β_L and β_D (where $\beta=\mu.C_{ox}$ (W/L) can be chosen according to some trade-off between area, noise margin and power consumption [6]. The static and dynamic characteristics were derived using the EKV MOSFET model [7], and they have been validated by simulations and measurements[8]. Table I and Table II summarize expressions to calculate static and dynamic parameters of the CSL inverter. Basic structures such as inverters, NAND and NOR gates have been integrated in the 0.7µm CMOS technology from EUROCHIP ATMEL-ES2 and measured [6].

Table I : Static Characteristics of the CSL Inverter.

Output high logic level	$V_{OH} - V_{T0} = \sqrt{\frac{2 \cdot n \cdot I \cdot Gv}{\beta_L}}$
Output low logic level	$V_{OL} = \frac{(V_{OH} - V_{T0})}{n} \cdot \left(1 - \sqrt{1 - Gv^{-1}}\right)$
Input high logic level	$V_{IH} = (V_{OH} - V_{T0}) \cdot \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{Gv^{-1}} + V_{T0}$
Input low logic level	$V_{IL} = (V_{OH} - V_{T0}) \cdot \sqrt{\frac{1}{Gv \cdot n^2 + 1}} \cdot \sqrt{Gv^{-1}} + V_{T0}$
High Noise Margin	$NM_H = V_{OH} - V_{IH}$
Low Noise Margin	$NM_L = V_{IL} - V_{OL}$

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Table II: Dynamic Characteristics of the CSL Inverter.

Fall Time	$\tau_F = A \cdot B$
Rise Time	$\tau_R = C + D$

$$A = -\frac{\frac{2 \cdot n \cdot CL}{\beta_D}}{\sqrt{\frac{2 \cdot n \cdot I}{\beta_D}} \cdot \sqrt{Gv - 1}}$$

$$B = \left\{ arctg\left[\frac{1}{\sqrt{1+Gv} \cdot \sqrt{Gv-1}}\right] - arctg\left[\frac{1}{\sqrt{Gv-1}}\right] \right\}$$

$$C = \frac{CL}{I} \cdot (V_{T0} - V_{OL})$$

$$D = \frac{n \cdot CL}{\beta_D \cdot \sqrt{\frac{2 \cdot n \cdot I}{\beta_D}}} \cdot \ln\left(\frac{\left(1 - \frac{1}{\sqrt{1+Gv}}\right)}{1 + \frac{1}{\sqrt{1+Gv}}} \right)$$

V_{T0} is the transistor threshold voltage and n is the slope factor, usually between 1 and 2, slightly dependent on the gate voltage [7].

B. Mismatching Effects

To determine the standard deviation of the high logic level noise margin –a critical design parameter– V_{OH} and V_{IH} were assumed not correlated because they are determined by two different gates.

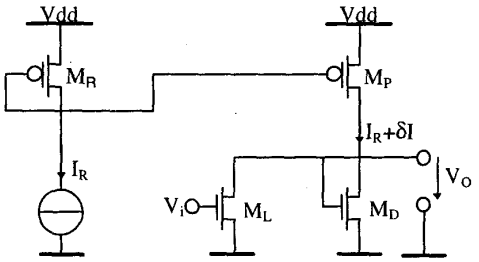

Figure 2. Circuit used to determine the effects of mismatching.

V_{OH} and V_{IH} expressions (Table I) can be modified in order to consider a variation of current (δI) introduced by the current mirror :

$$V_{OH} = \sqrt{\frac{2 \cdot n \cdot (I_R + \delta I)}{\beta_D}} + V_{T0N}^D \qquad (1)$$

$$V_{IH} = \sqrt{\frac{2 \cdot n \cdot (I_R + \delta I)}{\beta_D}} \cdot \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{\frac{\beta_D}{\beta_L}} + V_{T0N}^L \qquad (2)$$

The resulting expression for the standard deviation of high logic level noise margin is :

$$\sigma^2(\delta NM_H) = \sigma^2\left(\delta V_{T0N}^D\right) + \sigma^2\left(\delta V_{T0N}^L\right) +$$
$$\left(\frac{1}{2} \cdot \frac{n \cdot gm_R}{\beta_R} \cdot \sqrt{\frac{\beta_R}{\beta_L}}\right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_R}{\beta_R}\right) + \sigma^2\left(\frac{\delta\beta_D}{\beta_D}\right)\right) +$$
$$\left(\frac{1}{2} \cdot K \cdot \frac{n \cdot gm_R}{\beta_R} \cdot \sqrt{\frac{\beta_R}{\beta_L}}\right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_R}{\beta_R}\right) + \sigma^2\left(\frac{\delta\beta_L}{\beta_L}\right)\right) + \qquad (3)$$
$$\sigma^2\left(\delta V_{T0P}^P\right) \cdot \left(\frac{gm_R}{I_R} \cdot \sqrt{\frac{\beta_R}{\beta_D}}\right)^2 \cdot \left(K^2 + \left(\frac{1}{2} \cdot \frac{n \cdot gm_R}{\beta_R}\right)^2\right)$$

Assuming the following parameters for the CSL inverter: I_R= 20 µA, $(W/L)_D$ = 2.5µm/3µm, $(W/L)_L$ = 2.5µm/1µm and $(W/L)_P$ = 8µm/1µm. After estimating $\sigma(\delta V_T)$ and $\sigma(\delta\beta/\beta)$ of each device according to [9], the standard deviation of the noise margin is $\sigma(\delta NM_H)$ = 66 mV. An increase of the device dimensions would reduce this number, at the cost of sacrificing area and gate delay. Therefore, a robust CSL gate should have a minimum noise margin of $3 \cdot \sigma(\delta NM_H)$. The gates of the implemented CSL library present a minimum noise margin of 300mV.

C. Thermal effects

Another source of errors for the CSL gates is the thermal drift. In order to determine the dependence of the DC parameters on the temperature, the MOSFET EKV model has been used. The thermal parameters used in the EKV model are [7] :

- TCV - Threshold voltage temperature coefficient ;
- BEX - Mobility temperature exponent.

Therefore, the temperature effects on V_{OH}, V_{OL} and NM_H can be written as :

$$\Delta V_{OH} = -\frac{\Delta T \cdot BEX}{2 \cdot T_{ref}} \cdot \sqrt{\frac{2 \cdot n \cdot I}{K_P \cdot \left(\frac{W}{L}\right)_d \cdot \left(\frac{T}{T_{ref}}\right)^{2+BEX}}} - TCV \cdot \Delta T \qquad (4)$$

$$\Delta V_{OL} = \left(\Delta V_{OH} + TCV \cdot \Delta T\right) \cdot \left(1 - \sqrt{1 - Gv^{-1}}\right) \qquad (5)$$

$$\Delta NM_H = \left(\Delta V_{OH} + TCV \cdot \Delta T\right) \cdot \left(1 - \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{Gv^{-1}}\right) \qquad (6)$$

As an example, assuming the following conditions : Gv = 3, ΔT = 43°C , TCV = 2 mV/° and BEX = -1.5. The static characteristics variations due to the thermal effects are: ΔV_{OH}=162 mV, ΔV_{OL} = 45mV, and ΔNM_H = 246 mV. Therefore, the noise margin is improved by 162mV.

The analysis of equations 4 to 6 shows that when the temperature increases:

- ΔV_{OH} increase.
- ΔV_{OL} increase with a smaller rate than ΔV_{OH}.
- ΔNM_H increase, that improving the reliability of the gate.

However, when the temperature decreases, the inverse effect occur with ΔNM_H, thus affecting the reliability of this gate.

The designer should be aware of the statistical and thermal variations given by expressions (3) to (6). The maximum parameter deviation should be below a minimum in order to preserve the reliability of the gate.

CSL Library

The complete set of gates available in the CSL library were generated based on the inverter scheme (Figure 3-a), replacing the NMOS transistor by a tree (series and/or parallel) of NMOS transistors. For instance:

- A two-input NOR gate (Figure 3-b) uses two parallel NMOS transistors.
- A two-input NAND gate (Figure 3-c) uses two series NMOS transistors.

Unfortunately, this method degrades some gates noise margins. Such a problem has been solved by increasing the width of the series transistors (Figure 3-c) at the expense of a higher propagation time.

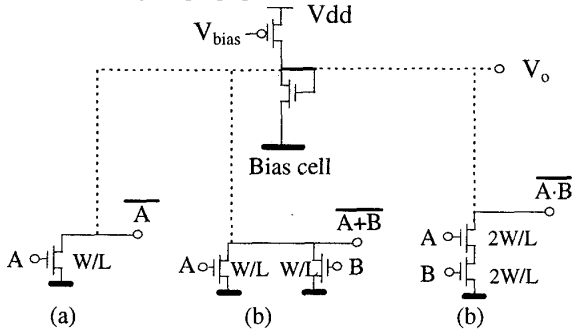

Figure 3. Circuits used in the CSL library

The realized library contains the following functions :

- Combinatorial logic gates: AND, NAND, INVERTOR, NOR, OR, XOR.
- Memory elements : Set/Reset Latch, Latch with Preset and Clear, D Flip-Flop, JK Flip-Flop.
- CMOS static logic interface from CSL output to CMOS input.
- Biasing cell with power down capability.

The CSL library was entirely designed in the Cadence environment using CAD tools which are originally dedicated to standard static logic development (Figure 4).

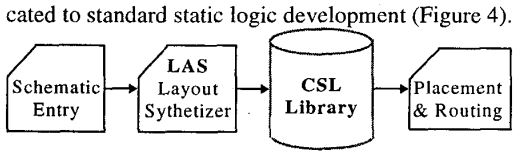

Figure 4.CAD tools used to build up the layout of the CSL library

CSL Application

The developed CSL library has been used to implement an algorithm to compensate the offset of an operational amplifier[14]. The main objectives of this system are :

- to provide 100% of duty cycle for signal processing.
- to process low frequency low voltage input signals.
- robustness against temperature variation/ mismatching.

The scheme consists of two matched operational amplifiers (OA1 and OA2) (Figure 5) working in a ping-pong architecture [12]. In this architecture, while one OA is processing a signal, the other is under offset calibration. The autozeroed technique uses a successive approximation algorithm [14].

The amplifier is very sensitive to any kind of internal and external noise owing to its high gain and low offset voltage. Note that, in this integrated circuit the power supply of the analog and digital parts are the same. No shielding technique was used to protect the analog part from the digital one.

The offset compensation scheme was selected in order to verify the efficiency of the developed CSL library in terms of area, switching noise and robustness to temperature variations.

Experimental Results

Test devices were fabricated in ATMEL-ES2 0.7µm CMOS technology, available through the EUROCHIP prototype fabrication program. The total circuit area (Figure 5) is 0.5 x 1 mm^2.

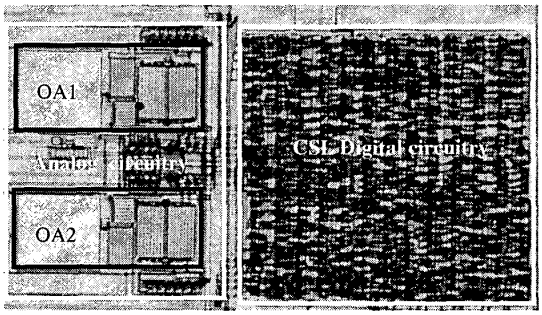

Figure 5. Photomicrograph of the chip.

Table III: Measured Chip Parameters

Parameter	Value
Supply Voltage	3V
CSL Biasing Current	20 µA
Open Loop Voltage Gain of OA	75 dB
GBW	2 MHz
CMRR	56 dB
Maximum OA DC offset	200 µV

This chip showed full functionality at the first silicon integration. Experimental results confirmed the robustness of the CSL for a temperature variation in the range from 20°C to 80°C.

The only special precautions applied at the layout level of this circuit are :

- the separation of the digital and analog parts (Figure 5) without any substrate contact,
- the careful routing of the clock signal to avoid cross talk between the analog circuits and this signal.

In order to measure the switching noise generated by the digital CSL circuitry, one of the integrated operational amplifier was connected in open loop configuration (Figure 6) and used as a noise sensor, when the digital circuitry is in activity.

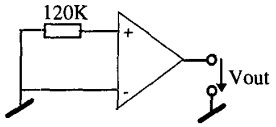

Figure 6. Open loop OA configuration used as noise sensor.

V_{out} has been measured under the following conditions :

- OA Offset voltage = 4μV.
- DC open loop gain = 75 dB.
- Clock frequency = 1kHz.

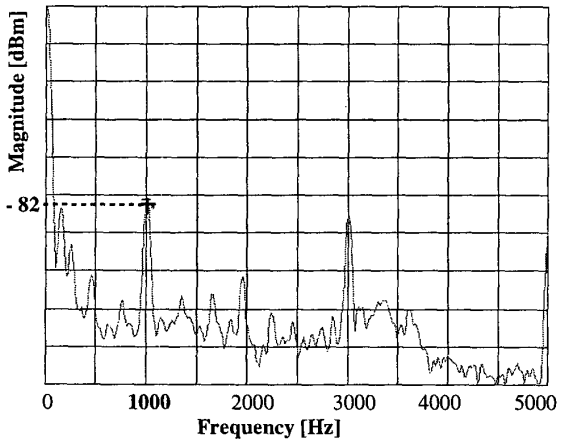

Figure 7. Measured OA output signal.

Figure 7 shows the spectral analysis of the OA's output. Note that a peak appears at the clock frequency (1 KHz) and displays -82 dBm. Considering the proximity between analog and digital parts, and the high gain of the amplifier at the clock frequency, the measured amplitude is very small. This experiment has demonstrated that the switching noise generated by the CSL circuitry is very low.

Conclusion

This paper has presented an overview of the CSL first and second order theoretical formulations. Which are experimentally measured and validated.

In order to demonstrate the feasibility of the CSL technique for industrial applications, a new CSL library was designed and successfully tested. Moreover, the CSL cells were employed to implement an autozeroed compensation scheme. This application has demonstrated the potential of the CSL approach as a silent circuit.

Acknowledgment

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