A COMPACT CHARGE-BASED MOSFET MODEL FOR CIRCUIT SIMULATION

O. C. Gouveia Filho¹, A. I. A. Cunha², M. C. Schneider¹ and C. Galup-Montoro¹,³

¹LINSE - Departamento de Engenharia Elétrica - UFSC - C.P. 476
88 040 900 Florianópolis - SC - Brasil
E-mail: ogouveia@linse.ufsc.br

²Departamento de Engenharia Elétrica da Escola Politécnica - UFBA
40210-630 Salvador - BA - Brasil

³Texas A & M University - Department of Electrical Engineering
College Station - Texas - 77843-3128 - EUA

Abstract
This paper presents a physically based model for the MOS transistor suitable for design and simulation of integrated circuits. The static and dynamic characteristics of the MOSFET are accurately described by single-piece functions of the inversion charge densities at source and drain. A new compact and physical approach to short-channel effects is presented. We have run some tests to compare the performances of our model and widely used MOSFET models.

1. INTRODUCTION
MOSFET models included in circuit simulators can be classified into the following three categories [1]: analytical models, table lookup models and empirical models. Almost all the models in current use are analytical.

Most MOSFET analytical models are based on either the regional approach or surface potential formulations, or semi-empirical equations [2]. Models based on the regional approach use different set of equations to describe the weak and strong inversion regions, generally bridged by using a non-physical curve fitting. Models based on surface potential formulation are inherently continuous; however, they demand the solution of an implicit equation for the surface potential. Semi-empirical models are usually neither scalable nor suited for statistical analysis.

This paper presents a charge-based physical model [2 - 4] of the MOSFET. All the large and small-signal characteristics are given by single-piece expressions with infinite order of continuity (C∞ functions). Our model preserves the structural source-drain symmetry of the transistor and uses a reduced number of physical parameters. It is also charge-conserving and has explicit equations for its 16 transcapacitances. Moreover, short-channel effects are easily introduced by using a charge-based model.

The fundamentals of our model are presented in Section 2 while its implementation in a circuit simulator is described in Section 3. Section 4 presents some examples of simulation to compare the relative performances of our model, EKV, SPICE3, and BSIMv3 models.

2. FUNDAMENTALS
The fundamental assumption of our model is the linear dependence of the inversion charge density $Q_i$ on the surface potential $\phi_s$ [2, 6], for a given gate-to-substrate voltage ($V_G$):

$$dQ_i = nC_{ox}d\phi_s$$  \hspace{1cm} (1)

where $C_{ox}$ is the oxide capacitance per unit area and $n$ is the slope factor, slightly dependent on the gate voltage [2-5].

Equation (1) has allowed the model in [2] to be fully formulated in terms of the inversion charge densities at the source ($Q_{is}$) and drain ($Q_{id}$) channel ends. The relationship between the inversion charge density and the terminal voltages is [4,7]

$$V_s - V_C = \phi_s \left[ \frac{Q_{ip} - Q_i}{nC_{ox} \phi_s} + \ln \left( \frac{Q_{is}}{Q_{id}} \right) \right]$$ \hspace{1cm} (2)

where $V_C$ is the channel voltage, $V_p$ is the pinch-off voltage, $Q_{ip}$ is the inversion charge density at pinch-off and $\phi_t$ is the thermal voltage. All the voltages are referred to the local substrate, as in [3-5]. Equation (2) cannot be solved analytically for $Q_i$; but it can be approximated by the following expression [4]:

491 0-7803-5008-1/98/$10.00©1998 IEEE.
\[ q = \ln \left[ 1 + \frac{e^{u-1}}{1 + k(u) \ln(1 + e^{u-1})} \right] \quad (3) \]

with \[ k(u) = 1 - \frac{84.4839}{u^2 + 150.8640} \quad (4) \]

where \[ u = \frac{V_p - V_{SDP}}{\phi_i} \] and \[ q = -\frac{Q'_{IS(D)}}{nC_{ox} \phi_i} \quad (5) \]

3. MOSFET MODEL

3.1. Short and narrow channel effects

If velocity saturation effects are negligible, the drain current of a MOS transistor can be written as

\[ I_D = f(V_p, V_D) - f(V_p, V_D) \quad (6) \]

For a long and wide transistor the pinch-off voltage is a function of \( V_D \) only, but for short and narrow channel devices \( V_p \) is a function of \( V_G \), \( V_S \) and \( V_D \). To keep the symmetry of equation (6), \( V_p \) is modeled as

\[ V_p(V_G, V_S, V_D) = V_{po}(V_G) + \sigma \left( V_D + V_S \right) \quad (7) \]

\( V_{po}(V_G) \) is the pinch-off voltage at equilibrium \( (V_G = V_S = 0) \) and is given by

\[ V_{po} = \left( V_G - V_{th} + \phi_o + 2\phi_o \frac{1}{2} + \gamma' \right)^2 \quad (8a) \]

\[ \gamma' = \gamma - \frac{eV_{gs}}{C_{ox}L_{eff}} \left[ \frac{2\eta_l}{L_{eff}} + \frac{3NP \eta_w}{W_{eff}} \right] \sqrt{\phi_o} \quad (8b) \]

where \( \phi_o \) is a fitting parameter whose value is about twice the Fermi potential \( (2\phi_F) \) and \( V_{th} \) is the threshold voltage at equilibrium. \( \gamma' \) is the body effect coefficient modified to include short and narrow channel effects. \( \eta_l \) and \( \eta_w \) are parameters to be adjusted; \( L_{eff} \) and \( W_{eff} \) are the effective length and width, respectively. The parameter \( \sigma \) accounts for the drain induced barrier lowering (DIBL) \( (7) \) and is proportional to \( 1/L_{eff}^2 \).

3.2 Mobility reduction [4]

The mobility reduction due to the vertical field is modeled by

\[ \mu = \frac{\mu_0}{1 + \theta \cdot \sqrt{V_{po} + \phi_o}} \quad (9) \]

where \( \mu_0 \) is the zero bias mobility, and \( \theta \) is a fitting parameter.

3.3 Velocity saturation

The effect of velocity saturation in our model is based on the expression [6] below:

\[ \mu_S = \frac{\mu}{1 + \frac{\mu}{v_{lim} \frac{d\phi_f}{dx}}} \quad (10) \]

The substitution of both the approximations (1) and (10) into the differential equation of the drain current leads, after integration along the channel, to [4, 6]

\[ I_D = \frac{\mu W_{eff}}{C_{ox}L_{eq} \phi} \frac{1}{1+\frac{Q_{th}}{Q_{ox}}} \left[ Q_{th} - Q_{ox} \right] \frac{2nC_{ox} \phi_{th}}{Q_x} \quad (11) \]

\[ Q_{th} = nC_{ox} \cdot L_{eq} \frac{V_{lim}}{\mu} \quad (12) \]

\( v_{lim} \) is the saturation velocity and \( I_{th} = L_{eff} \cdot \Delta L \). The channel length modulation (\( \Delta L \)) is modeled as in [7]. The maximum current that can flow in the channel occurs when saturation velocity is reached:

\[ I_D = -Wv_{lim}Q_{th} \quad (13) \]

Equating (11) to (13) allows one to calculate the value of \( Q_{th} \) which corresponds to saturation

\[ Q_{th} = Q_{th} - nC_{ox} \phi - Q_{ox} \left[ 1 - \frac{2(Q_{th} - nC_{ox} \phi)}{Q_{th} - Q_{ox} \phi} \frac{(nC_{ox} \phi)^2}{Q_{th}^2} \right] \quad (14) \]

\( V_{th} \) is calculated from (2).

3.4 Charge equations and capacitances

Models that do not conserve charge generate critical errors for the analysis and design of a variety of widely employed MOS circuits such as switched capacitors, switched current and dynamic memories. Charge nonconservation occurs due to the use of capacitance models instead of charge models [8]. Our model is charge-based and has explicit equations for the source, drain, bulk, and gate charges. The charge equations in our model are continuous and have continuous derivatives in all regions of operation, allowing for the calculation of the 16 MOSFET (trans)capacitances [2].

4. RESULTS

The results shown in figures 1 to 3 correspond to the tests 1 to 3 suggested in [9] to evaluate the performance of a model. They show that our model is continuous.
from weak to strong inversion and represents well the moderate inversion region. The plot of the ratio $g_m/I_D$ versus $V_G$ presents the expected shape. No discontinuities are observed in $g_m$. The DC characteristics of our MOSFET model are in close agreement with those of the EKV model. Figure 4 shows 9 independent MOSFET (trans)c capacitances. All the curves are continuous and vary smoothly. A test to verify charge conservation in the sample-hold circuit shown in figure 5 was performed using both our model and SPICE3 from SMASH [10], as well as BSIM3v3 from T-SPICE [11]. Figure 6 shows the simulation results. Our model and BSIM3v3 give results consistent with the physical behavior while SPICE3 does not.

5. CONCLUSIONS

A compact MOSFET model for circuit simulation has been presented. Simulations using NMOS transistor have shown that the proposed model attains the criterion of continuity. The simulation of a sample-hold circuit showed that our model as well as BSIM3v3 conserve charge, while the SPICE3 model does not. Some advantages of our model over BSIM3v3 are the use of compact expressions to describe all regions of operation as well as a smaller number of device parameters.

Fig. 1. log($I_D$) x $V_G$ for our model

Fig. 2. $g_m/I_D$ x $V_G$ for our model

Fig. 3. log($g_m$) x $V_G$ for our model

Fig. 4. (a) Comparisons between the 5 capacitances available in EKV and those of our model (b) 4 capacitances in our model that are not modeled in EKV. The simulations were run in SMASH.
Acknowledgments

The authors would like to thank CAPES and CNPq (from the Brazilian Ministries of Education and Science and Technology) for the financial support, and Dolphin Integration, France for licensing SMASH simulator.

References