A PROGRAMMABLE LOW VOLTAGE SWITCHED-CURRENT FIR FILTER

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Abstract

In this paper we describe a 20MHz sample rate switched-current Finite Impulse Response (FIR) filter, suitable for equalizer architectures. The basic cell of the FIR filter is the switched-current (SI) sample-and-hold (S/H) circuit proposed in [1], appropriate for low voltage operation. The programmability of the FIR filter structure is achieved via MOSFET-Only Current Dividers (MOCD) [2]. The FIR filter has been designed using the AMS 0.8um CMOS process. The power consumption per tap is 12mW at ±1.5V power supply.

I – Introduction

Digital communication channels have bandwidth limitations and other non-idealities that cause intersymbol interference (ISI) [3,4]. ISI limits the speed of communication systems and the density of storage systems and is minimized by channel equalization. In most equalizer circuits, a programmable FIR filter is used. Because many consumer, telecommunication and computing products are battery-powered, there is a trend towards low power, low voltage operated circuits. Following this trend, this paper presents a programmable switched-current FIR filter which is suitable for low voltage operation. The FIR filter is based on a circular delay line architecture [5]. This paper is divided into three parts. Section II describes the filter structure. The switched-current realization and simulation of the FIR filter are presented in section III. Section IV summarizes the results about this paper.

II – Circular delay line structure

In the traditional direct or transposed forms of the FIR filter structure [6], the signal is moved from one memory cell to the next on each clock cycle, resulting in an analog delay line. In the analog delay line structure, errors such as noise and offset are accumulated up to the ultimate tap. To avoid this drawback, the circular FIR structure [5] has been proposed (Fig. 1). The signal flow through the FIR filter is described as follows :

- During ck1, the S/H 1 is in the sampling mode (active) and the other S/H's are in the holding mode. The filter coefficients and the stored signals are distributed as shown in Fig. 1.
- On ck2 (S/H 2 is active), the stored value of the S/H 1 is not moved to next delay cell (S/H 2), but its tap weight is changed from a_1 to a_2. Also, all the tap weights must be shifted, as shown in Fig (1.a), to realize Eqn. 1.

$$H(Z) = a_1 + a_2 Z^{-1} + a_3 Z^{-2} + a_4 Z^{-3} \qquad (1)$$

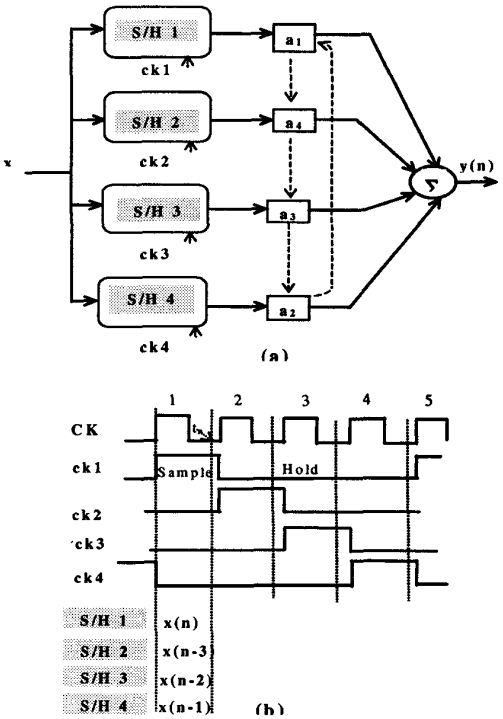

Fig. 1. (a) Circular FIR filter (coefficients during ck1). **(b)** Clock waveforms.

The circulating process continues on each clock cycle thus cycling the digital coefficients through all the multipliers. This process simulates a tapped delay line without passing the sampled value into series delay elements on each clock cycle. Consequently, this structure has the advantage of avoiding the propagation of offset voltage and noise from each cell to the next.

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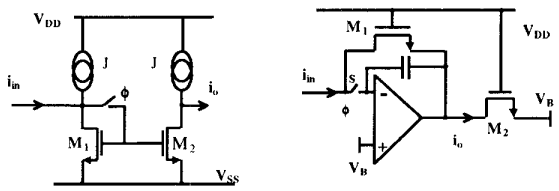
III- The Switched-Current Realization of the Circular FIR Filter

(III-1) The sample-and-hold circuit

The sample-and-hold circuit can be built as a switched-capacitor (SC) integrator with zero initial condition on each clock cycle. In the SC technique, the op amp design is relatively complicated due to the change of the load capacitance on each clock phase. Moreover, programmable SC circuits require capacitor arrays, which occupy a large active area compared with the binary weighted transistor array and the MOCD structures in the SI technique. In the switched-current technique [1, 7], the S/H element can be realized as shown in Fig. 2.



(a) The conventional SI technique [7]. (b) The SI technique [1] for low Voltage supply.

Fig. 2. S/H implementation in SI techniques.

In this work, the technique for switched-current (SI) circuits proposed in [1, 8] has been used. This SI technique avoids the conduction gap [9] by properly biasing the switches. Therefore, it is more suitable for low voltage applications than the conventional SI technique [7]. In this switched-current method, shown in Fig. (2.b), the current is processed in two steps:

- Track mode : the input current is fed to the cell when switch "s" (ϕ) is closed. The current is memorized as a voltage across the holding capacitor. It should be emphasized that linear capacitors are not needed to store the data.
- Sampled mode: when switch "s" opens, the voltage is held on the capacitor. This voltage causes $i_o=-i_{in}$ as long as M_1 and M_2 have the same aspect ratios.

In the SI structure shown in Fig. (2.b), all the switches operate at a constant DC voltage, equal to V_B, thus causing both the charge injection and switch opening time [10] to be signal independent.

(III-2) The MOCD

The schematic of the MOCD together with its symbol are shown in Fig. 3. The output currents of the MOCD are digitally controlled fractions of the input current. In the SI technique proposed here, the MOCD structure is used as the digitally programmable element. The MOCD has an input impedance independent of both the digital word and the clock phase, thus providing a constant load impedance to the op amps. Without trimming techniques, MOCD's easily achieve 6-bit resolution, which is sufficient for disk drive circuits [6].

(III-3) The FIR architecture

The S/H circuit and the programmable MOCD have been used for the SI implementation of a 4-tap circular FIR filter, as shown in Fig. 4. In the sample mode of each cell, the corresponding switch of the cell must be closed (ck1 for the first delay cell, for example) while the others are open. Fig. 5 shows details about the switching methodology of the FIR filter structure shown in Fig. 4 at different clock cycles. Here, we propose a clock scheme to reduce the injected charge into the holding capacitor due to MOCD (M_{3L}). The scheme is shown in Fig. 5. Switch "S2" has to open before M_{3L} turns off to avoid the charge injected by M_{3L} to be stored into the holding capacitor.

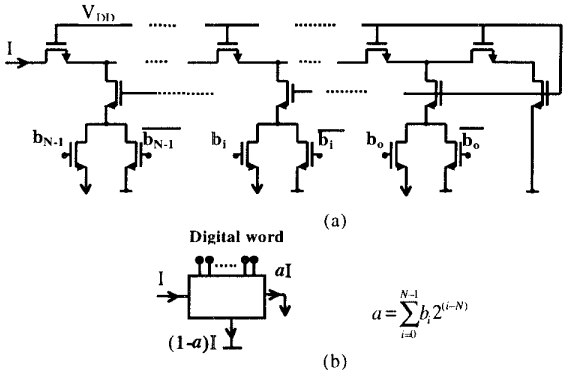


Fig. 3. The MOCD circuit scheme and its symbol.

To validate our analysis, the circuit shown in Fig. (5.a) has been simulated with SMASH [11] for a 10μA input current and using 2μm/0.8μm n-channel switches. The ACM model [12] has been used for the transistors. M and M_{3L} have aspect ratios equal to 6μm/5μm and the holding capacitor is 0.5 pF. Two-stage CMOS op amps have been designed using the methodology described in [13].

The bias voltage (V_B) has been generated using the voltage divider scheme proposed in [1].The overall switched current FIR filter shown in Fig. 4 has been simulated. The output current is shown in Fig. 6. The DC offset current and spikes have been suppressed using the clock scheme of Fig. (5.b). The programmability of the filter is shown in Fig. 7.

IV- Conclusion

A programmable switched-current FIR filter has been proposed using the circulating tap technique. The problem of low voltage switches has been overcome by using the SI technique described in [1, 8]. A 4-tap FIR filter has been designed and simulated. The total power dissipation is 48mW from a ±1.5V power supply. The results of the simulations show that the applied SI technique is very

promising for the implementation of programmable low voltage FIR filters.

ACKNOWLEDGMENTS

The authors would like to thank the financial support of CNPq, the Brazilian Research Council.

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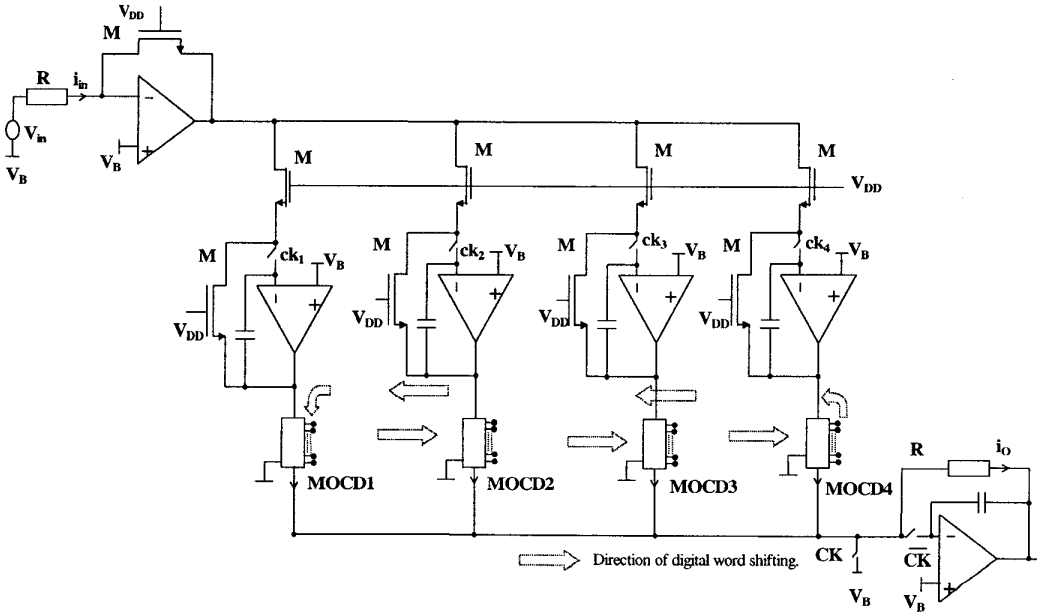


Fig. 4. The SI 4-tap FIR realization in circulating form.

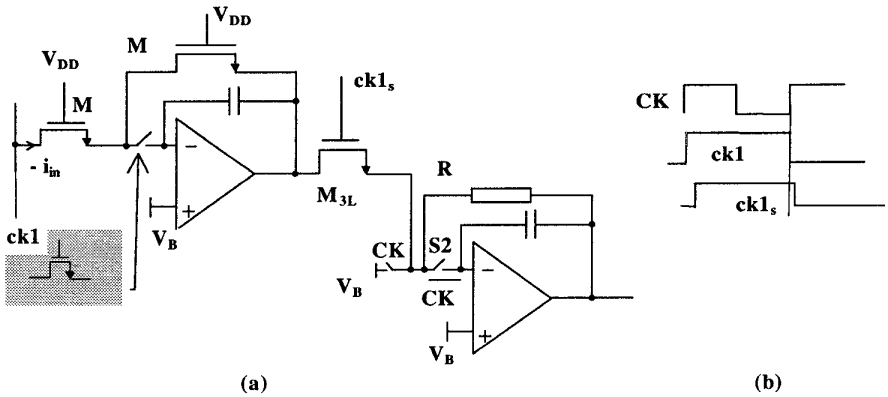


Fig. 5. (a) The basic S/H cell and the summer block. **(b)** Proposed clock scheme.
Obs: M_{3L} is equivalent to an MOCD in Fig. 4.

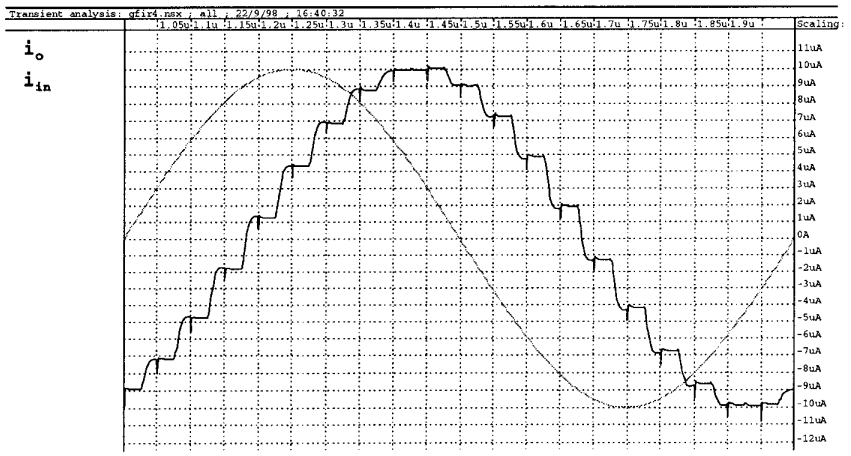
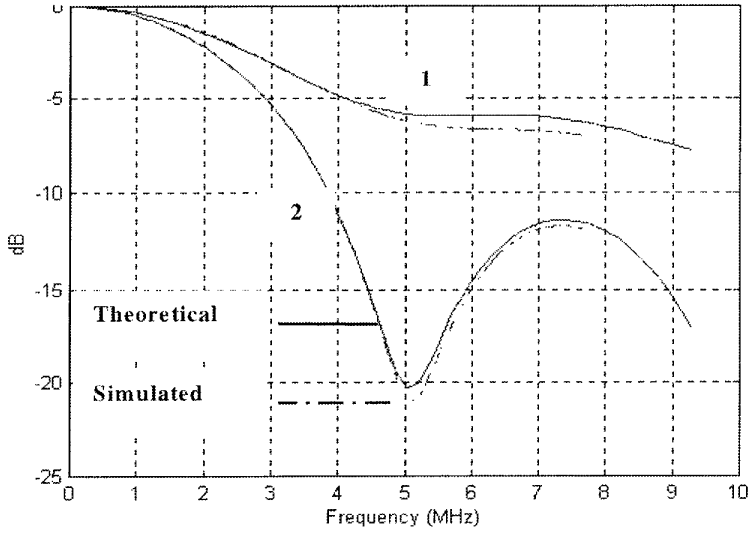


Fig. 6. Pure delay of 4 clock cycles (a_1=a_2= a_3=00 and a_4 =3F).



a_1 =3F , a_2 =15, a_3 =0B and a_4 =06.
a_1 =3F , a_2 =36, a_3 =2E and a_4 =27 .

Fig. 7. The magnitude response of the filter for different digital words.