OPTIMAL DESIGN OF LOW POWER NESTED GM-C COMPENSATION AMPLIFIERS USING A CURRENT-BASED MOS TRANSISTOR MODEL

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ABSTRACT

A sound design of low power multistage amplifiers is presented. The amplifiers are stabilized by Nested Transconductance-Capacitance Compensation (NGCC). The key for an optimal design is a current-based MOSFET transistor model, which allows the amplifiers to be designed in moderate inversion. With 2 V supply voltage and 10 kΩ/20 pF load, a four-stage amplifier implemented in a 1.2 μm n-well CMOS process achieved 1.03 MHz gain bandwidth product, 103 dB open loop gain and 62.7° phase margin with a power consumption of 0.3 mW. The active area of the amplifier is 0.0052 mm^2. With the same specifications, a three-stage amplifier was also integrated in the 1.2 μm n-well CMOS process. Compared to the design in strong inversion, both amplifiers satisfy the specifications while the power consumption is reduced by a factor of 3.

1. INTRODUCTION

Low power operational amplifiers are widely used in many mixed signal applications such as mobile communication and other portable systems. Since low voltage is applied to scale down the power consumption, cascoding is no longer a suitable solution to enhance the gain of the amplifiers. Multistage cascading is required for those high gain amplifiers. The stability is one of the most important issues in designing multistage amplifiers [1]. One technique for multistage amplifier design is a Nested Miller Compensation (NMC) structure, which uses Miller capacitors to split poles [1]-[2]. The transfer function of an NMC amplifier is complicated by the zeros associated with pole splitting. In our design, amplifiers are stabilized by a Nested Transconductance-Capacitance Compensation (NGCC) topology [3]-[5]. This topology is similar to the NMC technique, except that extra feed-forward stages are added to cancel the zeros.

In addition to low supply voltage, low operating current is another effort to reduce the power consumption. Low current implies that transistors will operate in weak or moderate inversion. As design approaches weak inversion, the sizes of the transistors and the speed of the circuits become the most important concerns. Optimization of power, speed and area can be obtained in moderate inversion. However, conventional MOSFET transistor models only have separated expressions for strong and weak inversion. Most designs generally assume strong inversion and use the transistor gate voltage as the key design parameter [6]. New MOSFET transistor models which are universal for any inversion level have become available in recent years [7]-[8]. Low voltage NGCC amplifier [4] designed in strong inversion can go further to reduce the power consumption using the new models.

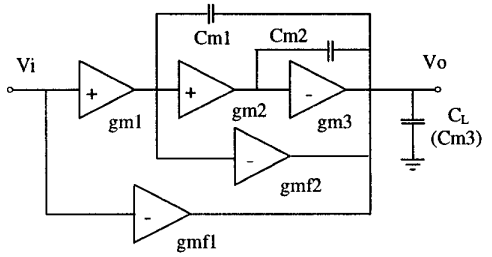

Figure 1. Three-stage NGCC amplifier topology

The purpose of this work is the design of three-stage and four-stage NGCC amplifiers [4] in moderate inversion by using a current-based MOSFET transistor model [7]. We describe the NGCC topology in Section 2. In Section 3 we briefly introduce the current-based transistor model. Implementations of the amplifiers are presented in Section 4. Simulation results are summarized in Section 5, and conclusions are given in Section 6.

2. TOPOLOGY OF NGCC AMPLIFIERS

We start with the architecture of a three-stage NGCC amplifier as shown in Fig. 1. Besides the feedback paths through the Miller capacitors for pole splitting, additional stages g_{mf1} and g_{mf2} are used to cancel the Right Half Plane (RHP) zeros introduced by the Miller capacitors. Ignoring the parasitic capacitance at input and output nodes, each stage can be modeled as a transconductance amplifier g_{mi} with an output conductance g_{oi}. Making $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$, the RHP zeros will be eliminated. Assuming one dominant pole at low frequency and other two poles at high frequency, we can write the transfer function as

$$H(s)=\frac{V_o(s)}{V_i(s)}=\frac{-k_1k_2k_3}{\left(1+s\frac{k_1k_2k_3}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2f_3}\right)} \qquad (1)$$

where $k_i = g_{mi}/g_{oi}$ and $f_i = g_{mi}/C_{mi}$. f_1 determines the unity gain frequency (GB) and $A_o = k_1k_2k_3$ is the dc gain. The phase margin of the amplifier is given as

$$PM \cong 90^o - \tan^{-1}\frac{1}{\left(\frac{f_2}{GB}-\frac{GB}{f_3}\right)} \qquad (2)$$

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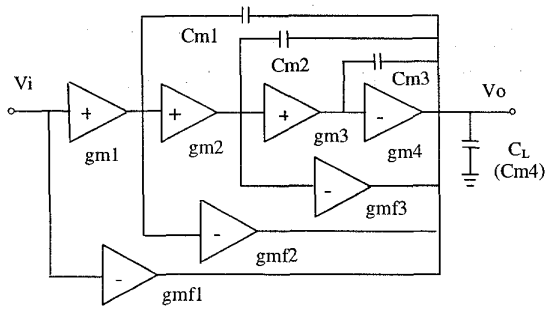

Figure 2. Four-stage NGCC amplifier topology

A four-stage NGCC amplifier is formed by adding one more inner gain stage to the three-stage amplifier (Fig. 2). The transfer function of a four-stage NGCC amplifier is written as

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{\left(1+\frac{A_0 s}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\frac{s^3}{f_2 f_3 f_4}\right)} \tag{3}$$

where $A_o = k_1 k_2 k_3 k_4$. Letting $f_1 = GB$ and assuming f_3 and f_4 are both greater than f_2, from (3) the phase margin of a four-stage amplifier can be approximated as

$$\begin{aligned} PM &= 90^o - \tan^{-1}\left(\frac{GB}{f_2}\times\frac{1-GB^2/f_3 f_4}{1-GB^2/f_2 f_4}\right) \\ &\approx 90^o - \tan^{-1}\left(\frac{GB}{f_2}\right) \end{aligned} \tag{4}$$

In realizing low power NGCC amplifiers, transistor sizes increase drastically when design approaches weak inversion. The parasitic effect associated with the large area aggravates the stability of the amplifiers. For a three-stage op amp, we may need to increase the channel length of the transistors to obtain adequate gain. The parasitic is more significant if long-channel transistors are used. To have a positive gain, the second stage of a three-stage amplifier includes a current mirror that may cause a phase delay τ on g_{m2}. Involving these factors, (1) is not exactly applicable for low power design. After including the dominant parasitic capacitance C_i at the output of each stage and replacing g_{m2} by $g_{m2}(1-\tau)$ for taking the phase shift into account, the transfer function of the three-stage NGCC amplifier becomes

$$H'(s) = -\frac{A_0 + a_1 s + a_2 s^2}{\left(1+s\frac{A_0}{f_1'}\right)\left(1+\frac{s}{f_2'}+\frac{s^2}{f_2' f_3'}\right)} \tag{5}$$

where

$$a_1 = k_1 k_2\left(\frac{C_2}{g_{o3}} - k_3\tau\right)$$

$$a_2 = k_1\left(\frac{C_1(C_2+C_{m2})}{g_{o2}g_{o3}} + k_2\tau\frac{C_{m2}}{g_{o3}}\right)$$

The denominator of (5) is written in the same way as done in (1) by replacing f_i by f_i'. It is found $f_1' = f_1$ while the parameters f_2' and f_3' are given as

$$f_2' = f_2\frac{1}{1+\varepsilon_1+\varepsilon_2\frac{g_{m2}}{g_{m3}} - f_2\tau + \frac{g_{o3}}{g_{m3}}(1+\varepsilon_1)(1+\varepsilon_2)}$$

$$f_3' = f_3\frac{\frac{1}{1+\varepsilon_2} - f_2\tau\frac{1}{1+\varepsilon_1}\frac{1}{1+\varepsilon_2} + \frac{g_{o3}}{g_{m3}} + \frac{g_{m2}}{g_{m3}}\frac{1}{1+\varepsilon_1}\frac{\varepsilon_2}{1+\varepsilon_2}}{1+\frac{C_3}{C_L}+\frac{C_2}{C_L}\frac{1}{1+\varepsilon_2}+\frac{C_1}{C_L}\frac{1}{1+\varepsilon_1}+\frac{g_{m2}\tau}{C_L}\frac{1}{1+\varepsilon_1}\frac{1}{1+\varepsilon_2}}$$

with $\varepsilon_1 = C_1/C_{m1}$ and $\varepsilon_2 = C_2/C_{m2}$. When the parasitic capacitance C_i are comparable to C_{mi} and C_L, f_2' and f_3' will be much smaller than their nominal values f_2 and f_3 based on ideal design. For good stability, the transistors are kept working in moderate inversion to avoid overwhelming parasitic effect.

3. CURRENT-BASED TRANSISTOR MODEL

To design the amplifiers in moderate inversion, a current-based MOSFET transistor model [7] was applied for our demand. This new model has a unique and continuous single expression for MOSFET characteristics in weak, moderate and strong inversion. The main design equations of this new model are written as

$$\frac{I}{\phi_t g_m n} = \frac{1+\sqrt{1+i_f}}{2} \tag{6}$$

$$f_T = \frac{\mu\phi_t}{2\pi L^2}2\left(\sqrt{1+i_f}-1\right) \tag{7}$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t}\frac{1}{\sqrt{1+i_f}-1} \tag{8}$$

$$\frac{V_{DSAT}}{\phi_t} \cong \left(\sqrt{1+i_f}-1\right)+0.1 \tag{9}$$

where

I — drain current in transistor
g_m — transconductance in saturation
n — slope factor
ϕ_t — thermal voltage
i_f — inversion level of the transistor defined as $i_f = I/I_s$,

while $I_s = \mu n C_{ox}\frac{\phi_t^2}{2}\frac{W}{L}$ is the normalization current.

Substituting (6) into (8), we obtain another expression of (8) as

$$\frac{W}{L} = \frac{g_m}{2\mu C_{ox}\phi_t\left(\frac{I}{\phi_t g_m n}-1\right)} \tag{10}$$

(6) - (10) show that the inversion level i_f plays a key role in design applications using this model. Transistors operate in weak inversion for $i_f << 1$ and in strong inversion for $i_f >> 1$. Given the transconductance of a transistor, the dimension can be determined by specifying either the inversion level or the drain current.

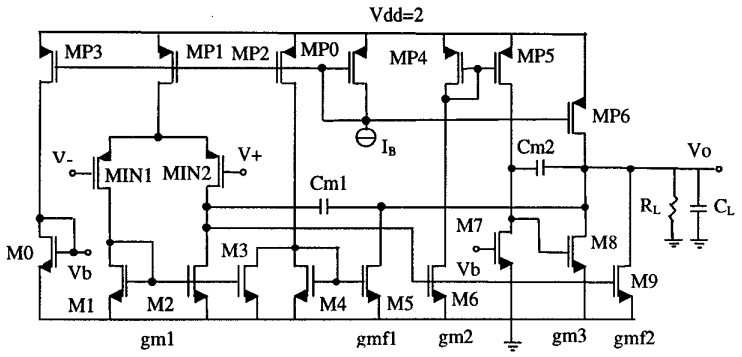

Figure 3. Implementation of three-stage NGCC amplifier

TABLE I

TRANSISTORS DIMENSIONS OF THE THREE-STAGE AMPLIFIER

Transistor NO.	W(μm)	L(μm)	i_f
M_1 — M_4	1×18	4.2	20
M_0, M_5	2×18	4.2	20
M_6, M_7, M_9	6×18	4.2	20
M_8	25×18	4.2	20
M_{IN1}, M_{IN2}	20×18	4.2	4
M_{P0} — M_{P3}	2×18	4.2	80
M_{P4}, M_{P5}	6×18	4.2	80
M_{P6}	33×18	4.2	80

4. DESIGN PROCEDURE

By using the current-based transistor model, a three-stage and a four-stage amplifier were designed in moderate inversion while a four-stage reference amplifier was designed in strong inversion for comparison. The design methodology based on the new transistor model can be applied to other design. The supplied voltage is 2 V and the load condition is 10 kΩ/20 pF. The design specifications are: i) *GB* = 1 *MHz*, dc gain ≥ 100 *dB*, phase margin $PM \geq 60^o$; ii) as a unity gain follower, 0.2% settling time $T_s < 1\ \mu S$. It is also possible to add other performance aspects (noise, slew rate, common mode rejection, etc.) into the specifications once they can be determined by g_m, I and i_f. In section 3, we mentioned that either drain current or inversion level i_f can be chosen as a design parameter. To approach the optimization of operating current and main performances, moderate inversion level was mainly used as a design parameter.

The architecture of the three-stage NGCC amplifier is illustrated in Fig. 3. The input stage is a single-ended differential amplifier that determines the gain bandwidth product (GB). The second stage uses a current mirror along with an inverter to have positive gain. The output stage is an inverter realized with single transistor. Additionally the feed-forward path g_{mf2} is also realized with single transistor. The condition $g_{mf2} = g_{m2}$ implies that transistors M_6 and M_9 should be closely matched. Making $g_{mf1} = g_{m1}$ needs more precaution since five transistors M_1 - M_5 are involved in the realization of g_{mf1}.

First we need to calculate the transconductance g_{mi} of each stage. The gain bandwidth product *GB* determines f_1. To ensure $PM \geq 60^o$, from (2) we obtain the following inequality

$$\frac{f_2}{GB} - \frac{GB}{f_3} \geq 1.732$$

Ideally, by choosing $f_2 = 2\ GB$, a 60° phase margin can be achieved as long as $f_3 > 4\ GB$. According to the analysis in section 2, f_2 and f_3 will be smaller than their nominal values due to the significant parasitic effect so that the phase margin will be much smaller than its design value. Since the phase margin is mainly determined by f_2, we can choose a relatively larger value of f_2 to compensate the reduction on phase margin. Given $f_2 = 3\ GB$, it seems that choosing f_3 has much more freedom. At this point, another critical parameter, the settling time, is needed to limit the possible range of f_3. For a four-stage NGCC amplifier, the settling time is related to the combination of f_2, f_3 and f_4. The analysis on the settling time for a four-stage NGCC amplifier is also applicable to a three-stage amplifier, which is equivalent to pushing f_4 to infinity. For the three-stage amplifier, we choose $f_3 = 5\ GB$ for $f_2 = 3\ GB$ to optimize the settling time and power consumption. Given $C_{m1} = C_{m2} = 8$ pF, we can calculate the transconductance of each stage from the definition of f_i.

To avoid large parasitic capacitance, for the PMOS transistors, only the input transistors M_{IN1}, M_{IN2} work in moderate inversion. Choosing $i_f = 4$ for M_{IN1}, M_{IN2} and substituting it along with g_{m1} into (6) give the drain current. The dimensional ratio W/L of M_{IN1} and M_{IN2} can be calculated from (8). For all other PMOS transistors in the current mirrors, we choose $i_f = 80$ to let them operate in strong inversion for good matching and low noise. Their transconductance and W/L can be calculated from (6) and (10) once the drain currents are determined.

The transconductance of transistor M_1 (or M_2) is assumed to be half of g_{m1}. With the same drain current as that of M_{IN1}, the inversion level and W/L of transistors M_1 and M_2 are obtained from (6) and (10) respectively. Again assuming that all the NMOS transistors operate at the same inversion level, from (6) and (8) we know that the drain current and W/L of these transistors are only proportional to their transconductance. The NMOS transistors realize g_{m2}, g_{m3}, g_{mf1} and g_{mf2}, the W/L and drain current can be determined based on the ratios of their transconductance to M_1. The dimensions and inversion levels of the transistors in the three-stage NGCC amplifier are listed in Table I.

The four-stage amplifier designed in moderate inversion has one more inner gain stage. The parasitic capacitance is reduced since shorter channel length is used for the transistors. Only the parasitic effect at final stage is dominated because of large transistor size. With the aid of analysis on the settling time, we choose $f_1 = GB$, $f_2 = 2\ GB$, $f_3 = 5\ GB$ and $f_4 = 6\ GB$ by taking only the parasitic capacitance at the output stage into account. Given $C_{m1} = C_{m2} = C_{m3} = 8$ pF, the dimensions and inversion levels of the transistors were determined following the same procedure used for the three-stage amplifier. The reference four-stage amplifier was designed in strong inversion. It is the conventional design approach as in [4].

TABLE II

SIMULATION RESULTS OF THE NGCC AMPLIFIERS (V_{DD} = 2 V, Z_{LOAD} = 10 kΩ/20 pF)

	Specifications	Three-Stage	Four-Stage	Four-Stage(ref.)
Power Consumption	Minimum	0.28 mW	0.30 mW	0.93 mW
DC Gain	≥ 100 dB	~ 100 dB	~ 105 dB	~ 110 dB
Gain Bandwidth	1.0 MHz	1.08 MHz	1.03 MHz	1.09 MHz
Phase Margin	> 60°	59.5°	62.7°	61.2°
0.2% Settling Time (100 mV)	< 1 μS	0.77 μS	0.55 μS	0.53 μS
THD (1kHz $1V_{P-P}$)		- 84.8 dB	- 88 dB	- 55.8 dB
1% THD Input (1kHz)		1.36V	1.38V	1.26V
Active Area (relative area)		0.01mm^2(1.75)	0.0052 mm^2(0.91)	0.0057 mm^2(1)
min i_f, max i_f		4 , 80	6 , 30	100 , 130

5. SIMULATION RESULTS

These amplifiers were simulated with BSIM (HSPICE level 13) transistor parameters in the 1.2 μm AMI n-well CMOS technology. The open-loop dc and ac responses were first simulated to characterize the gain, gain bandwidth product and phase margin of the amplifiers. The transconductance and drain current of each transistor were also monitored during the simulation, and the results showed good agreement with the calculation using the new transistor model.

The performances of the op amps were also simulated in a unity-gain follower configuration. By applying 1 kHz and 100 kHz 1 V_{P-P} sine wave respectively, the THD of the amplifiers were measured. To check the stability and speed of the circuits, various step inputs (10 mV, 100 mV and 800 mV) were applied to the op amps. The 0.2% settling times were measured for the 10 mV and 100 mV signals. Simulation results are summarized and compared in Table II. It is shown that the amplifiers satisfy all specifications.

For a complete evaluation, we compare the op amps in several key aspects such as design complexity, power consumption, performance and area. The power consumptions of the two amplifiers in moderate inversion are quite close to each other. The four-stage low power amplifier has a better overall performance than the three-stage one, but design of the latter one will encounter less complexity with one less parameter to handle. The phase margin of the three-stage amplifier can further be improved by increasing the transconductance of the second stage. This improvement is limited by the parasitic capacitance and will dissipate more power. Compared to the reference amplifier, the amplifiers designed in moderate inversion consume 1/3 power while the major performances are retained or improved.

6. CONCLUSIONS

By using a new MOSFET transistor model, NGCC amplifiers can be designed in moderate inversion region yielding optimal trade-off design. Simulation results showed high accuracy of this model on calculation of the dimensions and transconductance of transistors. With the same or better performance, the power consumption of the low power amplifiers was reduced by over 65% compared to strong inversion design. Based on overall comparison of the two low power amplifiers, the four-stage low power op amp has better performance while the dissipated power is slightly larger than three-stage one. The advantage of the three-stage op amp is the reduction of design complexity, but the active area increases since longer transistors are required for high dc gain. It seems that the optimal design for reduction on area and power while satisfying the specifications is the four-stage amplifier operating in moderate inversion.

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