AN AMPLIFIER DESIGN METHODOLOGY DERIVED FROM A MOSFET CURRENT-BASED MODEL

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ABSTRACT

This paper presents a design methodology for MOS amplifiers based on a universal model of the MOSFET, valid from weak to strong inversion. A set of very simple expressions allows quick design by hand as well as an evaluation of the design in terms of power consumption and silicon real estate. The design and integration of a common-source amplifier illustrate the appropriateness of the proposed methodology.

1. INTRODUCTION

The design of CMOS amplifiers is based on MOSFET models developed for either weak inversion or strong inversion [1,2]. However, the current trend towards low-power often requires the transistor to be biased in the moderate inversion region. Therefore, a MOSFET model capable of providing the designer with a set of equations valid for any inversion level is a very powerful tool. Indeed, a good MOSFET model for all regions of operation allows the designer to choose an initial solution which is very close to the desired one. Here we use the universal MOSFET model developed in [3], which employs the bias current as the key variable, as a basic guideline to design amplifiers. The design methodology proposed here accounts for specifications of gain-bandwidth product, DC gain and voltage swing. It allows the designer to choose the bias current and transistor dimensions from closed expressions. The design approach proposed here can be applied to the design of common-source amplifiers as well as to more complex topologies such as differential and operational amplifiers.

2. MOSFET MODEL

The following set of equations developed in [3] can be readily used for the design of MOSFETs operating in saturation:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_d}} \tag{1.a}$$

$$i_d = \frac{I_D}{I_S} \tag{1.b}$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \tag{1.c}$$

$$f_T \cong \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_d}-1\right) \tag{2}$$

$$\frac{V_{DSsat}}{\phi_t} \cong \left(\sqrt{1+i_d}-1\right)+4 \tag{3}$$

(1.a) is a universal relationship for MOSFETs, independent of technology, dimensions and temperature. I_S, the normalization current, depends on the aspect ratio and technological parameters: mobility μ, oxide capacitance per unit area C'_{ox} and the thermal voltage ϕ_t. n, the slope factor, is slightly greater than one [3]. i_d is the normalized drain current or inversion level [3,4] for transistors operating in saturation. The transconductance-to-current ratio of MOSFETs (Fig. 1) is given by (1.a) while $\phi_t g_m/I_C=1$ for bipolar transistors. If g_m is defined in a bipolar design, so is I_C. However, in a MOSFET design, the specification of g_m allows the designer to choose from a range of currents, according to (1.a). Equation (2) is an approximation for the intrinsic cut-off frequency f_T in

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terms of i_d. An approximate formula for the source-to-drain saturation voltage as a function of the inversion level is shown in (3). (1) to (3) constitute a set of fundamental expressions to design MOS amplifiers for any inversion level.

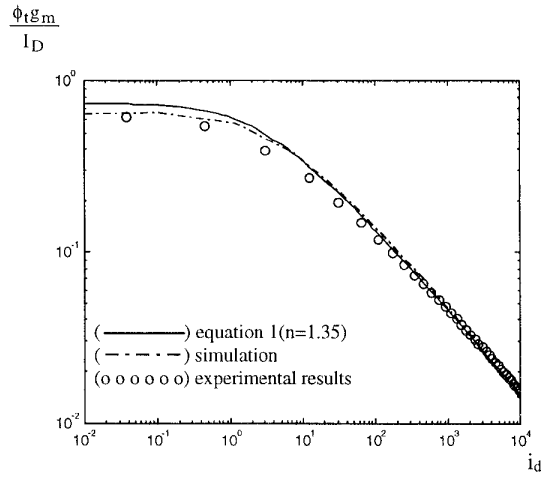

Figure 1. Transconductance-to-current ratio of a MOSFET vs inversion level.

3. COMMON-SOURCE AMPLIFIER

The methodology presented in [5] to design amplifiers is based on either calculated [4] or measured curves of g_m/I_D in MOSFETs. The approach proposed in our paper is based on a universal g_m/I_D ratio, valid for any technology. Moreover, closed expressions for the bias current, the aspect ratio, the saturation voltage as well as the intrinsic cut-off frequency are also provided. The only technology-dependent parameter used in our methodology is I_S, the normalization current.

In the ideal common-source amplifier in Fig. 2, the transconductance required to achieve a gain-bandwidth product (GBW) for a load capacitance equal to CL is $g_m=2\pi\cdot GBW\cdot CL$. Using this equation together with (1) allows writing the drain current and the aspect ratio as:

$$I_D = 2\pi\cdot GBW\cdot CL\cdot n\cdot\phi_t\frac{1+\sqrt{1+i_d}}{2} \tag{4}$$

$$\frac{W}{L} = \frac{2\pi\cdot GBW\cdot CL}{\mu C'_{ox}\phi_t}\left(\frac{1}{\sqrt{1+i_d}-1}\right) \tag{5}$$

(4) and (5) show that an infinite set of solutions is available to meet the required GBW. Fig. 3 shows plots of the bias current in (4) and the aspect ratio in (5) as functions of i_d. Both curves have been normalized to $i_d=8$. A trade-off between area and power consumption can be reached by an appropriate choice of i_d. It is important to note that the power consumption is low but the aspect ratio is high for low inversion levels. Moreover, the lowest current to meet the specified GBW is obtained for weak inversion, when $i_d<1$. i_d close to 1 can be a good choice if low-power is required. On the other hand, a normalized drain current much smaller than 1 leads to a prohibitively high aspect ratio for a negligible reduction in power consumption as compared with the case $i_d\approx 1$.

The following set of equations is used to determine the DC voltage gain A_{vo}:

$$A_{vo} = -\frac{g_m}{g_{ds}} = -\frac{g_m}{I_D}V_A \tag{6.a}$$

$$A_{vo} = -\frac{V_A}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_d}\right)}\right) \tag{6.b}$$

V_A is the Early voltage which, in a first order approximation, is proportional to the transistor channel length.

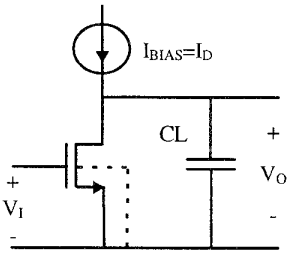

Figure 2. Common-source amplifier.

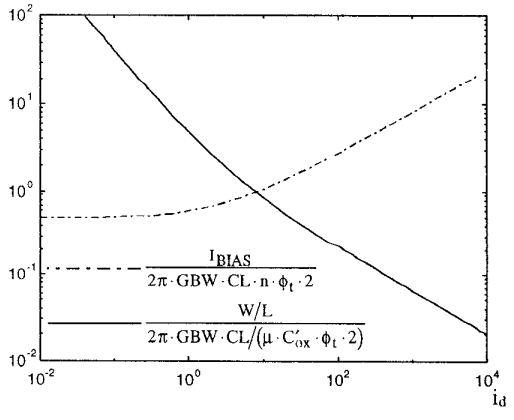

Figure 3. Bias current and aspect-ratio vs inversion coefficient. Both curves are normalized to $i_d=8$.

4. DESIGN METHODOLOGY

Assuming that the gain-bandwidth product and DC gain are the specifications to be met for a given load capacitance, the following design methodology for a common-source amplifier is suggested:

1. For the CL and GBW specified, use expressions (4) and (5) to determine I_D and W/L as functions of the inversion level. Plots of both the bias current and the aspect ratio required to meet the gain-bandwidth product specification are shown in Fig. 3. Choose a value for i_d and, consequently, a pair (I_D, W/L) which satisfies the design requirements as regards power consumption and area;

2. Select the dimensions, W and L, of the input transistors according to the aspect ratio determined in step 1. Verify if the unity gain frequency of the input transistor is consistent with the gain-bandwidth product specified. Typically, f_T should be at least three times higher GBW in order to avoid the parasitic diffusion and overlap capacitances of the NMOSFET to be of the same order of magnitude of the load capacitance. From (2) and (5) one can write:

$$W \cong 2\frac{CL}{LC'_{ox}}\frac{GBW}{f_T} \qquad (7)$$

   The diffusion and overlap capacitances are both proportional to W; therefore, the parasitic capacitance of the NMOSFET drain is proportional to GBW/f_T. If the GBW/f_T ratio is close to 1, the ratio of the parasitic capacitance to the load capacitance can be very large;

3. Verify if the gain specification is satisfied. If not, an increase in channel length and/or a reduction in i_d can be employed to increase the gain;

4. Design the current source. For a low voltage design, the saturation voltage of the current source should be as small as possible. Therefore, inversion coefficients close to 1 can be used in order to achieve a good compromise between area and saturation voltage.

5. SIMULATION RESULTS

The design methodology is illustrated by a common-source amplifier whose specifications are GBW=10MHz, CL=10pF and $A_{vo}\geq$40dB. The technological parameters are $\mu_N \cdot C'_{ox} = 107\mu A/V^2$, n is supposed to be 1.3 and ϕ_t=26mV. L=5μm is chosen for the specified gain. Table I illustrates the results obtained from hand design. W/L and I_{BIAS} are calculated from (4) and (5). The simulated gain-bandwidth products have been obtained by using the EKV model from SMASH simulator [6], using W/L ratio and I_{BIAS} calculated from (4) and (5). The simulations show that, for low inversion levels, W/L is large and, consequently, the parasitic capacitance in parallel with CL can be large. As a consequence the gain-bandwidth product is much lower than the one expected from hand calculation. Therefore, in order to obtain the desired GBW, the bias current has to be correspondingly increased.

6. EXPERIMENTAL RESULTS

A common-source amplifier has been integrated in the 1μm CMOS process from ES2. Composite transistors [7], series/parallel combinations of single transistors, have been employed as both the driver transistor and the current source. The "equivalent channel length" [7] of the driver is L=4μm and the normalization current I_S=62.5μA. The gain-bandwidth product, GBW, as well as the DC gain, A_{vo}, have been measured for several current levels, as shown in Table II. The differences between experimental and simulated results of the DC gain can be attributed to three factors: the finite output impedance of the current source, the shorter channel length of the driver and improper modeling of the transistor output conductance. The measured gain-bandwidth product is smaller than the simulated one owing to the parasitic capacitances of both the current source and the measurement setup as well as deviations from the nominal process parameters. Anyway, the simulated and experimental results do not differ very much and, consequently, the design methodology presented here can be used for a first order calculation of the bias current and transistor aspect ratio for any inversion level. Fig. 4 illustrates the experimental frequency response of the common-source amplifier for i_d=30.

7. CONCLUSIONS

A methodology to design MOS amplifiers has been developed. It is supported by a current-based MOSFET model which has accurate and continuous equations from weak inversion to strong inversion. The design approach is suitable for both low power design or for area optimization. The proposed methodology has been applied to the design of a common-source amplifier and corroborated by simulation and experimental results.

ACKNOWLEDGMENTS

The authors would like to thank the financial support of CNPq and CAPES, from the Brazilian Ministeries of Science and Technology and Education. They also acknowledge the assistance of Mr. Ricardo Takase Gonçalves in the circuit design and layout.

Table I. Common-source amplifier - hand design and simulation. The nominal specifications are GBW=10MHz, CL=10pF and $A_{vo} \geq 40dB$.

Design				Simulation (L=5μm)	
i_d	$\frac{I_{BIAS}}{CL}$ (μA/pF)	$\frac{W}{L}/CL$ (1/pF)	$\frac{f_T}{GBW}$	GBW (Hz)	A_{vo} (dB)
1	2.6	54.5	0.64	7.7M	60
3	3.2	22.6	1.5	8.6M	59
10	4.6	9.7	3.6	9.0M	57
30	7.0	5.0	7.0	9.2M	55
100	11.7	2.5	14.0	9.2M	52
300	19.5	1.4	25.0	10.0M	47

Table II. Common-source amplifier-experimental results.

Measurements			
i_d	$\frac{I_{BIAS}}{CL}$ (μA/pF)	GBW (Hz)	A_{vo} (dB)
1	2.7	4M	41
3	3.2	6M	40
10	4.7	7M	39
30	7.0	7.5M	37
100	11.8	7.5M	34
300	19.7	6M	29

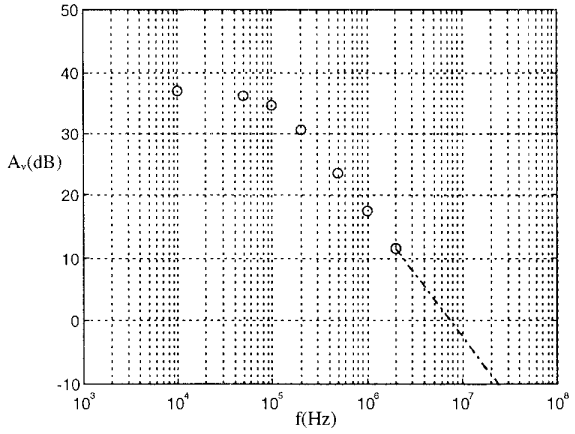

Figure 4. Common-source amplifier frequency response for id=30.

(o o o o o) experimental results
(– · – · –) extrapolation (20dB/dec)

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