DISTORTION ANALYSIS OF MOSFETS

FOR APPLICATION IN MOSFET-C CIRCUITS

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ABSTRACT

The aim of this paper is to provide some guidelines on the design of MOS V-I converters. An explicit formula for the harmonic distortion based on an analytic model of the MOSFET has been derived for any inversion level. Experimental results for the distortion in the MOSFET V-I characteristics as well as biasing and tuning strategies applied to MOSFET-C filters are presented.

1. INTRODUCTION

Integrated active RC filters use the MOSFET in nonsaturation as a tunable element [1,2] in order to cope with component tolerances. MOS transistors are inherently nonlinear resistors whose I-V characteristics depend on bias voltages. Some papers [3,4] in the technical literature provide results for the harmonic distortion of MOSFETs operating in strong inversion. However, as pointed out in [5], some of the results available to calculate distortion must be revised for low voltage applications since they have been derived for operation of the MOSFET in strong inversion.

The purpose of this work is to provide an analysis of the harmonic distortion of the drain current in long-channel MOSFETs, valid for any inversion level [7]. In Section II we review the MOSFET model from references [6,7] which supports the equations derived here. Section III presents theoretical and experimental results for the harmonic distortion of the drain current. In Section IV we show a MOSFET voltage divider appropriate to bias low-voltage V-I converters. The conclusions are summarized in Section V.

2. MOSFET MODELING

In low voltage applications one needs a MOSFET model valid in all regions of operation: weak, moderate and strong inversion. The MOSFET model presented in [6,7], based on the linearization of the inversion charge density Q_I' with respect to the surface potential ϕ_S, has been proved to be accurate enough for any operating region. The model in [6,7] allows writing the drain current in terms of the inversion charge densities Q_{IS}' and Q_{ID}' at the source and drain ends of the channel as:

$$I_D = I_F - I_R \tag{1.a}$$

$$I_{F(R)} = \frac{\mu W}{C_{ox}' L}\left(\frac{Q_{IS(D)}'^{\,2}}{2n} - C_{ox}'\phi_t Q_{IS(D)}'\right) \tag{1.b}$$

μ is the mobility, ϕ_t the thermal voltage, C_{ox}' the oxide capacitance per unit area and W/L the aspect ratio. n is the slope factor (usually between 1 and 2), slightly dependent on the gate voltage.

In (1.a) the drain current has been decomposed into a forward current I_F and a reverse current I_R [7, 8]. $I_F(I_R)$ depends only on the source(drain)-to-bulk and gate-to-bulk voltages for a long channel device. In saturation, $I_F >> I_R$ and $I_D \cong I_F$ is independent of the drain voltage as shown in Fig. 1.

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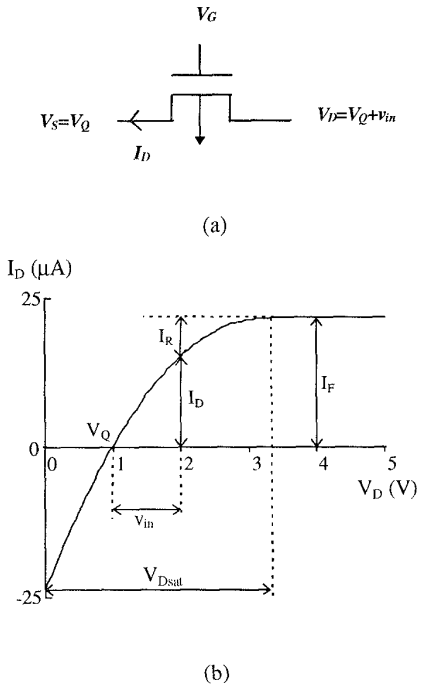

Figure 1. (a)MOSFET symbol and applied voltages; (b)Output characteristic for V_Q=1V, V_G=4.5V.

Combining (1.b) and the definition of the source(drain)-transconductance [6,8]

$$g_{ms(d)} = -(+)\frac{\partial I_D}{\partial V_{S(D)}} = -\mu Q'_{IS(D)}\frac{W}{L} \tag{2.a}$$

allows writing:

$$\frac{I_{F(R)}}{\phi_t g_{ms(d)}} = \frac{1+\sqrt{1+i_{f(r)}}}{2} \tag{2.b}$$

The variable $i_{f(r)} = I_{F(R)}/I_S$ is the normalized forward (reverse) current or inversion coefficient [7,8] at source (drain). The normalization current is given by

$$I_S = \mu\frac{W}{L}nC'_{ox}\frac{\phi_t^2}{2} \tag{2.c}$$

If $i_f << 1$ (weak inversion), the right-hand side of (2.b) is equal to 1. On the other hand, $i_f >> 1$ corresponds to the strong inversion regime. Eqn. (2.b), a universal characteristic of MOSFETs, has been experimentally verified for different technologies, geometries and gate voltages. Fig. 2 shows the plots of the current-to-transconductance ratio for different technologies.

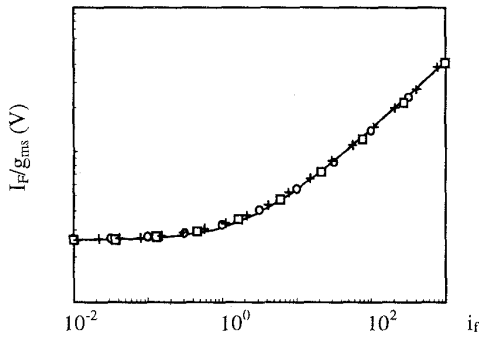

Figure 2. Measured I_D/g_{ms} ratio for transistors from different technologies at V_G=2V:
o t_{ox}=280 Å (I_S=26 nA) + t_{ox}=490 Å (I_S=32 nA)
t_{ox}=55 Å (I_S=110 nA) —— eqn. (2.b)

3. DISTORTION AND DRAIN CURRENT

Let us now compute the distortion in the I-V characteristic of the MOSFET shown in Fig. 1, where all the voltages are referred to the substrate. According to the model in the previous section, I_F is constant if V_S and V_G are held constant. The normalized drain current can be written as:

$$i_d = \frac{I_D}{I_S} = i_f - i_r = \sum_{j=1}^{\infty} k_j v_{in}^j \tag{3.a}$$

$$\text{with} \qquad k_j = -\frac{1}{j!}\frac{d^j i_r}{dv_{in}^j}\bigg|_{i_r = i_f} \tag{3.b}$$

The coefficients in (3.b) can be readily calculated from (2.b):

$$k_1 = -\frac{2}{\phi_t}\left(\sqrt{1+i_f}-1\right); \tag{3.c1}$$

$$k_2 = \frac{1}{\phi_t^2}\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_f}}; \tag{3.c2}$$

$$k_3 = -\frac{1}{3\phi_t^3}\frac{\sqrt{1+i_f}-1}{\sqrt{(1+i_f)^3}}; \tag{3.c3}$$

Therefore, if the input voltage is $v_{in}=V_M \sin\omega t$, the second and third order harmonic distortion are given by

$$HD2 \equiv \frac{k_2}{2k_1} = \frac{1}{4\sqrt{1+i_f}}\frac{V_M}{\phi_t} \tag{3.d1}$$

$$HD3 \cong \frac{k_3}{4k_1} = \frac{1}{24\sqrt{(1+i_f)^3}}\left(\frac{V_M}{\phi_t}\right)^2 \qquad (3.d2)$$

The harmonic distortion is thus computed from (3.d) in terms of the normalized saturation current (i_f). The results of the second and third-order harmonic distortion are shown in Figs. 3 and 4 for different gate (V_G) and common-mode (V_Q) voltages.

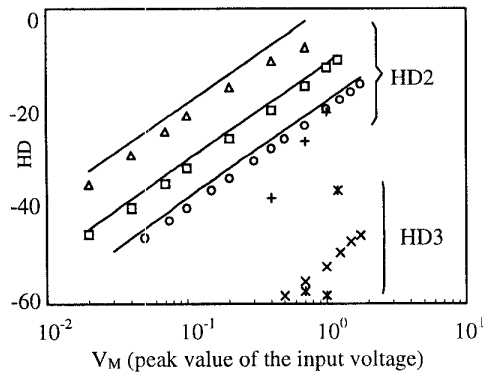

Figure 3. Measured and theoretical harmonic distortion of a transistor, W/L=18μm/5μm, from a 2μm technology:
Δ + V_G=1.2V V_Q=0.1V (i_f=80)
* V_G=2.5V V_Q=0.4V (i_f=1200)
o x V_G=5V V_Q=1.1V (i_f=7200)
——— eqn (3.d1)
V_Q is equal to the voltage in node B of the bias circuit in Fig. 6

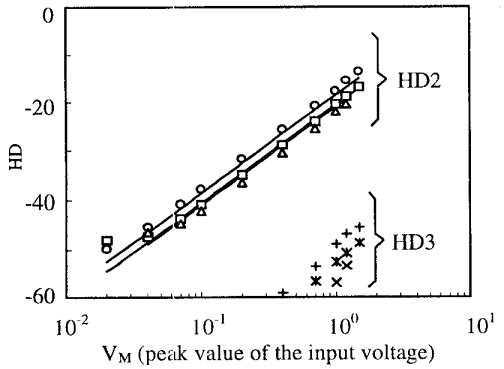

Figure 4. Measured harmonic distortion of a transistor, *W/L*=18μm/5μm, from a 2μm technology, V_G=5V:
o x V_Q=1.9V (i_f=6600)
* V_Q=1.1V (i_f=10500)
Δ + V_Q=0.5V (i_f=11500)
——— eqn (3.d1)

The dominant deviation from linearity comes from the second order term. The theoretical second order distortion fits very well to the experimental results. However, the error that results to calculate HD3 from (3.d2) is very large. *HD3* increases dramatically when the drain voltage approaches the saturation voltage. In fact, the analytic determination of third and higher order terms would need an I-V MOSFET model precise up to the third order derivative. Non-uniform substrate doping and short-channel effects make it difficult to obtain such a precise model. Theoretically, the even order terms of the harmonic distortion are canceled out in fully balanced structures [1,2], as the one shown in Fig. 5. However, in practical cases, the even-order harmonic distortion is generally higher than the odd-order harmonic distortion owing to op amp offsets, transistor mismatching and unbalanced input signals [3].

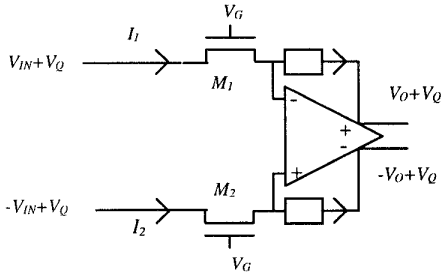

Figure 5. 2-transistor MOS V-I converter

4. BIAS AND TUNING

For a proper operation of the V-I converter, the bias voltage V_Q in Fig. 5 should be a fraction of the MOSFET saturation voltage. V_Q has been obtained from the bias network shown in Fig. 6. In any of the intermediate nodes in Fig. 6, the voltage is a fraction of the saturation voltage. The values of V_Q= 1.9, 1.1 and 0.5V in Fig. 4 are the node voltages at A, B and C, respectively, in Fig. 6.

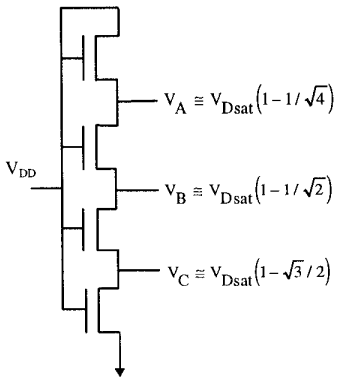

Figure 6. Series association of identical MOS transistors to form the bias network [9]

Usually, the tuning of the MOS transconductance in Fig. 5 is performed by controlling the gate voltage. This tuning methodology changes the transistor quiescent point. A direct consequence of a reduction in the DC gate voltage is an increase in the harmonic distortion of the current, as shown in Fig. 3. Therefore, the harmonic distortion can be minimized if the gate voltage is kept at its maximum value. In the proposal of [9] M1 and M2 in Fig. 5 are replaced by two matched MOSFET-only current dividers (MOCD) [9,10] programmed with two equal input words. The MOCD performs as an MOS transconductor whose gate voltage is V_{DD} and whose transconductance is controlled by a digital word.

5. CONCLUSIONS

We presented expressions and results for the harmonic distortion of the MOSFET drain current in terms of the normalized saturation current, for any current level. The MOSFET bias voltage for application in a V-I converter is obtained from the intermediate node of a series association of transistors. Therefore, the quiescent voltage is equal to some fraction of the transistor saturation voltage. The use of digitally programmable MOSFET-only current attenuators (MOCD) in MOSFET-C filters has been found to be the best tuning solution in terms of harmonic distortion because it does not require changes in the gate voltage, thus avoiding degradation in the linearity of the filter.

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REFERENCES

[1] Banu M., Tsividis Y., "Fully integrated active RC filters in MOS technology", *IEEE Journal of Solid State Circuits*, Dec, 1983, vol. 18, no.6, pages 644-651.

[2] Czarnul Z., "Modification of Banu-Tsividis continuous-time integrator structure", *IEEE Transactions on. Circuits and Systems*, Jul, 1985, vol. 33, no. 7, pages 714-716.

[3] Banu M. and Tsividis Y., "Detailed analysis of nonidealities in MOS fully integrated active RC filters based on balanced networks", *IEE Proceedings*, Oct, 1984, vol. 131, part G, no. 5, pages 190-196.

[4] Groenewold G. and Lubbers W. J., "Systematic distortion analysis for MOSFET-C integrators with use of a new MOSFET model", *IEEE Transactions on Circuits and Systems - II*, Sep, 1994, vol. 41, no. 9, pages. 569-580.

[5] Flandre D. and Jespers P., "Charge-sheet modelling of MOS I-V fundamental nonlinearities in MOSFET-C continuous-time filters", *Electronic Lett*ers, Aug, 1995, vol. 31, no. 17, pages 1419-1420.

[6] Cunha A.I.A, Schneider M.C. and Galup-Montoro C., "An explicit physical model for the long-channel MOS transistor including small-signal parameters", *Solid-State Electronics*, Nov, 1995, vol. 38, no.11, pages 1945-1952.

[7] Cunha A.I.A, Gouveia-Filho O. C., Schneider M.C. and Galup-Montoro C., "A current-based model for the MOS transistor", *Proceedings of the International. Symposium on Circuits and Syst*ems, Hong-Kong, Jun, 1997, pages 1608-1611.

[8] Enz C.C, Krummenacher F. and Vittoz E.A., "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", *Analog Inegrated. Circuits. and Signal Processing*, Aug., 1995, pages 83-114.

[9] Schneider M. C., Galup-Montoro C. and Noceti Filho S., "A digitally programmable V-I converter for application in MOSFET-C filters", *Electronic Letters*, Aug, 1995 vol 31, no. 18, pages 1526-1527.

[10] Bult K. and Geelen G. J. G. M., "An inherently linear and compact MOST-only current division technique", *IEEE Journal of Solid State Circuits*, Dec, 1992, vol. 27, no 12, pages 1730-1735.