Design Guidelines for CMOS Current Steering Logic

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ABSTRACT

Closed-form expressions for static and dynamic parameters have been derived for the Current Steering Logic (CSL) inverter. Measurements and simulation results that validate these expressions are presented for a 2.5V power supply. Design guidelines are given for the application of CSL gates in low voltage, low power mixed analog/digital circuits.

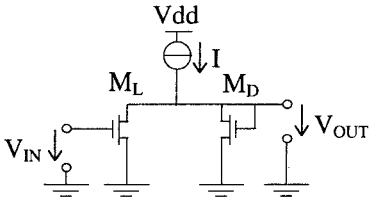

Fig. 1 :CSL Inverter

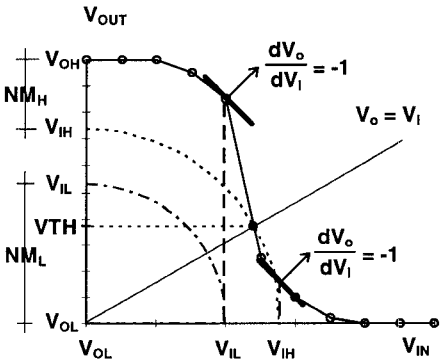

Fig. 2 : Inverter voltage transfer curve and definitions of DC parameters.

I. INTRODUCTION

Current spikes generated by logic gates cause voltage variation in the supply lines. In mixed-mode (analog/digital) circuits, the pervasive effect of this noise is coupled into the sensitive analog circuitry, degrading its performance [1,2]. Moreover, this transient noise may cause errors in purely digital circuits.

Circuit techniques [3] have been proposed recently in order to complement the static logic and reduce the digital switching noise.

Current steering logic has proven to be a very suitable technique as far as high performance, low power and low voltage are concerned [4,5]. However, to exploit the whole potential of this technique, models that allow designers to gain an insight into the static and dynamic characteristics of the gates are necessary.

This work presents a set of expressions, based on the EKV MOSFET model [6], to calculate the most important DC and AC parameters of CSL gates. Measurements and simulated results, that validate the analytical expressions, are shown. Finally, some guidelines for application of this logic in low power, low voltage mixed-mode circuits are given.

II. STATIC ANALYSIS OF THE CSL INVERTER

In the CSL inverter of Fig. 1, the current I is shared between the logic device M_L and the diode connected device M_D. The gate DC parameters, defined in Fig. 2, can be computed from Table I [5] . They depend on **Gv**, which is equal to the ratio $(W/L)_L/(W/L)_D$. The values of β_L and β_D for the inverter can be chosen according to some trade-off between area and noise margin, as will be shown in Section V.

Output high logic level $V_{OH} - Vt = \sqrt{\frac{2 \cdot n \cdot I \cdot Gv}{\beta_L}}$	Gate threshold voltage $VTH = Vt + \left(\frac{V_{OH} - Vt}{\sqrt{1+Gv}}\right)$
Output low logic level $V_{OL} = \frac{(V_{OH} - Vt)}{n} \cdot \left(1 - \sqrt{1 - Gv^{-1}}\right)$	
Input high logic level $V_{IH} = (V_{OH} - Vt) \cdot \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{Gv^{-1}} + Vt$	
Input low logic level $V_{IL} = (V_{OH} - Vt) \cdot \sqrt{\frac{1}{Gv \cdot n^2 + 1}} \cdot \sqrt{Gv^{-1}} + Vt$	
High Noise Margin $NM_H = V_{OH} - V_{IH}$	Low Noise Margin $NM_L = V_{IL} - V_{OL}$

Table I : DC Characteristics of the CSL inverter.

In Table I, Vt is the transistor threshold voltage, $\beta = \mu \cdot C_{OX} \cdot (W/L)$ and n is the slope factor, usually between 1 and 2, slightly dependent on the gate voltage [6].

III. DYNAMIC ANALYSIS OF THE CSL INVERTER

The fall (rise) propagation time has been defined here as the time required for the output to go from V_{OH} (V_{OL}) to the logic threshold VTH, after an input step has been applied to the gate. We have denoted these propagation times as τ_F and τ_R, respectively. The overall delay has been defined as $(\tau_F+\tau_R)/2$.

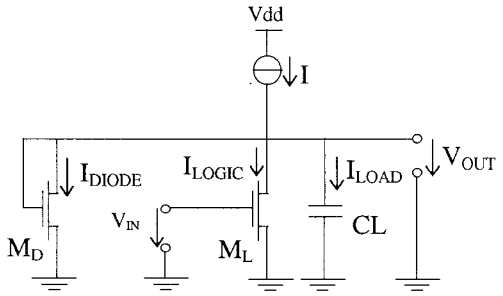

Fig. 3: Scheme to derive the rise and fall propagation times

Fig. 3 shows the equivalent circuit used to derive the inverter dynamic characteristics. The EKV MOSFET model in strong inversion yields expressions (1) and (2) for τ_F and τ_R.

$$\tau_F = A \cdot B \tag{1}$$

$$\tau_R = C + D \tag{2}$$

$$A = -\frac{\frac{2 \cdot n \cdot CL}{\beta_D}}{\sqrt{\frac{2 \cdot n \cdot I}{\beta_D}} \cdot \sqrt{Gv - 1}} \tag{3}$$

$$B = \left\{ arctg\left[\frac{1}{\sqrt{1+Gv} \cdot \sqrt{Gv-1}}\right] - arctg\left[\frac{1}{\sqrt{Gv-1}}\right] \right\} \tag{4}$$

$$C = \frac{CL}{I} \cdot (Vt - V_{OL}) \tag{5}$$

$$D = \frac{n \cdot CL}{\beta_D \cdot \sqrt{\frac{2 \cdot n \cdot I}{\beta_D}}} \cdot \ln\left(\frac{\left(1 - \frac{1}{\sqrt{1+Gv}}\right)}{1 + \frac{1}{\sqrt{1+Gv}}} \right) \tag{6}$$

The current generated by the CSL inverter in the Vdd supply line is ideally constant. However, the parasitic capacitances of the PMOS transistors used as current sources connect the output node to the Vdd line. This capacitive coupling is responsible for the resultant digital switching noise in CSL gates.

Fig. 4 shows the equivalent circuit used to analyse the current spikes. The load capacitance has been split into C_{CS} and C_{EQ}. C_{CS} is the drain-to-bulk capacitance of the PMOS transistor. C_{EQ} represents the fan-out of the inverter as well as the capacitances of M_L and M_D connected between output and ground.

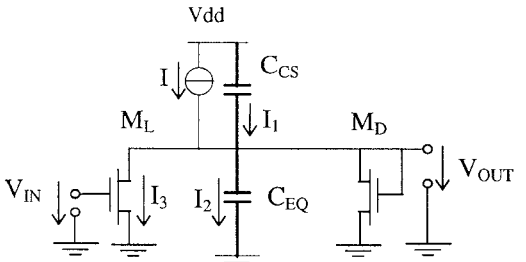

Fig. 4: Equivalent circuit to analyse the current spikes on the power supply line.

The current spikes I'_{MAX} and I''_{MAX} are calculated for rising and falling input steps, respectively. Assuming the current I_1 in the circuit of Fig. 4 is the main component of the current spike, the expressions for I'_{MAX} and I''_{MAX} are given by :

$$\left|\frac{I'_{MAX}}{I}\right| = \frac{C_{CS}}{C_{EQ} + C_{CS}} \cdot [Gv - 1] \tag{7}$$

$$\left|\frac{I''_{MAX}}{I}\right| = \frac{C_{CS}}{C_{EQ} + C_{CS}} \tag{8}$$

IV. RESULTS

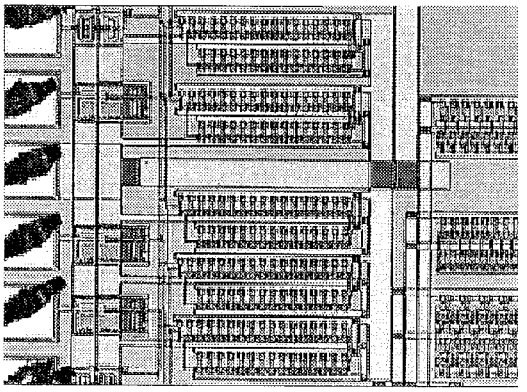

Fig. 5 : Microphotograph of the fabricated chip - Integrated ring oscillators.

To validate the theoretical results CSL inverters, and ring oscillators (RO's) with different Gv's were integrated. Fig. 5 shows the microphotograph of the ring oscilators.

Table II provides information about the CSL inverters. Simulation results have been obtained using the EKV MOSFET in ANACAD/ELDO simulator. The technology is a 0.7µm CMOS from EUROCHIP ATMEL-ES2. Theoretical results were calculated from previous equations with the same set of parameters used for simulations .

Fig. 6 illustrates curves of logic levels in terms of Gv. The correlation between measured, theoretical and simulated figures validates the expressions of Table I.

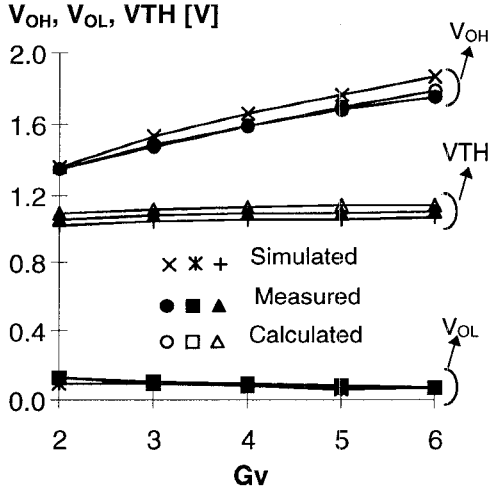

Fig. 6: Measured, simulated and calculated logic levels for the CSL inverter.

Fig. 7 shows the experimental and simulated delays obtained from the ring oscillators. The experimental results fit very well to the simulations.

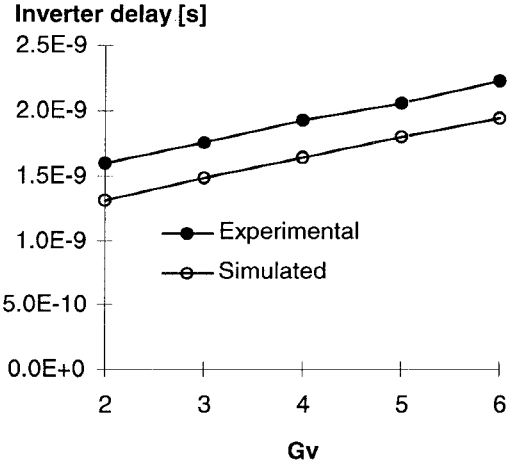

Fig. 7: Experimental and simulated delay times in terms of Gv (characterised from ring oscillators).

Fig. 8 shows the theoretical and simulated delays times computed assuming an input step. The results are closed to each other. The difference between the calculated and experimental delays is mainly caused by the approximation of the input by a step function in order to compute the theoretical delays. Moreover, the difficulty to evaluate parameters such as capacitances and slope factor (n) also contributes to generate errors. Nevertheless, analytical expressions (1) to (6) are very useful because they show the most important parameters that contributes to the inverter delay.

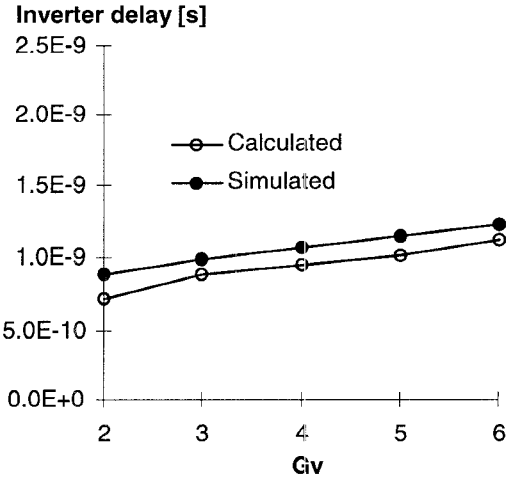

Fig. 8: Calculated and simulated delay times in terms of Gv (step input).

Fig. 9 displays the current spikes generated during rising and falling transitions of the output signal. Simulated and theoretical results present identical behaviours.

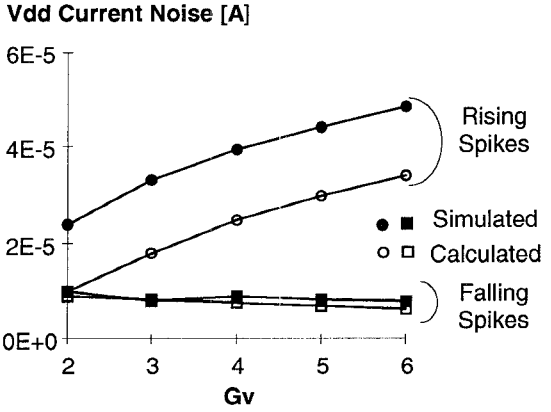

Fig. 9: Simulated and calculated current spikes as a function of Gv.

Gv	$W/L\|_L$	$W/L\|_D$	$W/L\|_{PMOS}$
2	2.5/1	2.5/2	8/1
3	2.5/1	2.5/3	8/1
4	2.5/1	2.5/4	8/1
5	2.5/1	2.5/5	8/1
6	2.5/1	2.5/6	8/1

Table II : Design parameters for the inverters.

For the ten samples used, the measured characteristics were very closed to each other, demonstrating a reasonable matching between gates.

V . DESIGN GUIDELINES FOR THE CSL INVERTER

To reach an efficient design of the CSL inverter, we suggest the following steps :

- Step 1: Choose the bias current I considering the best power/speed trade-off for the application.
- Step 2: Choose an adequate noise margin (NM_H, NM_L);
- Step 3 : Choose β_L as a minimum feature size allowed by the technology;
- Step 4: From the equation set of Table I, find the Gv required to meet the specified noise margin for the selected bias current;
- Step 5: Choose a saturation voltage Vsat for the PMOS transistor, such that $Vdd \geq V_{OH} + Vsat$;
- Step 6: Find β for the PMOS transistor based on the Vsat value calculated above.

The choice of an appropriate noise margin for a particular logic is not an easy task because it depends on many factors such as architecture of the logic block and surrounding generated noise. In the example given below, we have adopted a noise margin of 300mV. It is an acceptable value for many applications [3,7]. In order to illustrate the design methodology we have chosen a power consumption of 50µW/gate at 2.5V.

Step 1 : 20µA
Step 2 : 300mV of noise margin;
Step 3 : W_L/L_L = 2.5µm/1µm;
Step 4 : Gv=3;
Step 5 : Vsat ≈ 0.16V;
Step 6 : W/L=8µm /1µm for the PMOS transistor.

The total current consumption of the CSL circuits is easily estimated by adding the bias current of all gates. Low saturation voltages are especially important for low supply voltages. The saturation voltage of the PMOS transistor is low if its aspect ratio is large. However, the MOSFET drain-to-bulk capacitance is proportional to its width, thus increasing current spikes. Therefore, the reduction of the saturation voltage through the increase of the transistor channel width affects adversely the current spikes.
Reducing the capacitance C_{CS} is an efficient way to reduce the current spikes. The drain-to-bulk capacitance of the MOSFET can be diminished by using closed MOSFETs in which the source surrounds the drain.

VI . CONCLUSIONS

This work has presented expressions for the static and dynamic behaviour of the CSL inverter. The accuracy of these expressions have been confirmed by measurements and simulations. The main design parameters of a CSL gate are the bias current and Gv (relation between the aspect ratios β_L and β_D). Guidelines to design CSL gates have been described.

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