

# DIGITAL CIRCUIT TECHNIQUES FOR MIXED ANALOG/DIGITAL CIRCUITS APPLICATIONS

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## ABSTRACT

This paper presents a detailed analysis of CSL (Current Steering Logic) [1] and compares its characteristics with FSCL (Folded Source Coupled Logic) [1,2,3], two logic families intended to be applied in mixed-mode CMOS circuits. These logic families generate small current spikes compared to the CMOS static family. They feature high robustness to process fluctuations, and are capable to operate at low quiescent current and power supply voltage. Simulation results, based on ES2 0.7 CMOS low voltage technology, are presented.

## I. INTRODUCTION

Low voltage mixed-mode ICs follow the new trends in technology and modern design methodologies. In this context, the *CMOS static logic* has been widely employed because of its simple design, high packing densities, wide noise margins and high operating frequencies. However, the digital noise generated by the large current spikes during the logic transitions can be coupled into the critical analog portion of the circuit, reducing the target accuracy [4]. Several methods such as shielding, separation of digital and analog power supply lines have been employed to reduce the effects of digital switching noise [2,5]. In fact, logic families that generate a low amount of switching noise are needed. Recently CSL [1], a single ended logic family and FSCL [1,2,3], a fully-differential logic family, were proposed. The main advantage of these logic families is the reduced amount of switching noise generated.

This paper analyses both the CSL and FSCL techniques, intended to be applied in low voltage/low power applications. Section II presents a detailed analysis of the CSL technique; section III reviews the FSCL family; section IV presents a comparison between CSL and FSCL; the conclusions are summarised in section V. All the analysis and simulations are based on the EKV MOSFET model [9] and employ the ES2 CMOS 0.7  $\mu\text{m}$  parameters.

## II. CURRENT-STEERING LOGIC (CSL) FAMILY

In the CSL inverter and NAND gates (Fig. 1-a and c), the current  $I$  is divided between the logic device  $M_L$  and the diode connected device  $M_D$ .

The output voltage levels depend only on NMOS devices, therefore decreasing the sensitivities of the logic levels with respect to process variations. The static characteristics of the CSL inverter are dependent on the ratio  $G_v$ , according to the expressions shown in Table I. For a given bias current  $I$ , the criterion to define  $\beta_L$  and  $\beta_D$  could be a trade-off between area ( $G_v$ ) and noise margin. The design of complex gates follows the same blueprint used on the CSL inverter.

Compared to the static CMOS logic, CSL generates a smaller amount of digital switching noise since the power supply current ( $I$ ) remains constant during output logic transitions. In CSL the current spike on the power supply line is due to the parasitic drain-to-bulk capacitance of the PMOS transistor employed to implement the constant current source. The current spikes in CSL are about a factor of 10 smaller than those generated in the static CMOS logic. Note that CSL is a digital

version of a simple CMOS analog amplifier cell [6].

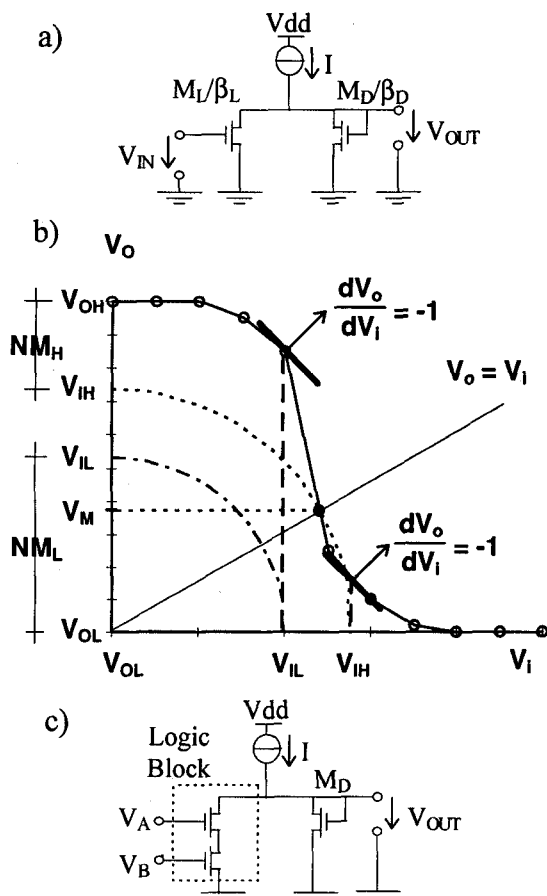


Fig.1 : a) CSL Inverter. b) Inverter voltage transfer curve. c) CSL NAND Gate.

Definition of $G_v$ $G_v = \beta_L/\beta_D$	Output high logic level $V_{OH} - V_t = \sqrt{\frac{2 \cdot n \cdot I}{\beta_D}}$
Output low logic level $V_{OL} = (V_{OH} - V_t) \cdot (1 - \sqrt{1 - G_v^{-1}})$	
Gate threshold voltage $V_M = V_t + \left( \frac{V_{OH} - V_t}{\sqrt{1 + G_v^{-1}}} \right)$	
Input high logic level $V_{IH} = (V_{OH} - V_t) \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{G_v^{-1}} + V_t$	
Input low logic level $V_{IL} = (V_{OH} - V_t) \cdot \sqrt{\frac{1}{G_v^{-1} \cdot n^2 + 1}} \cdot \sqrt{G_v^{-1}} + V_t$	

Table I : DC Characteristics of the CSL inverter.

### III. FOLDED SOURCE COUPLED LOGIC (FSCL) FAMILY

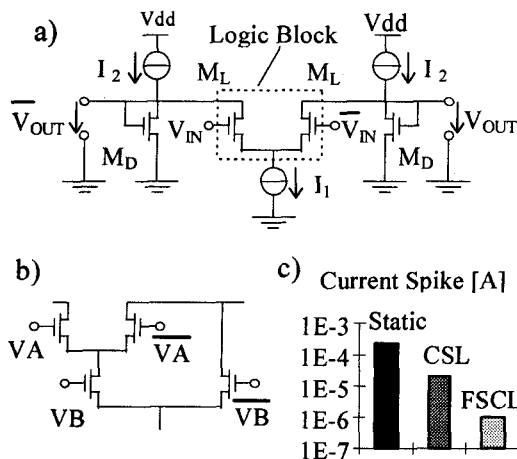


Fig. 2: a) FSCL Inverter. b) AND/NAND logic block. c) Current spike generated by: Static ( $S_N=2.5/1$ ;  $S_P=4 \cdot S_N$ ;  $V_{dd}=2.5V$ ); CSL ( $G_v=3$ ); and FSCL ( $\xi=0.87$ ) logic families.

The description of FSCL can be found elsewhere [2,3,7]. Table II presents the static characteristics of the FSCL inverter in terms of the logic swing ( $\Delta V_L = V_{OH} - V_{OL}$ ) and  $\xi$ .

The current sources (PMOS transistors) have parasitic drain-to-bulk capacitances coupling the output lines to the Vdd line. However due to the small logic swing and the circuit symmetry the resulting current spikes are very small. Typically, current spikes generated in FSCL are two orders of magnitude smaller than those generated in the static CMOS logic (Fig. 2-c).

Definition of $\xi$ $\xi = \frac{I_1}{I_2}$	Logic swing $\Delta V_L = \sqrt{\frac{2 \cdot n \cdot I_2}{\beta_D(\xi)}} \cdot (1 - \sqrt{1 - \xi})$
Output high logic level $V_{OH} = V_t + \frac{\Delta V_L}{1 - \sqrt{1 - \xi}}$	Output low logic level $V_{OL} = V_t + \Delta V_L \cdot \frac{\sqrt{1 - \xi}}{1 - \sqrt{1 - \xi}}$
Gate threshold voltage $V_M = V_t + \frac{\sqrt{1 - \xi}}{1 - \sqrt{1 - \xi}} \cdot \Delta V_L$	

Table II :DC Characteristics of the FSCL inverter.

#### IV. COMPARISON FSCL Vs. CSL

The FSCL inverter characteristics depend on the ratio of two currents, expressed by  $\xi=I_1/I_2$ . When  $\xi$  approaches 1, the matching constraints become more severe. A typical  $\xi$ , found in the literature [3,7], ranges between 0.6 to 0.8. On the other hand, the CSL inverter characteristics depend on a ratio of aspect ratios of NMOS transistors.

CSL	FSCL
Vdd = 2.5 V	Vdd = 2.5 V
Power consumption 50 $\mu$ W	Power consumption 50 $\mu$ W
Logic swing, NM <sub>H</sub> and NM <sub>L</sub> depend on Gv.	$\Delta V_L=0.5V$ ; $NM_H+NM_L=\Delta V_L/2$ .

Table III: Specific conditions of simulation.

The comparison between CSL and FSCL inverters has been made assuming the same Vdd, the same power consumption and noise margins such that  $(NM_H)_{CSL} \geq (NM_H+NM_L)_{FSCL}$  [8] is verified. The dynamic analysis has been performed on an inverter loaded with another inverter. Figures 3 and 4 present simulation results of the dynamic behaviour of the FSCL and CSL inverters. For Gv=3 the inverter noise margins satisfy the design requirements and  $V_{OH}=1.38V$ . The same  $V_{OH}$  is achieved in the FSCL inverter with  $\xi = 0.87$ . The dynamic analysis of the inverters for Gv=3 and  $\xi = 0.87$  shows that the propagation delays are 0.6ns and 2ns for the CSL and FSCL inverters, respectively. Note also that the CSL inverter can operate at a smaller Vdd than the FSCL inverter because the former has a smaller number of transistors between Vdd and ground.

Concerning matching, CSL appears to be less sensitive than FSCL because CSL characteristics depend on a geometric ratio rather than a current ratio. CSL displays a current spike larger than FSCL, but still one order of magnitude smaller than static CMOS logic (Fig. 2). Since CSL is a single ended technique and needs only one current reference, CSL gates have a smaller transistor count and dissipate less power than FSCL gates.

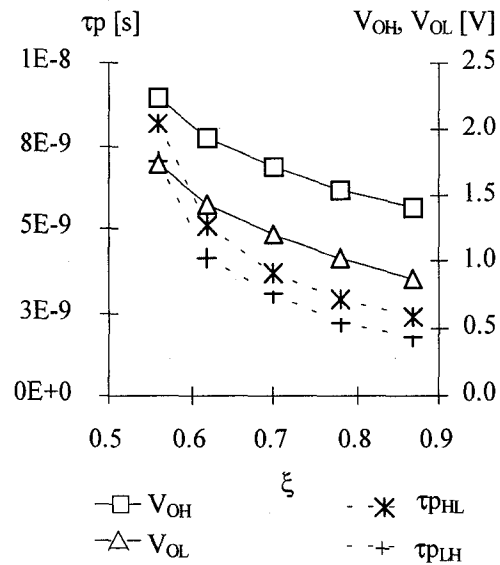


Fig. 3: FSCL inverter- Logic level and Propagation delays Vs.  $\xi$ .

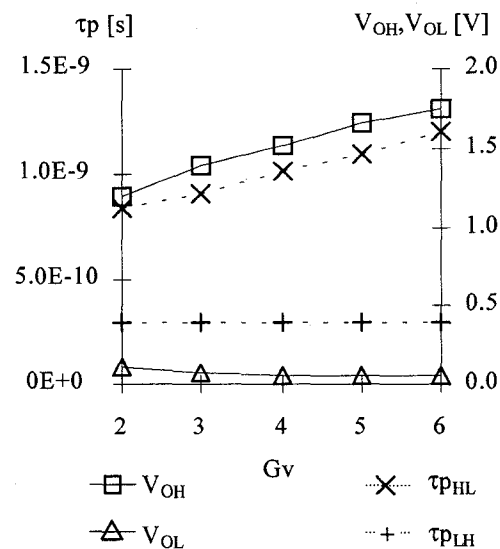


Fig. 4: CSL inverter- Logic level and Propagation delays Vs. Gv.

#### V. CONCLUSIONS

This work presented a detailed analysis and some design guidelines for the CSL and FSCL logic families. CSL presents the following desirable properties: reduced current spikes, high density layout, robustness to process fluctuations and capability to work at low power supply voltages and low bias current. The CSL inverter is faster than the FSCL inverter as long as the power consumption is the same for both. However, current spikes are smaller in FSCL than in CSL.

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