

Digitally programmable switched current filters

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ABSTRACT

A new design technique for switched current filters is presented. The basic element of the filter is a current mirror that employs MOS transistors and an operational amplifier. Programmability of the current mirror is obtained through MOSFET-only current dividers [1]. User programmable analog functions in digital CMOS technology is the main envisaged application for the proposed technique.

1 - INTRODUCTION

Switched capacitors (SC) and switched currents (SI) [2] are the sampled data processing techniques in use nowadays. However, programming both conventional SC or SI filters by digitally selecting different combinations of either capacitors [3] or current mirrors [4] requires a large silicon area. In this paper we show a procedure that employs opamps, MOSFET-only current attenuators [1], switches and gate capacitors to realize SI filters. This method to implement programmable filters takes full advantage of the reduced area, proportional to the number of bits, of programmable MOSFET-only current attenuators.

2 - OPERATION OF THE CURRENT MIRROR

Classically, the simple current mirror shown in Fig. 1(a) (or other topologies derived from it) is employed in analog circuits. In this paper we propose the current mirror shown in Fig. 1(b) for applications in SI filters. Assuming the op amp is ideal, transistors M_1 and M_2 are both biased with the same set of voltages. Therefore, neglecting transistor mismatch, we obtain:

$$i_2 = - \left[\frac{(W/L)_2}{(W/L)_1} \right] i_1 \quad (1)$$

Therefore, the output current i_2 is an inverted replica of the input current i_1 .

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Suppose now that the op amp allows a rail-to-rail output voltage swing. In this case, let us choose V_{BIAS} in order to allow for the highest current swing. As shown in Fig. 2, the MOS transistor does not have a symmetrical behavior for $V_{BIAS} = V_{DD}/2$. Therefore, in order to have equal positive and negative current swings, we have to bias the transistor in such a way that:

$$i_1(v_1 = V_{DD}, V_{BIAS}) = -i_1(v_1 = 0, V_{BIAS}) \quad (2)$$

The circuit in Fig. 3, a series association of two identical transistors, generates a voltage V_{BIAS} at the intermediate node such that eqn. (2) is satisfied [6].

3 - ANALOG ERRORS

3.1 - Op amp finite gain

The finite gain of the op amp of Fig. 1(b) causes an error in the current gain equal to $-1/A$, being A the op amp open loop gain.

3.2 - Op amp finite bandwidth

The bandwidth of the current mirror of Fig. 1(b) is determined by the op-amp gain-bandwidth product provided M_1 and M_2 are not very long.

3.3 - Op amp offset voltage

An offset voltage ΔV_{OS} gives rise to a DC error ΔI_2 in the output current. This error is given by

$$\frac{\Delta I_2}{I_{2 \max}} = 2\sqrt{2} \frac{\Delta V_{OS}}{V_P} \quad (3a)$$

where

$$I_{2 \max} = \frac{\beta_2 n}{4} V_P^2 \quad (3b)$$

V_P is the pinch-off voltage and n the slope factor [5,6].

3.4 - Transistor mismatch

A difference in the transconductance parameters produces a relative gain error proportional to the mismatch in the transconductance parameters. A mismatch in the threshold (pinchoff) voltage causes a

gain error and harmonic distortion, summarized in the following expression:

$$x_2 = \left(1 + \frac{\Delta V_P}{V_P}\right) x_1 + \frac{\Delta V_P}{V_P} \left(\frac{x_1^2}{8} + \frac{x_1^3}{32} + \dots\right) \quad (4)$$

where $\frac{\Delta V_P}{V_P} = \frac{\Delta V_{TO}}{V_{DD} - V_{TO}}$ is the threshold voltage mismatch normalized to the overdrive voltage and $x_1 = i_1/I_{1\max}$, $x_2 = i_2/I_{2\max}$ are the normalized input and output currents.

4 - DIGITALLY PROGRAMMABLE CURRENT MIRROR

In order to provide the current mirror in Fig. 1(b) with digital programmability, MOSFET-only current dividers (MOCD) [1] as shown in Fig. 4 can be used instead of MOS transistors.

The output current of an MOCD is a fraction, selected by a digital word, of the input current. This programmable current divider has two big advantages over other digitally programmable dividers: (i) MOSFET's perform simultaneously as elements of the divider network and as switches and (ii) the impedance of the current attenuator is independent of both the number of bits and of the attenuation factor. Moreover, the high linearity of this current division technique [1] has been proved adequate for analog signal processing.

5 - THE SI MEMORY CELL

Fig. 5 displays the scheme of the proposed switched current mirror. With the switch closed, the hold capacitor is charged to a voltage V , which depends on the value of the input current i_A , the transistor parameters and the gate voltage. The output current is such that $i_B = -\beta i_A$, where β is the scale factor defined in eqn.(1). When the switch opens, a voltage equal to V is held on the memory capacitor and the current is sustained at the output. An important property of the proposed current mirror is that the switches operate at a voltage V_{BIAS} provided by the bias circuit shown in Fig. 3. Therefore, the "conduction gap" of the switches in conventional SC an SI circuits operated at low power supply voltages is avoided [7].

6 - EXPERIMENTAL RESULTS

Fig. 6 shows the programmability of a current mirror designed with discrete op amps and MOSFET-only current dividers. A prototype of an SI lossy integrator has been built with NMOS ($W = 6\mu\text{m}$, $L = 5\mu\text{m}$) integrated transistors and discrete opamps, switches and capacitors. The integrator scheme has been obtained from the delay

circuit shown in Fig. 7 by feeding the output current βi_O back to the input node (A). The z -domain transfer function of the integrator is

$$H(z) = \frac{I_0^{\phi 1}(z)}{I_1^{\phi 1}(z)} = \frac{z^{-1}}{1 - \beta z^{-1}} \quad (5)$$

The measured magnitude responses of the lossy integrator are presented in Fig. 8 for $\beta = 7/8, 3/4, 1/2$.

7 - CONCLUSIONS

A current mirror using MOSFET's operating in the triode region has been proposed and analyzed. The main advantage of this mirror, compared with the conventional ones, is its easy programmability. A new switched current technique, which employs opamps, switches, gate capacitors and MOSFET's has been described. The use of MOSFET-only current dividers for the proposed current mirrors allows compact programmability when compared to traditional programming techniques that employ binary-weighted capacitor or transistor arrays. Moreover, the proposed technique is suited to low-voltage operated systems.

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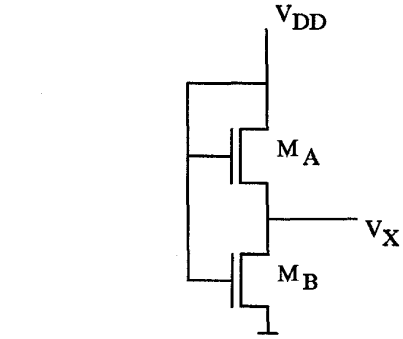
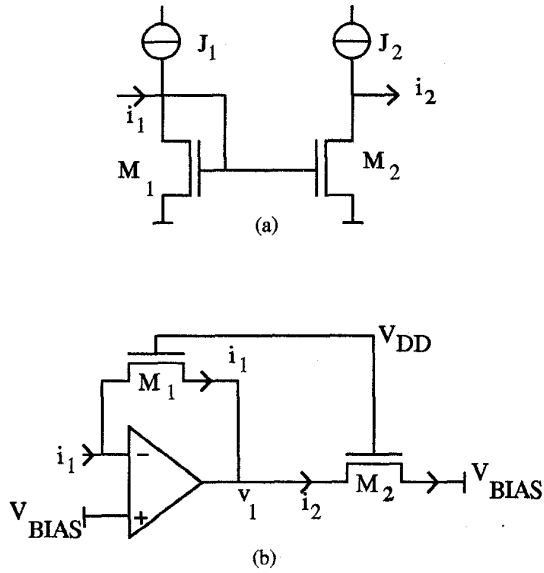


Fig. 3. Bias circuit for the proposed current mirror. M_A and M_B are identical transistors. $V_X = V_P(1 - 1/\sqrt{2})$. V_P is the pinch-off voltage [5,6].

Fig. 1. (a) Conventional current mirror. (b) Proposed current mirror.

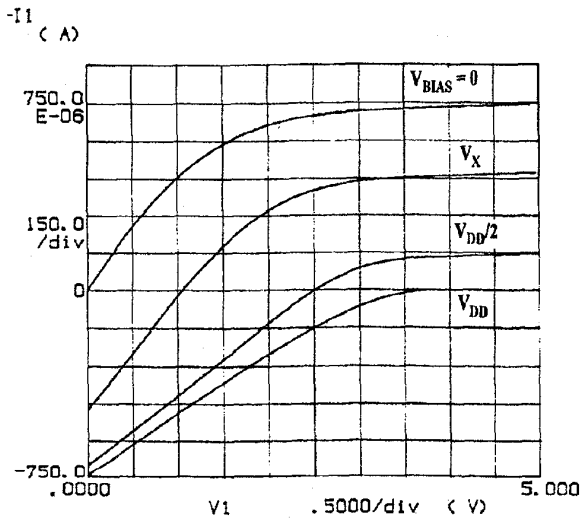


Fig. 2. I_D vs. V_D for different values of V_{BIAS} . V_X is the bias voltage obtained from the circuit shown in Fig. 3.

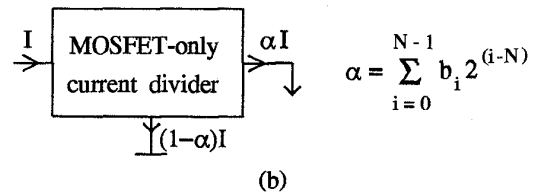
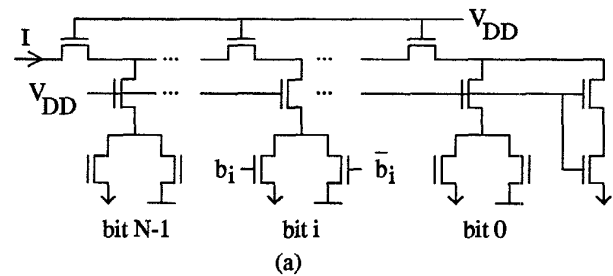
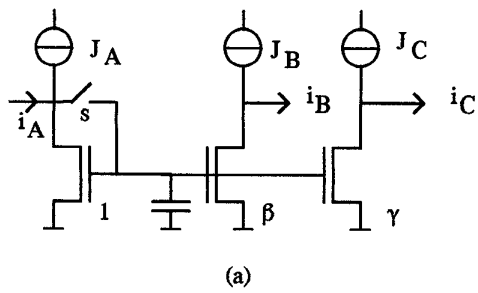
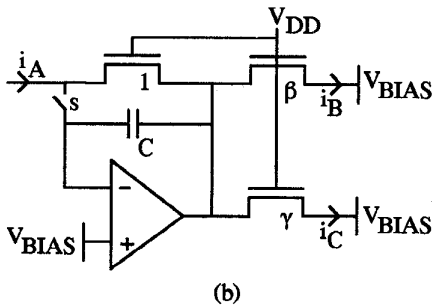


Fig. 4. (a) MOSFET-only current divider. (b) its symbol.



(a)



(b)

Fig. 5. Switched current mirrors: (a) conventional. (b) proposed in this work.

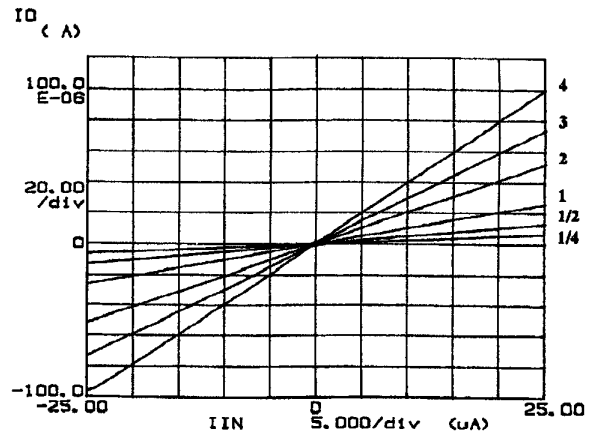


Fig. 6. Output current vs. input current of the programmable current mirror.

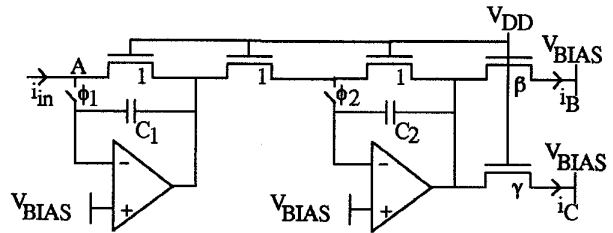


Fig. 7. Switched current circuit whose outputs are delayed scaled replicas of the input current.

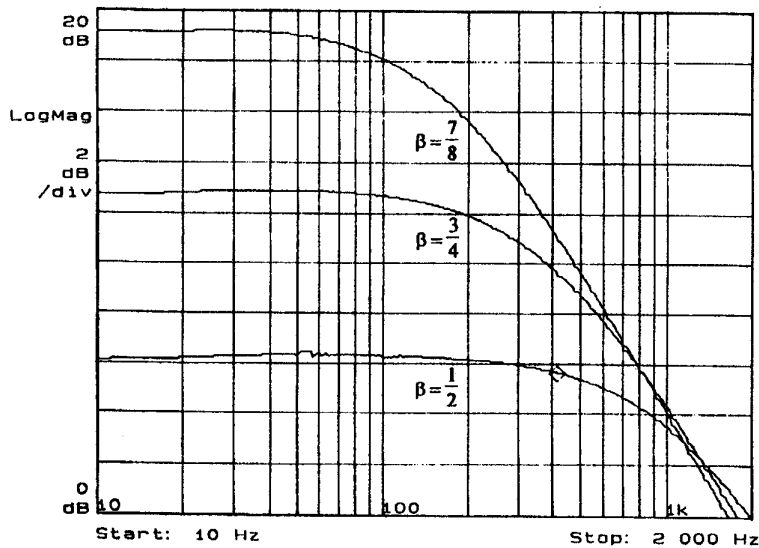


Fig. 8. Measured magnitude responses of the SI integrator for a clock frequency of 10 kHz.