Design Techniques for Analog Circuits in Sea of Transistors

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ABSTRACT

This paper shows that the use of the series-parallel association of transistors can substitute with advantages transistors with arbitrary W and L.

Also, the use of composite transistors allows the design of current dividers which can be used for D/A conversion. As consequence, it becomes clear that the design of high performance analog circuit in a conventional SOG is very well possible.

I. INTRODUCTION

Sea of Gates (SOG) or Sea of Transistors (SOT) are widely used for the implementation of digital circuits [1]. The main advantages of SOG over full custom design are the reductions in mask fabrication costs, design time and fabrication time [1-2]. Another important characteristic of SOG is that new technologies are usually first introduced for them because of the significant lower overhead in design support [1].

In view of the trend toward mixed-mode ASICs, there is a growing interest for the realization of analog circuits on SOG [2-6]. Some analog applications such as amplifiers, A/D and D/A converters have been reported [2-6]. However, SOG has not been employed to implement more complex mixed analog/digital circuits such as, for example, those required for communications systems. In fact, the only non-parasitic components available in a SOG are minimum length MOS transistors. By other hand, conventional analog integrated circuits require the free choice of transistor's width (W) and length (L), high-quality capacitors and good component matching.

It must be remarked that in SOG, the use of special dedicated parts for the analog design must be discarded because of the loss of flexibility and the inefficient use of the available chip area [6].

This paper shows that the use of the series-parallel association of transistors [7] can substitute with advantages transistors with arbitrary W and L. Also, the use of composite transistors allows the design of current dividers which can be used for D/A conversion and programmable analog functions [11-13].

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II. TRAPEZOIDAL ARRAY OF TRANSISTORS

Series and parallel associations of transistors are indispensable to get the aspect ratios required for analog design in SOG. Assuming a specific W/L is required for a transistor, a usual way to obtain this aspect ratio is to connect in parallel m branches of n series-connected transistors. Here, $m = W/W_u$ and $n = L/L_u$, being W_u and L_u the width and length, respectively, of a single transistor. This solution would need a rectangular array of mxn transistors to emulate the required W/L aspect ratio. As an alternative solution [7] to a rectangular array of transistors is a trapezoidal one, as shown in Fig. 1. It has been demonstrated [7] that a rectangular array and a trapezoidal array are DC equivalent if they have the same aspect ratio and the same width at the drain side. Therefore, the arrays shown in Figs. 1(b) and 1(c) are DC equivalent. As can be seen in Fig. 1, the trapezoidal array has a big advantage over its DC equivalent rectangular array - significant area saving and, consequently, a higher cutoff frequency. The price to be paid is the reduced matching and the increased $1/f$ noise. In this paper we will compare the characteristics of the trapezoidal and rectangular arrays in order to provide some guidelines for analog design in SOG.

DC characteristics and available voltage gain

As mentioned before, the DC characteristics of the trapezoidal and rectangular arrays are almost the same. The available voltage gains differ slightly in the weak inversion region, as can be seen in Fig. 2. This difference can be attributed to short channel effects, which are more pronounced in the trapezoidal array due to its shorter length. Particularly, for the weak inversion region, the dominant short channel effect which explains the difference between the gains of the two structures is the so-called drain-induced barrier lowering (DIBL).

Area and frequency response

Fig. 1 shows that the trapezoidal array requires a silicon area m times smaller than that of the rectangular array. Analysis of the frequency response [7] has shown that, for strong inversion, the cutoff frequency of the trapezoidal array is approximately $m^{3/2}$ times higher than that of the rectangular array.

As example, the simulated characteristics of two Miller's OTA (fig. 3), one using rectangular arrays are shown in table 1. The geometry of the transistors is reported in table 2.

TABLE I
Amplifier performance summary (V_{dd} = 2.5 V, V_{ss} = -2.5 V)

	trapezoidal array.	rectangular array.
Low frequency gain	76dB	76 dB
Bandwidth	1.6 MHz	1.5 MHz
Phase margin	73°	65°
Settling time (1%)	3.2 useg.	5 useg
Output voltage swing	-2.5 a 2.5	-2.5 a 2.5
Slew rate	1.5 V/us	1.4 V/us
Area	1380 um2	2970 um2
Power dissipation	0.23 mW	0.24 mW

TABLE II
Component sizes

	trapezoidal op. amp.	rectangular op. amp.
M1 - M2	trapezoidal array (m=5) 24/1.2*	rectangular array (5x6) 24/1.2 *
M3 - M4	30/1.2 (m=5) *	30/1.2 (5x6) *
M5	24/1.2	24/1.2
M6	60/1.2	60/1.2
M7	24/1.2	24/1.2
M8	30/30	30/30
Cc	10 pF	10 pF
Cl	20 pF	20 pF

* Dimension of unity transistor.

Matching

In order to evaluate mismatch effects in trapezoidal arrays, let us assume the MOSFET drain current in the triode region is given by [8]

$$I = \beta\left[f\left(V_G - V_T, V_S\right) - f\left(V_G - V_T, V_D\right)\right] \tag{1}$$

where $f(.,.)$ is a function that describes the current dependence on the terminal voltages. The other symbols have their usual meaning. In saturation the last term in eqn. (1) can be neglected.

Now, compute the relative current deviation in an array of transistors due to transistor mismatches. The application of eqn. (1) for a generic array of transistor leads to

$$\frac{\Delta I}{I} = \frac{\beta_S}{\beta_S+\beta_D}\left[\frac{\Delta\beta_D}{\beta_D} - \left(\frac{g_m}{1}\right)_D \cdot \Delta V_{TD}\right] + \frac{\beta_S}{\beta_S+\beta_D}\left[\frac{\Delta\beta_S}{\beta_S} - \left(\frac{g_m}{1}\right)_S \cdot \Delta V_{TS}\right] \tag{2}$$

where the subscripts S and D refer to the arrays between nodes X and S and between nodes X and D, respectively. The terms between the square brackets are the well-known terms which account for current mismatch in conventional current mirrors [9]. Note that for the arrays shown in Figs. 1(b) and 1(c), $\beta_D/\beta_S = m$. Therefore, in a current mirror or in a differential pair of trapezoidal transistor arrays, special care should be taken in order to match as close as possible the transistors connected to the source, since their mismatch is the prevailing factor in the overall mismatch.

Let us now suppose that both V_T and β are random variables whose standard deviations are defined [10] by

$$\sigma^2\left(V_T\right) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2$$
$$\sigma^2(\beta) = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{3}$$

where A and S are process-dependent constant and D is the distance between devices under consideration. Applying eqns. (3) into eqn. (2) leads to the following ratio between standard deviations:

$$\frac{\sigma^2(\Delta I/I)_{\text{trap}}}{\sigma^2(\Delta I/I)_{\text{rect}}} = 1 + \left(m^2 - 1\right)\varepsilon(I,m) \tag{4}$$

where $0 \le \varepsilon(I,m) \le 1$ depends on the mismatch parameters (A's and S's). The previous analysis can also be done to compute the offset voltage in a differential pair made up of arrays of transistors. Typical experimental results for current mismatches in current mirrors are shown in Fig. 4.

Experimental results shown in Fig. 2 and Fig. 4 were obtained for $m=3$. The dimensions of the unit transistor are: $\left(\frac{W}{L}\right)_N = \frac{12}{2}$ and $\left(\frac{W}{L}\right)_P = \frac{30}{2}$.

III. MOSFET-ONLY CURRENT DIVIDERS

MOSFET-only current dividers (MOCD) [11] as shown in Fig. (5) are analog building-blocks tailored for the SOG environment. In fact , they are obtained by the series-parallel association of elementary transistors and their input characteristics are those of single transistors [7].

The output current of the current attenuator is a fraction, selected by a digital word, of the input current. This

programmable current divider has two big advantages over other digitally programmed dividers: (i) MOSFET's perform simultaneously as elements of the divider network and as switches and (ii) the impedance of the current attenuator is independent of the number of bits and the attenuation factor. Moreover, the high linearity of this current division technique [11] has been proved adequate for analog signal processing. The applications of this technique are many, including D/A converters [12], switched current filters [13], programmable attenuators [11], mirrors [13], etc.

IV. CONCLUSIONS

Analog designers in SOG can advantageously use trapezoidal arrays of transistors instead of rectangular arrays in order to save area and increase bandwidth. Likewise, high gain, high bandwidth differential amplifiers and current mirrors implemented in a SOG environment, can profit from the higher performances offered by the trapezoidal configuration over its rectangular counterpart.

Finally, composite transistors allow the design of current dividers which can be used for D/A conversion and programmable analog functions.

V. REFERENCES

1. M. A. Beunder, J. P. Kernhof, and B. Hoefflinger, 'The CMOS gate forest: An efficient and flexible high-performance ASIC design environment', *IEEE J. Solid-State Circuits*, vol. 23, no. 2, pp 387-399, April 1988.
2. P. Duchene and M. J. Declercq, 'A highly flexible sea-of-gates structure for digital and analog applications', *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp 576-584, June 1989.
3. S. Masuda, S. Koazechi, T. Mizuca, K. Kimura, K. Matsumoto, Y. Kitamura, 'A CMOS analog and digital masterslice LSI', in *ISSCC Dig. Tech. Papers*, 1987, pp 146-147.
4. S. Kawada, Y. Hara, T. Isono, and T. Inuzuka, '1.5-μm CMOS gate arrays with analog/digital macros designed using common base arrays', *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp 985-990, August 1989.
5. P. P. Duchêne, M. J. Declercq, B. Goffart, and M. Novak, 'Analog circuit implementation on CMOS semi-custom arrays', *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp 872-874, July 1993.
6. R. van Dongen and V. Rikkink, 'Advanced analog circuit design on a digital Sea-of-Gates Array', *Proc. of EDAC-EUROASIC*, 1994, pp70-74
7. C. Galup-Montoro, M. C. Schneider, and I. J. Loss, 'Series-Parallel Association of FET's for High Gain and High Frequency Applications', *IEEE J. Solid-State Circuits*, vol.29, no. 9, pp. 1094-1101, September 1994.
8. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw Hill, New York, 1987.
9. E. Vittoz, 'Micropower Techniques', in *Design of Analog-Digital Circuits for Telecommunications and Signal Processing*, J. E. Franca and Y. P. Tsividis (editors), Prentice Hall, 1994.
10. M. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, 'Matching Properties of MOS Transistors', IEEE JSSC, vol. 24. no.5, pp 1433-1440, October 1098.
11. K. Bult and G. J. G. M. Geelen, 'An Inherently Linear and Compact MOST-Only Current Division Technique', *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1730-1735, December 1992.
12. R. T. Gonçalves, C. G. Montoro, M. C. Schneider, 'A D/A converter based on a transistor-only R-2R ladder network', *Proceedings of the Conference of Sociedade Brasileira de Microeletrônica, VIII SBmicro*, Campinas, SP, Brazil, pp II.1-II.4, september 1993
13. R. T. Gonçalves, S. Noceti Filho, M. C. Schneider, C. Galup-Montoro, 'Programmable switched current filters using MOSFET-only current dividers', *1995 Midwest Symposium on Circuits and Systems.*

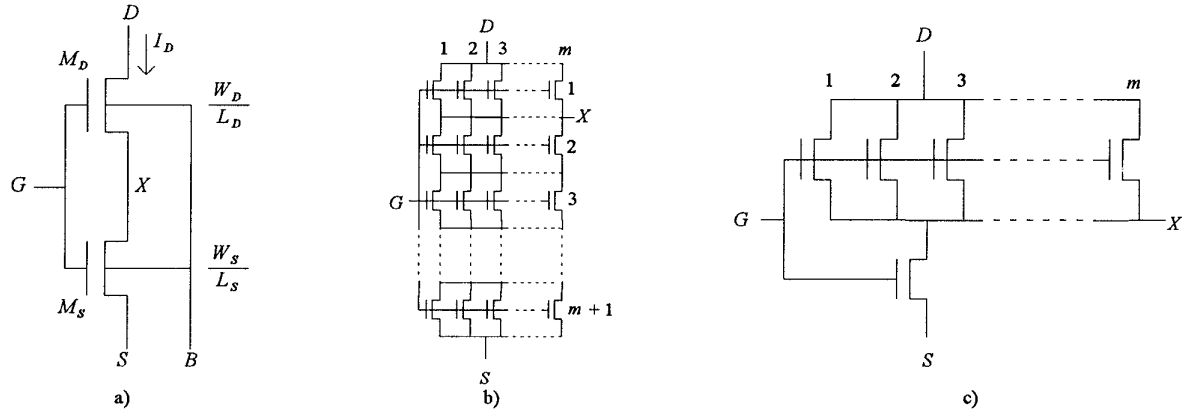

Fig. 1.: a) Composite transistor $L/W = L_D/W_D + L_S/W_S$; b) Rectangular array of transistors $L/W = L_u/mW_u + mL_u/mW_u$; c) Trapezoidal array of transistors $L/W = L_u/mW_u + L_u/W_u$

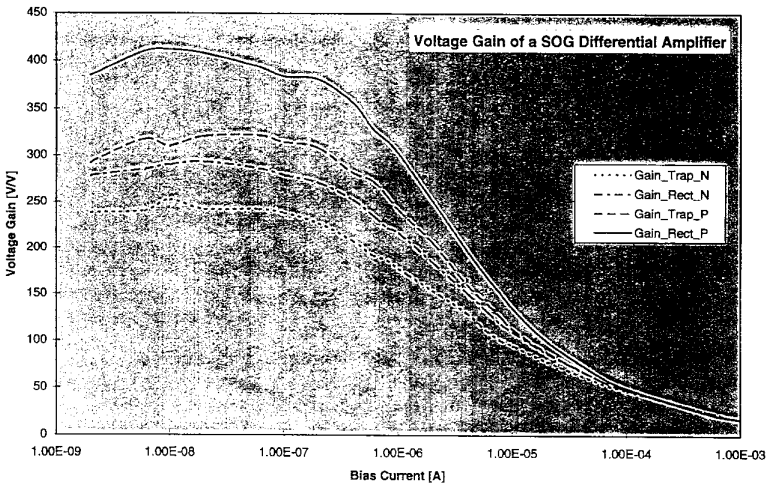

Fig. 2. Available voltage gains in the trapezoidal and rectangular arrays.

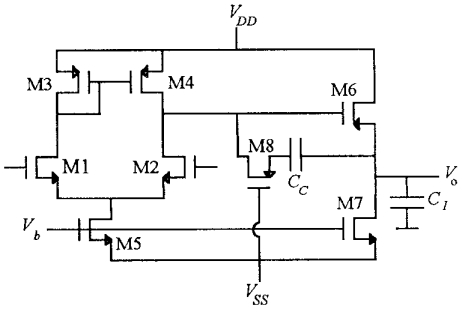

Fig. 3. Miler OTA.

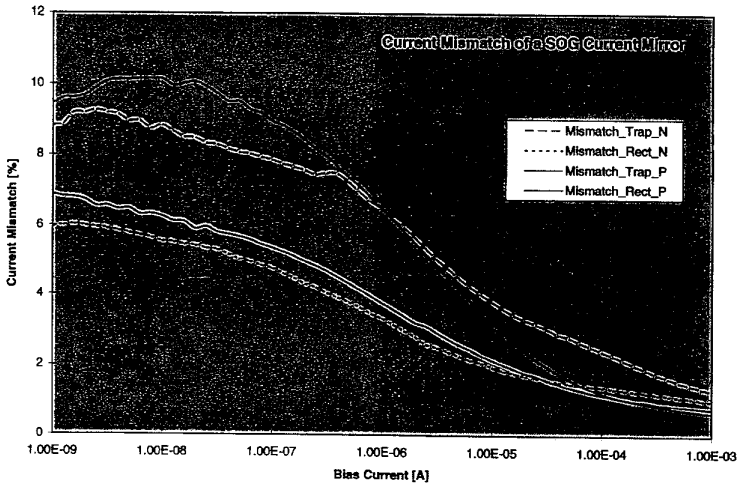

Fig. 4. Current mismatch in current mirrors.

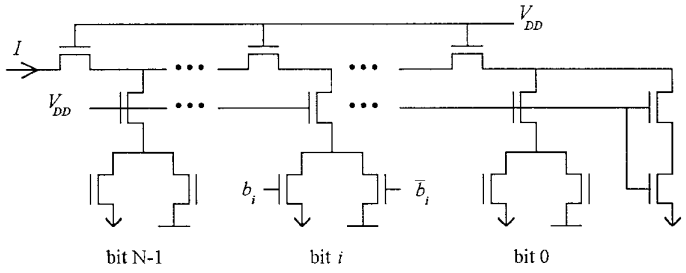

Fig. 5. MOSFET-only current divider (MOCD).