Programmable switched current filters using MOSFET-only current dividers

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ABSTRACT

A new technique to achieve switched current filters is presented. The basic elements of the filters are operational amplifiers, switches, MOS transistors and grounded capacitors. The use of MOSFET-only current dividers allows digitally programming the coefficients of the filter transfer function. User programmable analog filtering in digital CMOS technology and, particularly, in sea-of-gates is the main envisaged application of the proposed technique.

INTRODUCTION

Switched capacitors (SC) and switched currents (SI) are the sampled data processing techniques in use nowadays. SC filters, usually implemented through double-poly CMOS processes, have performance rarely matched by other types of analog integrated circuits and, as a consequence, have been extensively employed in commercial analog circuits. The driving force behind the development of the SI technique at the end of the last decade [1] was its full compatibility with conventional VLSI processes. However, few circuits using SI techniques have been fabricated to date [2,3]. Therefore, it is hard to conclude about the merit of SI circuits for a wide range of applications. Moreover, the digital programming of conventional analog filters achieved by selecting different combinations of either capacitors [4] or current mirrors [5] requires a large silicon area.

In this paper we show a procedure that employs opamps, MOSFET-only programmable current attenuators [6], switches and capacitors to realize SI filters. This approach to implement programmable filters takes advantage of the reduced area, proportional to the number of bits, of programmable MOSFET-only attenuators. The use of the opamp as the active device allows a simple and modular design of the filter. Even though nonlinear, grounded MOS capacitors [7] are the natural solution to act as memory elements.

THE SWITCHED CURRENT TECHNIQUE

Sampled-data analog signal processing requires four basic operations: inversion, addition, multiplication and delay. In SI circuits, these operations are accomplished by switched current mirrors. Current mirrors realize a nonlinear I-V conversion followed by an inverse V-I conversion, leading to a linear relationship between input and output currents. Fig. 1(a) displays the scheme of the conventional switched current mirror [1].

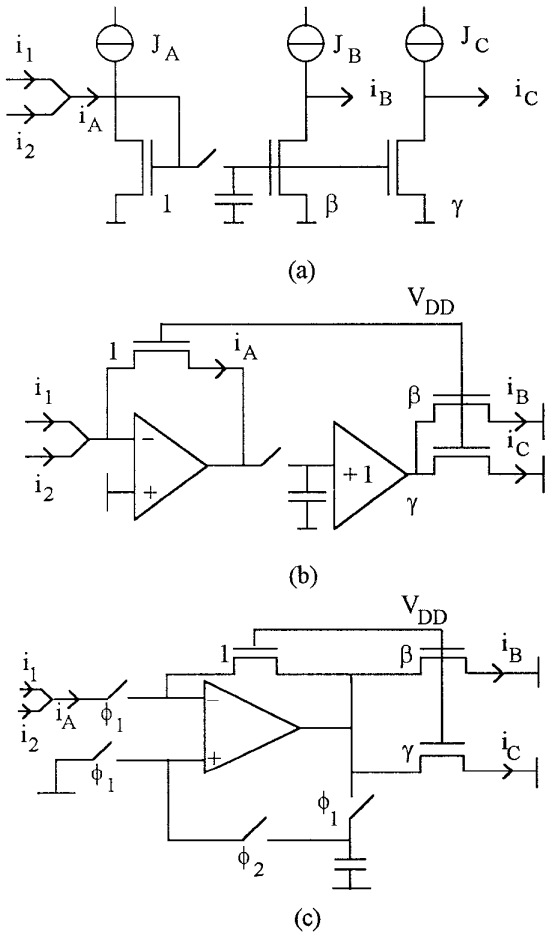

Fig. 1. First generation switched current mirrors
(a) conventional (b) proposed in this work
(c) modified version

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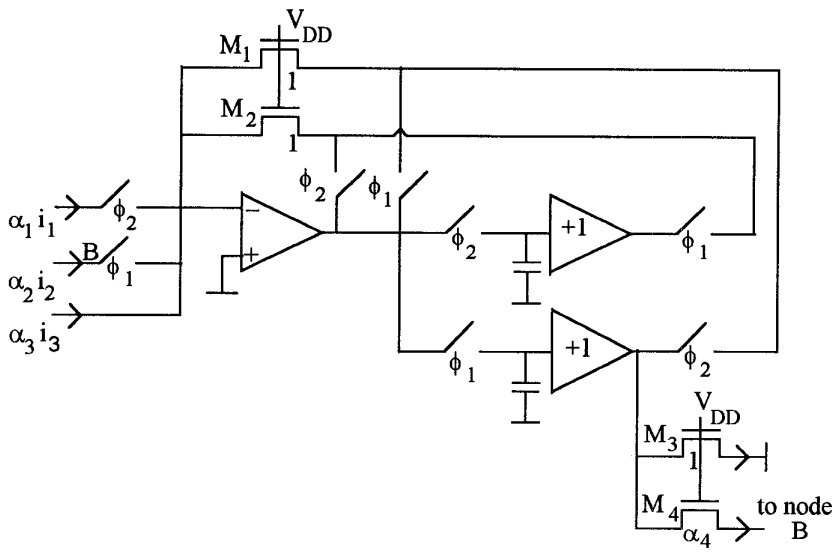

Fig. 2 - Second generation generalized switched current integrator

As shown in Fig. 1(b), a switched current mirror can also be implemented with one MOS transistor connected between the output and the virtual ground of the opamp and another between the output and ground (or a virtual ground of another opamp). With the switch closed, the hold capacitor is charged to a voltage V, which depends on the value of the input current i_A, the transistor parameters and the gate voltage. The output current is such that $i_B = -\beta\, i_A$, where β is the scale factor. When the switch opens, a voltage equal to V is held on the memory capacitor and the current is sustained at the output. The voltage follower avoids the discharge of the hold capacitor through the output transistors.

In order to reduce the number of operational amplifiers the cell shown in Fig. 1(c), where the clock waveforms are non-overlapping, can be used as an SI mirror. For the three cases presented in Fig. 1 the scale factor β of the current mirrors is equal to the quotient of the aspect ratios of the output and input transistors.

A building block for use in SI filters is the integrator. Fig. 2 shows the generalized second generation SI integrator [8], implemented according to the approach presented in this paper. The analysis of the network in fig. 2 is straightforward, leading to the following z-domain output current:

$$I_o(z) = \frac{A_1 z^{-1}}{1 - Bz^{-1}} I_1(z) - \frac{A_2}{1 - Bz^{-1}} I_2(z) \qquad \frac{-A_3(1 - z^{-1})}{1 - Bz^{-1}} I_3(z) \qquad (1)$$

where

$$A_1 = \frac{\alpha_1}{1+\alpha_4} \quad A_2 = \frac{\alpha_2}{1+\alpha_4} \quad A_3 = \frac{\alpha_3}{1+\alpha_4}$$

$$B = \frac{1}{1+\alpha_4}$$

Even though we have shown the application of the new method to implement SI filters through the examples of a delay and an integrator, we can readily extend it to any conventional SI filters [1,2,8].

In order to provide the current mirrors in Figs. 1(b) and 1(c) with digital programmability, MOSFET-only current dividers [6] can be used instead of MOS transistors.

Fig. 3 shows the principle of current division [6,9] for an array of identical transistors, where the current is successively divided by two in the branches of the network. The output current is a fraction of the input current, selected by, say, the ON state of the left side transistors in the parallel connections. This programmable current divider has two big advantages over other digitally programmed dividers: (i) MOSFET's perform simultaneously as elements of the divider network and as switches and (ii) the resistance of the current attenuator is independent of both the number of bits and of the attenuation factor. Moreover, the high linearity of this current division technique [6] has been proved adequate for analog signal processing.

A circuit which delays current samples by one complete clock period is shown in fig 4. This circuit is analogous to the first generation current delay cell, presented in ref. [1]. The inclusion of a current inversion block provides the network with outputs that are non-inverted replicas of the

input current. One of the output currents, delayed from the input current by one clock period is given by

$$\beta\, I_o(z) = (\beta/\alpha) z^{-1} I_i(z) \qquad (2)$$

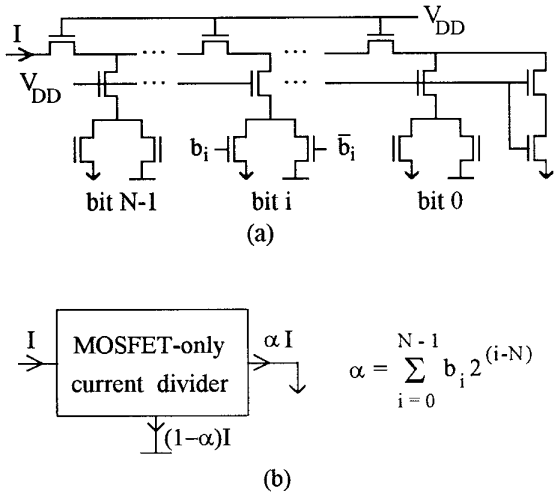

Fig. 3 -(a) MOSFET-only binary current divider and (b)its symbol.

A digitally programmable current integrator can be implemented by feeding back a fraction of the output current from a current delay circuit, such as the one shown in Fig. 4. By feeding back, for instance, the output current βI_o to the input node, one obtains the z-domain transfer function

$$H(z) = \frac{I_o(z)}{I_i(z)} = \frac{1}{\alpha} \cdot \frac{z^{-1}}{1 - \frac{\beta}{\alpha} z^{-1}} \qquad (3)$$

which corresponds to a forward Euler non-inverting lossy integrator if $(\beta/\alpha) < 1$ or to a lossless integrator if $(\beta/\alpha) = 1$.

Experimental Results

A prototype of an SI lossy integrator has been built with NMOS (W=3μm, L=1.2μm) integrated transistors and discrete opamps, switches and capacitors. The integrator scheme has been obtained from the delay circuit shown in Fig.4 by feeding back the output current βI_o to the input. The parameters of the network are $\alpha = 1$ and $\gamma = 1-\beta$.

Therefore, the z-domain transfer function is

$$H(z) = \frac{\gamma\, I_o(z)}{I_i(z)} = \frac{(1-\beta) z^{-1}}{1 - \beta\, z^{-1}} \qquad (4)$$

The output of the integrator (β=7/8) for a 3.6 *kHz* input current is shown in Fig.5 and the measured magnitude responses of the lossy integrator are presented in Fig.6 for β = 7/8, 3/4, 1/2. The measured and the theoretical magnitude responses of the integrator agree very closely.

Conclusions

A new switched current technique, which employs opamps, switches, grounded capacitors and MOSFET's has been described. Three methods regarding the realization of SI filters have been proposed.

The use of MOSFET-only current dividers in the output and feedback of the opamps allows digitally programming the filter coefficients without requiring large silicon areas. Therefore, the proposed technique is very useful for analog programmable filters.

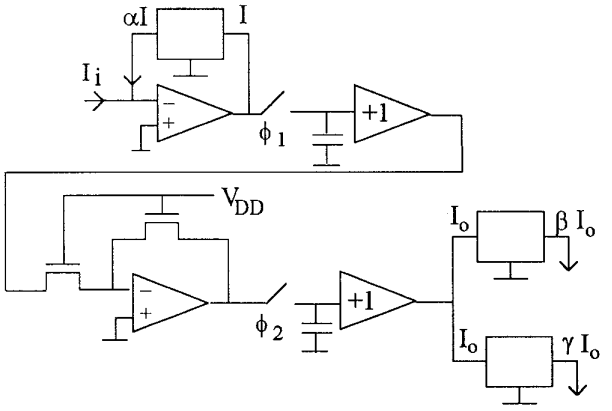

Fig.4 - Switched current circuit whose outputs are delayed scaled replicas of the input current

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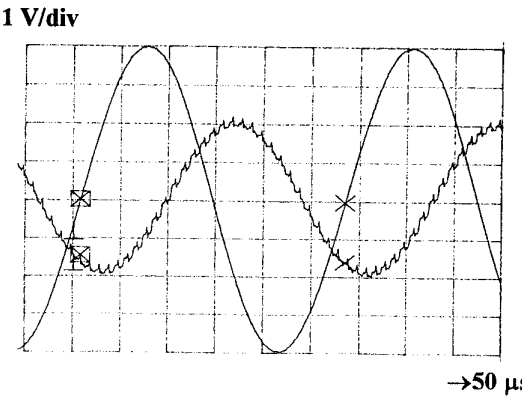

Fig.5 -Integrator (β=7/8) output and input waveforms measured at 3.6 kHz, the approximate -6dB frequency for a clock frequency of 100 kHz .

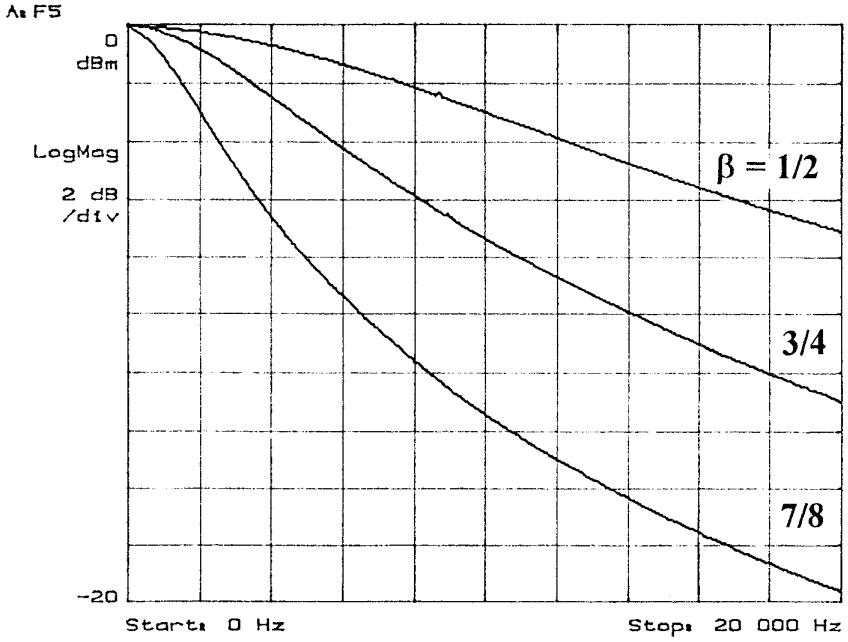

Fig.6 -Measured magnitude responses of the SI integrator for a clock frequency of 100 kHz.