Low Output Conductance Composite MOSFET's for High Frequency Analog Design

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ABSTRACT

This paper presents a simple approach to design composite FET's with low output conductance. These composite transistors consist of the series association of two transistors, with the transistor connected to the drain terminal wider than the transistor connected to the source terminal. A composite transistor has two main advantages over its "DC equivalent" transistor of uniform width: significant area savings and a much higher cutoff frequency.

INTRODUCTION

The growing trend towards smaller feature sizes and, consequently, to lower supply voltages in VLSI leads to new challenges in the design of MOS analog circuits . A basic problem to be solved is the design of high-gain single-stage amplifiers [1]. Two commonly employed methods to increase low-frequency gain are either to increase the length of the transistors or use cascoded transistors [2]. However, the transistor cutoff frequency is inversely proportional to the square of the channel length [3]. Hence, the use of long-channel transistors is restricted to low frequency applications. On the other hand, cascoding transistors results in a loss in linear output swing for the amplifier [2].

In this work we propose a composite transistor that has been inspired from a 1984 paper by Riccó [4]. The composite transistor consists of the series association of two transistors, with the transistor connected to the drain terminal wider than the transistor connected to the source terminal. This device has a transconductance-to-output conductance ratio as high as that of a long-channel transistor but a higher cutoff frequency and a smaller area.

DC CHARACTERISTICS

We consider the series association of transistors as the one shown in Fig. 1, i. e., the gate and bulk terminals are common to both transistors.

Triode region

In the triode region, using the gradual channel approximation, the drain current of an MOS transistor can be written [3] as

$$I_D = \frac{W}{L}\,[\,g(V_G, V_S) - g(V_G, V_D)\,] \qquad (1)$$

where all voltages are referred to the substrate, emphasizing the symmetry between drain and source. W and L are the channel width and channel length, respectively and $g(V_G, V)$ is a function that describes the DC behavior of the MOS transistor.

For the series connection of transistors (Fig. 1), assuming the drain voltage V_D is such that transistor M_D is biased in the triode region, one obtains

$$g(V_G, V_X) = \frac{(\frac{W}{L})_S\, g(V_G, V_S) + (\frac{W}{L})_D\, g(V_G, V_D)}{(\frac{W}{L})_S + (\frac{W}{L})_D} \qquad (2a)$$

from applying eqn. (1) for both transistors. From eqns. (1) and (2a) the drain current in the composite transistor is

$$I_D = (\frac{W}{L})_{eq}\,[g(V_G, V_S) - g(V_G, V_D)] \qquad (2b)$$

where

$$(\frac{W}{L})_{eq} = \frac{(\frac{W}{L})_D\,(\frac{W}{L})_S}{(\frac{W}{L})_D + (\frac{W}{L})_S} \qquad (2c)$$

In the triode region, the composite transistor has a DC behavior equal to that of a single transistor whose aspect ratio is given by eqn. (2c).

Transistors M_S and M_D (Fig. 1) of different widths and lengths can be implemented with rectangular arrays, as shown in Fig. 2.

Saturation region

The equivalence of transistors in the triode region is extended to the saturation region if the transistors have, in addition to the same aspect ratio, the same channel width at the drain end. These two conditions are fulfilled by the

composite transistors illustrated in Fig. 2. Transistors M_{S1}, M_{S2} and M_{S3}, connected between nodes X and S, have different channel lengths but the same aspect ratios.

The behavior of these composite transistors in saturation can be better understood with the aid of Fig. 3, which presents the classical determination of the operating point from the output characteristics of transistors M_{S1}, M_{S2}, M_{S3} and from the load curve due to transistor M_D. The difference in the two load curves shows that transistor M_D, which operates in the saturation region, presents short-channel effects. The almost coincidence of the output characteristics of M_{S1}, M_{S2} and M_{S3} in the triode region indicate that transistors with the same aspect ratio have the same DC characteristics in this region despite the existence of short-channel effects. Hence, the drain current of the composite transistors in saturation and, consequently, their output conductances are approximately equal.

Summarizing, two transistors with the same technological parameters are DC equivalent if they have:

(i) the same aspect ratio,

(ii) the same channel width at the drain end.

(iii) equal short-channel effects in the triode region

From conditions *(i)* and *(ii)*, the "DC equivalent" electrical width and length of the composite transistor can be easily derived:

$$W_{eq} = W_D \tag{3a}$$

$$L_{eq} = L_D + m L_S \tag{3b}$$

where m is equal to the ratio W_D/W_S.

Therefore, in order to obtain a composite transistor equivalent to a long channel transistor but with a shorter physical channel length, we should choose a transistor with $m>1$, i. e., a composite transistor wider at the drain end than at the source end.

Fig. 4 shows an example of two DC equivalent arrangements of unit transistors.

TRANSIT TIME

Usually, the transistor response to dynamic signals is characterized by the transit time (τ) and/or the intrinsic cutoff frequency (ω_T). For the saturated MOS transistor in strong inversion these two parameters are related [3] by

$$\tau \omega_T = 2 \tag{4}$$

It can be demonstrated that eqn. (4) is also approximately valid for a composite transistor. For the composite MOS device in Fig. 4(a), the transit time has been calculated using the charge expression from refs. [1,5]:

$$\tau = \tau_u \{[(1+\frac{1}{m})^2 - \frac{\sqrt{1+m}}{m^2}] + \sqrt{1+m}\} \tag{5}$$

In the previous analysis we have considered the transistors connected to source and drain terminals with minimum channel length, equal to L_u, provided by the technology. τ_u is the transit time of the minimum-length transistor. In eqn. (5) the first term, between square brackets, represents the transit time of the transistor connected to the source terminal while the second term is associated to the transit time of the transistor connected to the drain terminal.

EXPERIMENTAL RESULTS

In order to demonstrate the theoretical results, arrays of transistors of minimum channel-length in a 1.2 μ m CMOS n-well process have been built. Fig. 5 shows the output characteristics of the two arrays of transistors in Fig. 4. These characteristics are almost coincident, specially the output conductances in the saturation region. In order to determine the transit time we have built the composite devices with large geometry p-channel transistors. Fig. 6 exhibits the normalized transit time of the composite transistor in terms of m, the number of unit transistors connected to the drain terminal.

CONCLUSIONS

We have proposed a method to design composite transistors wider at the drain side than at the source side. These transistors can be designed to obtain a transconductance-to- output conductance ratio much larger than that of a short-channel transistor with only a little penalty in the cutoff frequency and without reduction in signal swing. Hence, composite transistors are very useful for the design of simple scheme analog sections for high-speed and low-voltage applications. Composite transistors also provide a natural solution for gate array design of analog circuits.

ACKNOWLEDGMENT

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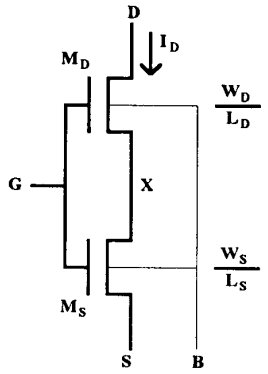


Fig. 1. Series connected transistors.

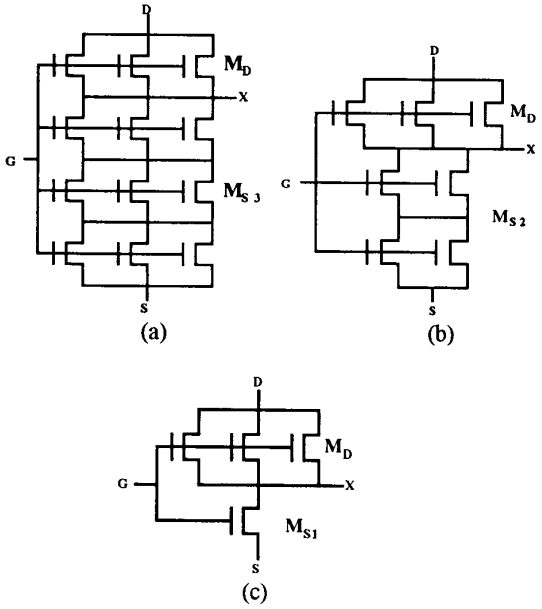


Fig. 2. Arrays of unit transistors with the same drain width ($W_D=3W_u$) and the same aspect ratio $(W/L)_{eq}=3/4$.

(a) $\left(\frac{L}{W}\right)_{eq}=\frac{3L_u}{3W_u}+\frac{L_u}{3W_u}$ (b) $\left(\frac{L}{W}\right)_{eq}=\frac{2L_u}{2W_u}+\frac{L_u}{3W_u}$

(c) $\left(\frac{L}{W}\right)_{eq}=\frac{L_u}{W_u}+\frac{L_u}{3W_u}$

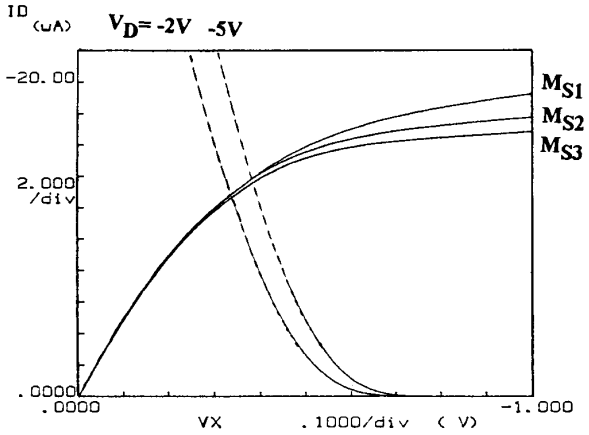


Fig. 3. Output characteristics of transistors M_{S1}, M_{S2}, M_{S3} and load curve due to transistor M_D from Fig.2 at V_G=-1.8V

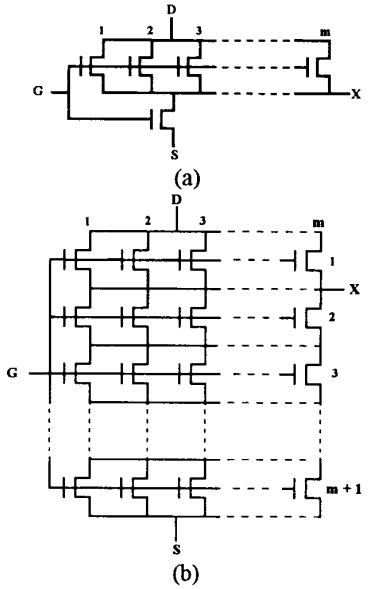


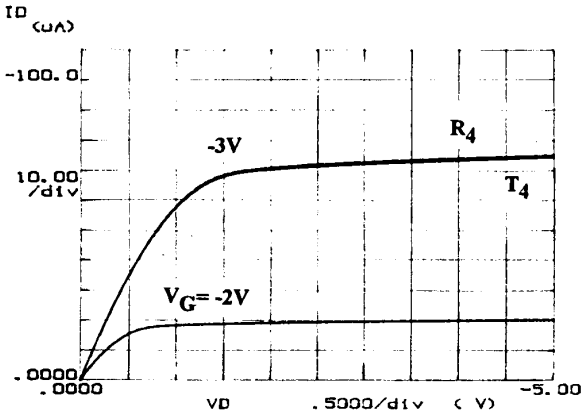
Fig. 4. Composite transistors:

(a) Trapezoidal type composite transistor (T_m - transistor)

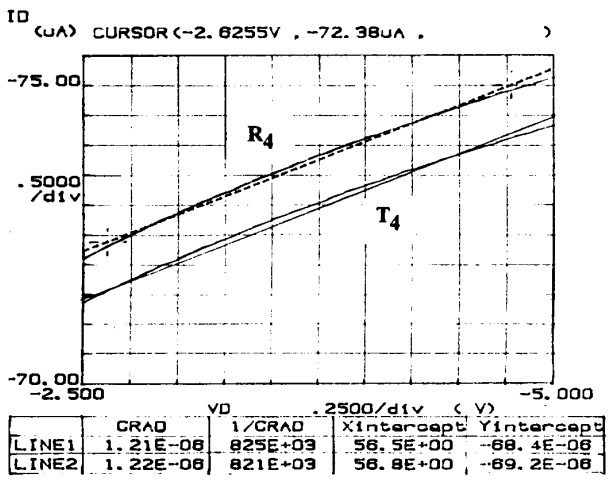
$$\left(\frac{L}{W}\right)_{eq}=\frac{L_u}{W_u}+\frac{L_u}{mW_u}$$

(b) Rectangular type composite transistor (R_m - transistor)

$$\left(\frac{L}{W}\right)_{eq}=\frac{mL_u}{mW_u}+\frac{L_u}{mW_u}$$



(a)



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.21E-08	825E+03	56.5E+00	-68.4E-08
LINE2	1.22E-08	821E+03	56.8E+00	-69.2E-08

(b)

Fig. 5. (a) DC characteristics of the rectangular (R_4) and trapezoidal (T_4) composite transistors.

(b) Detail in the saturation region.

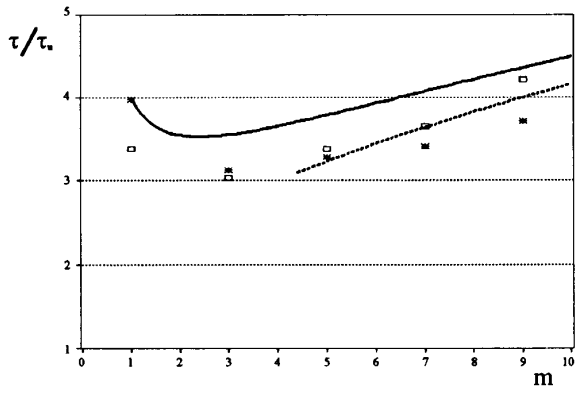


Fig. 6. Normalized transit time of the T_m-transistor (m is the number of parallel-connected transistors at the drain side):

theoretical

asymptotic curve for high values of m

□ experimentally determined at V_{GS} = -2 V

✱ experimentally determined at V_{GS} = -3 V