ON THE IMPLEMENTATION OF SWITCHED CAPACITOR CIRCUITS IN GATE ARRAYS

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Abstract: This paper presents results concerning the implementation of switched capacitor (SC) filters with weakly nonlinear capacitors. It is shown that low distortion transistor-only SC filters can be realized employing MOSFET gate structures biased in accumulation or strong inversion to implement the capacitors. As a consequence, mixed analog/digital circuits can be fully integrated using CMOS gate arrays.

INTRODUCTION

Gate arrays cover roughly 50 percent of the present ASIC market [1]. Three decisive advantages in comparison with full-custom designs are a reduced turnaround time, a reduced fabrication cost and, finally, a reduced design time [1]. Using this technique, about one tenth of the turnaround time can be achieved compared with full-custom LSI's for the same system [2]. This feature, combined with a reduced design time, avoids delays in bringing the product to market.

The predominant uses of CMOS gate arrays today are for pure digital applications but the demand for miniaturization makes it necessary to implement analog as well as digital functions on a single IC. Some analog applications such as amplifiers [1-5], A/D and D/A converters employing either an external resistor network [4] or internal diffused resistors [2], have been reported in the technical literature. However, gate arrays have not been employed to implement more complex mixed analog/digital circuits such as, for example, those required for communication systems. In fact, small area A/D and D/A converters and filters for communication systems have been usually realized by switched capacitor techniques. SC circuits have been traditionally integrated in nonstandard processes, basically due to the demand for linear capacitors. Presently, CMOS analog arrays are available for the integration of SC circuits in double-poly technology [6]. In this solution, however, the area occupied by the double-poly capacitors cannot be used for other ends, usually resulting in inefficient area realizations of mixed mode circuits. Attempts have also been made to integrate SC filters using the linear capacitors (metal-metal or metal-poly) available in standard digital processes [7]. In this case, the conclusion has also been that merging analog and digital circuits in the same chip leads to an excessive price to be paid in silicon real estate.

One alternative approach, not yet explored for gate array implementation of SC circuits, has been proposed [8] in which linear capacitors are realized by biased MOSFET gates. Nevertheless, a proper evaluation of this possibility depends on the determination of the output harmonic distortion of an SC filter due to the use of this type of capacitors. A detailed analysis of SC filters built with MOSFET capacitors is presented in this paper. It is shown that the output harmonic distortion is predictable from the knowledge of the capacitance nonlinearities and from the transfer function of the linearized network.

ANALYSIS OF SC FILTERS IMPLEMENTED WITH NONLINEAR CAPACITORS

In the following analysis, SC networks implemented with ideal op amps, ideal switches and nonlinear capacitors are considered. It will also be assumed that the same function f[v] can be used to model the nonlinearities of all capacitors in the network [10], a condition that can be accurately fulfilled in an integrated circuit. Under this assumption, the carge stored at time t=nT in a given capacitor C_A, having a voltage v(nT) across its terminals, is given by

$$q_A = C_A.v(nT) = C_{Ao}.f[v(nT)].v(nT) \qquad (1)$$

To avoid cumbersome notations, the following development is based on a second order SC network. Nevertheless, the conclusions reached are valid for networks of any order, as will soon become clear.

In the network shown in Fig.1, the capacitor plates have been biased using the scheme presented in [8]. Writing the charge conservation equations around the DC operating point and expressing the capacitance charges as in (1) yields, at t=nT (even phase),

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$$-C_{Jo}.f[v_1(nT-T/2)].v_1(nT-T/2) - C_{Ao}.f[v_3(nT-T)].v_3(nT-T)$$

$$= -C_{Bo}.f[v_2(nT)].v_2(nT) + C_{Bo}.f[v_2(nT-T)].v_2(nT-T) \quad (2a)$$

$$C_{Co}.f[v_2(nT)].v_2(nT) + C_{Lo}.f[v_3(nT)].v_3(nT) =$$

$$-C_{Do}.f[v_3(nT)].v_3(nT) + C_{Do}.f[v_3(nT-T)].v_3(nT-T) \quad (2b)$$

In the general case, this is a system of nonlinear equations on the node voltages. However, performing the change of variable [11]

$$u_i(\cdot) = f[v_i(\cdot)].v_i(\cdot) \quad (3)$$

system (2) is transformed into a set of linear equations on the variables $u_i(\cdot)$, as follows:

$$-C_{Jo}u_1(nT-T/2) - C_{Ao}u_3(nT-T) = -C_{Bo}u_2(nT) + C_{Bo}u_2(nT-T) \quad (4a)$$

$$C_{Co}u_2(nT) + C_{Lo}u_3(nT) = -C_{Do}u_3(nT) + C_{Do}u_3(nT-T) \quad (4b)$$

Applying the z-Transform to both equations and solving for the transform $U_3^e(z)$ of the output variable yields the transfer function

$$H_u(z) = \frac{U_3^e(z)}{U_1^o(z)} =$$

$$\frac{-C_{Jo}C_{Co}z^{-1/2}}{C_{Bo}(C_{Lo}+C_{Do})+(C_{Ao}C_{Co}-2C_{Bo}C_{Do}-C_{Bo}C_{Lo})z^{-1}+C_{Bo}C_{Do}z^{-2}} \quad (5)$$

Regarding this transfer function, it is important to note that its expression is exactly the same of the transfer function $H(z)=V_3^e(z)/V_1^o(z)$ of the same network implemented with linear capacitors. Therefore, since $u_i(\cdot)=f[v_i(\cdot)].v_i(\cdot)$, the nonlinearity of the relationship between $v_1(\cdot)$ and $v_3(\cdot)$ is due exclusively to the nonlinearities of the capacitances connected to the input and to the output of the network.

The above results can be extended to all SC networks for which the variable transformation (3) is applicable [11]. Such networks satisfy the following topological constraint: "after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage". This class clearly includes the large majority of practical SC networks.

Hence, for an Nth order filter, expression (5) assumes, aside from a possible half period delay, the general form

$$H_u(z) = \frac{U_{out}(z)}{U_{in}(z)} = \frac{\sum_{i=1}^{N} n_i z^{-i}}{\sum_{i=1}^{N} d_i z^{-i}} \quad (6)$$

HARMONIC DISTORTION DUE TO CAPACITORS NONLINEARITIES

From (6), the time-domain behavior of SC networks satisfying the aforementioned topological constraints will be described, in terms of the new variable u(nT), by a linear difference equation of the form

$$\sum_{i=1}^{N} d_i u_{out}(nT-iT) = \sum_{i=1}^{N} n_i u_{in}(nT-iT) \quad (7)$$

which, according to (3), implies the following voltage nonlinear difference equation:

$$\sum_{i=1}^{N} d_i f[v_{out}(nT-iT)]v_{out}(nT-iT) = \sum_{i=1}^{N} n_i f[v_{in}(nT-iT)]v_{in}(nT-iT) \quad (8)$$

To determine the output voltage harmonic distortion, (8) must be solved for an input signal $v_{in}(nT) = V_m\cos(\omega_o nT)$. Considering weak nonlinearities, the following simplifying assumptions can be made [10]:

a) The nonlinear function f[v] can be described by a Taylor series, i.e.,

$$f[v] = 1 + \sum_{\ell=1}^{\infty} \alpha_\ell . v^\ell \quad (9)$$

b) The terms of the series expansion responsible for the nonlinearities satisfy

$$\sum_{\ell=1}^{\infty} |\alpha_\ell . v^\ell| << 1 \quad (10)$$

for both the input and output voltages. Under this assumption, the fundamental frequency component at the output, $V_1\cos(\omega_o nT+\phi_1)$, can be approximated by the output of the ideal linear circuit. Hence,

$$V_1 \cong V_m|H(e^{j\omega_o T})| \quad , \quad \phi_1 \cong \text{phase of } H(e^{j\omega_o T}) \quad (11)$$

The nonlinear terms $\alpha_\ell[v_{out}(nT-iT)]^{\ell+1}$ in (8) can be approximated substituting v_{out} by the ideal linear circuit output voltage:

$$\alpha_\ell V_1^{\ell+1}[\cos(n\omega_o T - i\omega_o T + \phi_1)]^{\ell+1} \quad (12)$$

Substituting (9), (11) and (12) in (8) leads, after some algebraic manipulations, to the expression for the output distortion due to the usually dominant 2nd harmonic:

$$HD_2 = \frac{V_2}{V_1} = \left| a_2(V_m)\frac{H(e^{2j\omega_o T})}{|H(e^{j\omega_o T})|} - a_2(V_1)\frac{H^2(e^{j\omega_o T})}{|H(e^{j\omega_o T})|^2}\right| \quad (13)$$

where $a_2(V)$ is a nonlinear function defined by:

$$a_2(V)=\frac{\alpha_1 \cdot V}{2}\binom{2}{0}+\frac{\alpha_3 \cdot V^3}{2^3}\binom{4}{1}+\frac{\alpha_5 \cdot V^5}{2^5}\binom{6}{2}+\ldots \qquad (14)$$

Expressions (13) and (14) provide a very simple way to evaluate the second harmonic distortion at the output of the SC filter. The only informations required are the transfer function of the corresponding linear network and the coefficients (α_i's) expressing the capacitance nonlinearities.

EXPERIMENTAL VERIFICATION

The second order lowpass SC network of Fig.1 has been implemented as a discrete protoptype. As nonlinear capacitors, the capacitances from gate to the short-circuited source and drain terminals of well matched Motorola P5N40 power transistors have been used. A reference voltage V_R=-4V has been employed to obtain the same voltage capacitance coefficient of an integrated gate capacitor, inside an n-well and biased in accumulation with V_{GS}=2.5V [9]. The op amps used were 741 and the switches were 4066.

Fig.2 presents both the theoretical and experimental harmonic distortions at the inverting (v_3) and noninverting (v_2) outputs. In the experiments, only the second harmonic has been detectable. Hence, the theoretical results have been determined from expression (13), with $a_2(V) \cong 1/2\ \alpha_1 . V$, $\alpha_1 = 0.0045V^{-1}$ and with the transfer functions evaluated using the nominal capacitance values:

$$H_{inv}(z) = \frac{-0.08333}{1.33333 - 2.25\ z^{-1} + z^{-2}}\ z^{-1/2} \qquad (15)$$

$$H_{ninv}(z) = \frac{0.33333 - 0.25\ z^{-1}}{1.33333 - 2.25\ z^{-1} + z^{-2}}\ z^{-1/2} \qquad (16)$$

An interesting point to be observed is that the noninverting output presents a distortion substantially smaller than the inverting one. This is explained by the fact that, for the noninverting output, $V_1 \cong V_m$ and $H(e^{j2\omega_o T}) \cong H(e^{j\omega_o T}) \cong 1$ for ω close to zero and, therefore, from (13), $HD_2 \cong 0$.

CONCLUSIONS

An explicit formula for the harmonic distortion due to weak nonlinearities of the capacitors in SC filters has been presented. It has been shown that the harmonic distortion is predictable from the knowledge of the capacitances nonlinearities and from the transfer function of the same filter implemented with linear capacitors. Unlike numerical methods, this formula provides direct information about harmonics as a function of the frequency. Experimental and theoretical results indicated that harmonic distortion as low as -40dB to -60dB can be obtained in SC filters with capacitors implemented by MOSFET gates. These results show the possibility of the implementation of mixed analog/digital circuits using presently available CMOS gate arrays and, hence, benefiting from the advantages inherent to this type of implementation.

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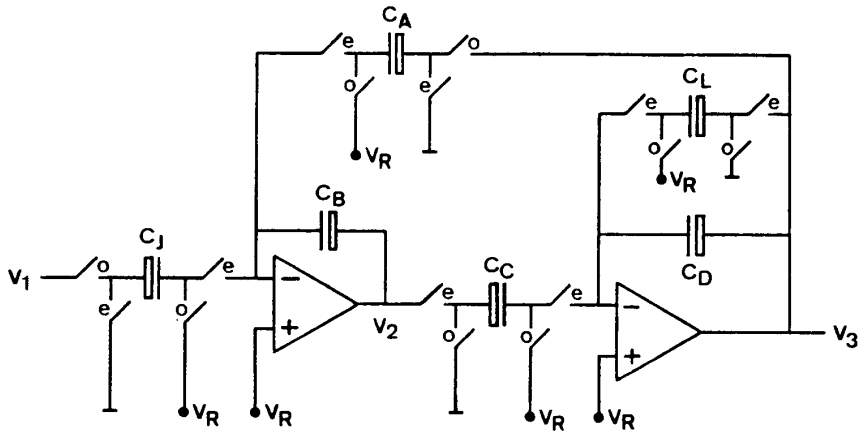

Fig.1. Prototype SC filter

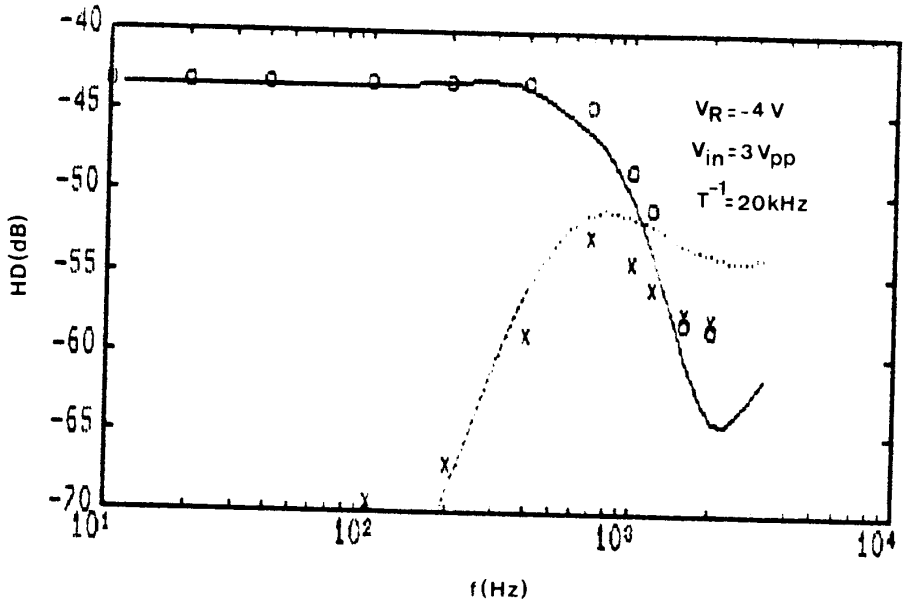

Fig.2. Second order harmonic distortion at

a) inverting output (V_2)

——— theoretical

x experimental

b) noninverting output (V_1)

------- theoretical

o experimental