LINEARITY OF SWITCHED CAPACITOR FILTERS EMPLOYING NONLINEAR CAPACITORS

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Abstract: This paper demonstrates the compatibility of SC filters with VLSI processes. Conditions to obtain linear and precise input-to-output voltage relationships in networks containing nonlinear capacitors are derived. Satisfied these conditions, considerations about the alternatives for capacitor implementations show the feasibility of the integration of SC filters in any digital MOS process.

I- INTRODUCTION

Due to the continuous advances in VLSI, the majority of the presently available integrated circuit technologies are optimized for digital circuits. This fact indicates a clear tendency towards a digital implementation of signal processing systems. On the other hand, analog circuits will always be required to interface the digital system with the physical world [1]. Consequently, most modern integrated systems are predominantly digital, with the analog part occupying only a small fraction of the total chip area. In these cases, economical reasons require the analog circuits to be fully compatible with a digital process.

The most successful method to realize analog functions in CMOS technology has been, for many years, the well established switched capacitor (SC) technique. Switched capacitor systems have been traditionally integrated in nonstandard MOS processes, basically due to the demand for linear capacitors. Attempts have also been made to integrate SC filters with linear capacitors available in standard digital processes [2]. The usual conclusion has been, however, that the price to be paid in silicon real estate was excessive [1,2]. More recently, a new design technique, denominated switched current (SI), has been actively pursued. One of the main driving forces behind the development of this new technique has been exactly the consideration that SC circuits do not fit standard VLSI processing [3].

The objective of this paper is to demonstrate the compatibility of SC circuits with VLSI processes. It is shown that, satisfying some trivial requirements, SC circuits containing nonlinear capacitors can realize linear charge processors, exactly in the same way SI circuits can be designed as linear current processors. Moreover, it is shown that highly linear and precise SC voltage processors can be realized using any digital MOS technology.

II- SC CIRCUITS AS CHARGE PROCESSORS

Sampled-data analog signal processing requires four basic operations: inversion, addition, multiplication and delay. In SI circuits, these operations are accomplished by switched current mirrors [3,4]. These mirrors realize a nonlinear I-V conversion followed by an inverse V-I conversion, leading to a linear relationship between input and output currents (Fig. 1(a)). Obviously, the mirror concept is not limited to the current variable. The basic cell of an SC circuit can be interpreted as a charge mirror composed of capacitors which may be even nonlinear.

In Fig. 1(b), suppose an ideal operational amplifier (op amp). If a charge q_A has been injected into the inverting input, its relationship with the voltage v at the output terminal is given by

$$q_A = C_A.v = C_{Ao}.f_A[v].v \qquad (1)$$

Here, $f_A[v]$ is a dimensionless function describing the nonlinearity of the capacitor C_A [5]. This nonlinearity depends on the structure of the capacitor and can be considered to be equal for capacitors with the same structure and physically close to each other in a chip. The parameter C_{Ao} is the capacitance value for a signal voltage v equal to zero, being proportional to the capacitor area. Likewise, the charge in C_B (Fig. 1(b)) can be written as

$$q_B = C_B.v = C_{Bo}.f_B[v].v \qquad (2)$$

If the nonlinearities of C_A and C_B are equal,

$$\frac{q_B}{q_A} = \frac{C_{Bo}}{C_{Ao}} = \frac{\text{Area}(C_B)}{\text{Area}(C_A)} \qquad (3)$$

Therefore, under this assumption the basic block in Fig 1(b) performs as a (linear) charge mirror with gain defined by a geometrical ratio and, consequently, independent of the technology.

Based on the above considerations, it is clear that both SI and SC circuits can employ nonlinear elements (transistors in SI circuits and capacitors in SC circuits) and still maintain linearity from

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input to output. If the external quantity is a voltage signal, linear input V-Q and output Q-V converters are then required for SC circuits, exactly as linear V-I and I-V converters are required for SI circuits.

III- REALIZATION OF LINEAR VOLTAGE PROCESSORS

For simplicity, we consider here the class of SC networks satisfying the following topological constraint: *"after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage"*.

This topological property is intrinsic to the great majority of stray insensitive SC networks and, therefore, its assumption does not represent any serious practical limitation.

Consider the SC lowpass filter shown in Fig.2. This network clearly satisfies the required topological constraint. For linear capacitors, $f[v(\cdot)]$ introduced in (1) is equal to one. Then, the charge conservation equations (CCEs) at the virtual grounds are given by

$$-C_{Io}v_I(nT-T/2) + C_{Eo}v_A(nT) + C_{Fo}v_B(nT) = -C_{Ao}v_A(nT) + C_{Ao}v_A(nT-T) \quad (4.1)$$

$$-C_{Go}v_A(nT-T) = -C_{Bo}v_B(nT) + C_{Bo}v_B(nT-T) \quad (4.2)$$

$$C_{Ho}v_B(nT) + C_{Jo}v_C(nT) + C_{Do}v_A(nT) - C_{Do}v_A(nT-T) = -C_{Co}v_C(nT) + C_{Co}v_C(nT-T) \quad (4.3)$$

Equations (4) can also be written in terms of the charges in the capacitors C_I, C_A, C_B, and C_C. Performing the change of variables yields

$$-q_I(nT-T/2) + \frac{C_{Eo}}{C_{Ao}}q_A(nT) + \frac{C_{Fo}}{C_{Bo}}q_B(nT) = -q_A(nT) + q_A(nT-T) \quad (5.1)$$

$$-\frac{C_{Go}}{C_{Ao}}q_A(nT-T) = -q_B(nT) + q_B(nT-T) \quad (5.2)$$

$$\frac{C_{Ho}}{C_{Bo}}q_B(nT) + \frac{C_{Jo}}{C_{Co}}q_C(nT) + \frac{C_{Do}}{C_{Ao}}q_A(nT) - \frac{C_{Do}}{C_{Ao}}q_A(nT-T) = -q_C(nT) + q_C(nT-T) \quad (5.3)$$

Equations (5) are represented by the signal flow graph (SFG) of the Q-processor in Fig.3, where the branch transmittances are proportional to the gains of the charge mirrors. The input V-Q and output Q-V conversions are also shown.

Consider now the same network with nonlinear capacitors. If all capacitors connected to the same op amp output have identical nonlinearities (linear charge mirrors), a condition that can be accurately fulfilled in an integrated circuit, the CCEs will be given by

$$-C_{Io}f_I[v_I(nT-T/2)].v_I(nT-T/2) + C_{Eo}f_A[v_A(nT)].v_A(nT) + C_{Fo}f_B[v_B(nT)].v_B(nT) = -C_{Ao}f_A[v_A(nT)].v_A(nT) + C_{Ao}f_A[v_A(nT-T)].v_A(nT-T) \quad (6.1)$$

$$-C_{Go}f_A[v_A(nT-T)].v_A(nT-T) = -C_{Bo}f_B[v_B(nT)].v_B(nT) + C_{Bo}f_B[v_B(nT-T)].v_B(nT-T) \quad (6.2)$$

$$C_{Ho}f_B[v_B(nT)].v_B(nT) + C_{Jo}f_C[v_C(nT)].v_C(nT) + C_{Do}f_A[v_A(nT)]v_A(nT) - C_{Do}f_A[v_A(nT-T)].v_A(nT-T) = -C_{Co}f_C[v_C(nT)].v_C(nT) + C_{Co}f_C[v_C(nT-T)].v_C(nT-T) \quad (6.3)$$

Expressing, as done for the linear network, the CCEs in terms of the charges in the capacitors C_I, C_A, C_B and C_C, the same set of linear equations (5) is obtained. This shows that, provided some simple conditions are satisfied, an SC network containing nonlinear capacitors can realize a linear charge processing. Furthermore, the expression of its charge transfer function will be equal to that of the same network with linear capacitors. Moreover, this charge transfer function is proportional to the voltage transfer function of the linear network. It can be verified from the SFG of Fig.3 that

$$\frac{V_C^e(z)}{V_I^o(z)} = \frac{C_{Io}}{C_{Co}} \cdot \frac{Q_C^e(z)}{Q_I^o(z)} \quad (7)$$

Since $Q_I^o(z)=\mathcal{Z}\{C_{Io}.f_I[v_I(nT-T/2)].v_I(nT-T/2)\}$ and $Q_C^e(z) = \mathcal{Z}\{C_{Co}.f_C[v_C(nT)].v_C(nT)\}$, a linear input-output voltage relationship will exist if $f_C[v_C(\cdot)] = f_I[v_I(\cdot)] = 1$. This requirement is satisfied if the capacitors connected to the input and to the output network nodes are linear. For all the remaining capacitors, the only existing requirement is that those connected to the same op amp output must present equal nonlinearities, what is equivalent to the implementation of linear charge mirrors. Satisfied these requirements, the right hand side of (7) represents also the voltage transfer function of the nonlinear network.

Summarizing, we state here a set of sufficient conditions to implement a linear input-output voltage relationship with an SC network containing nonlinear capacitors.

Condition 1: The network topology must satisfy the constraint that, after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage.

Condition 2: All capacitors connected to the same op amp output must present identical nonlinearities, expressed by the function $f_X[v_X]$, v_X the voltage at that output node.
Condition 3: Only the capacitors connected to the input and output nodes need to be implemented as linear capacitors, regardless of the order or the topology of the network.

IV- IMPLEMENTATION ISSUES

As pointed out previously, SC filters implemented with nonlinear capacitors and satisfying conditions 1 to 3 are actually linear charge processors with linear input V-Q and output Q-V converters. For charge processing, precision is guaranteed by satisfying condition 2 and by geometrically matching the capacitors connected to the same op amp output. For voltage processing, (7) shows that any mismatch between the input and output capacitors will cause only a voltage gain error, usually not a major drawback. For networks containing more than one input branch, all input capacitors must be matched to ensure the precise realization of the transmission zeros of the voltage transfer function. If the SC filter has too many capacitors connected to the input and output nodes, the linear V-Q and Q-V conversions can be realized by using amplifier stages at both ends, bringing the required number of linear capacitors down to two or three.

For the implementation of the nonlinear capacitors, the natural choice is to use a MOSFET gate structure. Compared with double-poly capacitors, gate capacitors present a larger capacitance per unit area and are expected to have better matching properties [6,7].

To implement the few required linear capacitors, discrete components could be used. For a fully integrated implementation, two main alternatives are available. One is the use of aluminium-poly [1,2] or aluminium-aluminium capacitors which, despite their low specific capacitances, may represent a solution to implement few capacitors. The other alternative is the MOSFET gate structure biased in accumulation or strong inversion [8]. Such capacitors may represent a good choice for many low distortion applications. This alternative is the topic of a current investigation which will be the subject of a future publication.

V- EXPERIMENTAL RESULTS

Fig.4 presents the total harmonic distortion measured at the op amp outputs of a third order cascade lowpass SC filter satisfying conditions 1 to 3. At least a 30dB improvement can be verified from the internal nodes to the output node. Fig. 5 shows the waveforms at an internal node and at the output, for a sinusoidal input signal.

VI- CONCLUSIONS

Full compatibility of SC filters with VLSI processes has been demonstrated. To this end, the conditions for linear charge and voltage processing have been derived. Considerations about precision of the transfer function coefficients and about the alternatives for capacitor implementations show the feasibility of high-precision, low-distortion SC filters, integrated in any digital MOS process.

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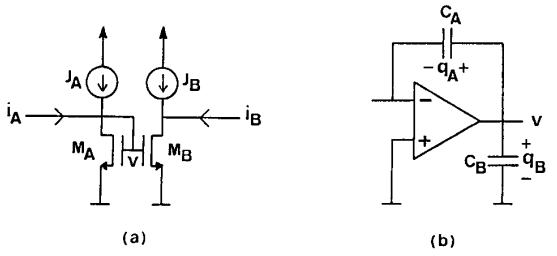


Fig.1- (a) Current mirror. (b) Charge mirror.

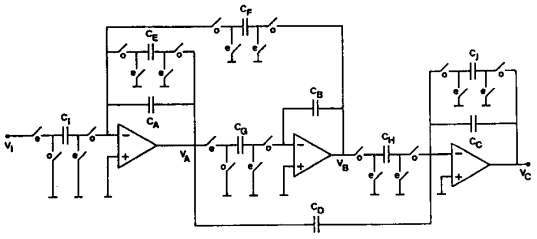


Fig.2- Third order lowpass SC filter.

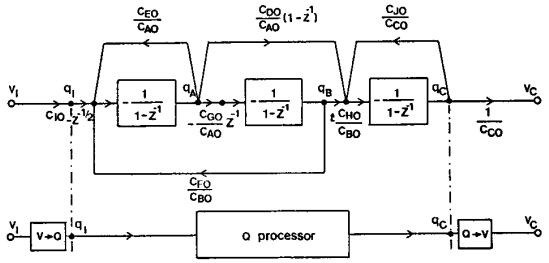
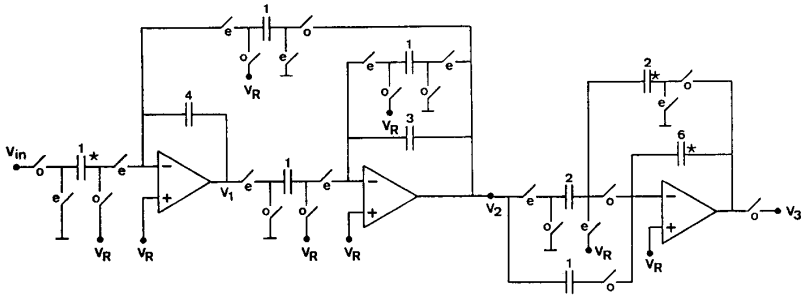


Fig.3- SFG of the SC filter in Fig.2.



* Linear Capacitors

Prototype SC filter

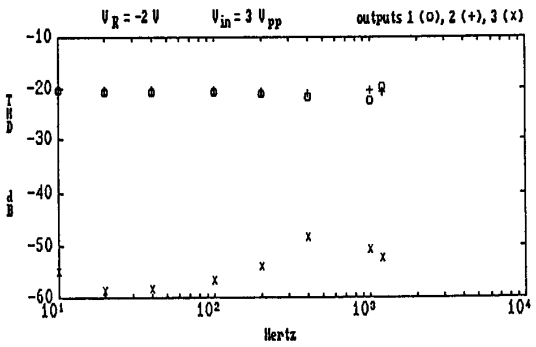


Fig.4- THD at the op amp outputs of the prototype SC filter.

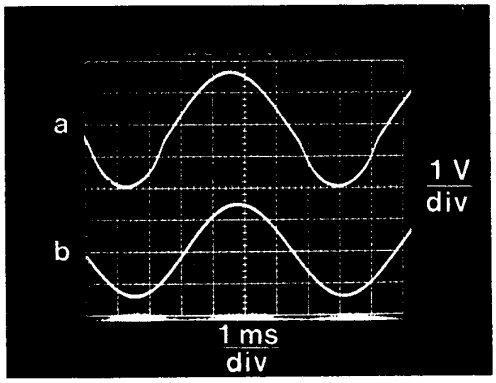


Fig.5- Measured output waveforms. (a) intermediate node. (b) output node.