NONLINEARITIES OF CAPACITORS REALIZED BY MOSFET GATES

A.T.Behr, M.C.Schneider, S.Noceti Filho, and C.G.Montoro.

Laboratório de Instrumentação Eletrônica - LINSE/EEL/CTC/UFSC/C.P. 476
CEP 88049 - Florianópolis - SC - Brasil
Telex 240 UFSC BR Fax 55-0482-341524
Tel. 55-0482-319504/319643 e-mail: LINSE@BRUFSC.BITNET

Abstract: The capacitive gate structures available in digital oriented CMOS processes are reviewed, with emphasis on their use as linear capacitors. Experimental and analytical results indicate that the total harmonic distortion in an adequately biased (2.5V) gate capacitor can be kept low (THD < -40 dB for a 3V voltage swing).

INTRODUCTION

For economical reasons, the analog part of a system-on-a-chip must be fully compatible with standard VLSI processes [1]. Most analog applications require high-quality capacitors, usually obtained through a nonconventional process, with the double-polysilicon option being the most frequently used.

One way to avoid the need for nonstandard processes to implement linear capacitors is through the use of the MOSFET gate structure, the intrinsic element of any MOS technology. Compared with double-poly capacitors, thin oxide capacitors present a larger capacitance per unit area and are expected to have better matching properties [2]. By properly biasing this device, a capacitor with weak nonlinearities is accomplished which is, however, much more voltage-dependent than the double-poly capacitor.

Some authors have described the use of gate capacitors in analog applications as, for example, in transconductance-C [3], transistor-only [4,5] and switched capacitor [6] filters. Despite the reported use of the gate structure in many analog applications, a more detailed analysis of this capacitor is necessary for the understanding of the impact of its use in practical filters.

The purpose of this paper is to evaluate the behavior of MOS gates as lumped capacitors. To this end, the capacitive structures available in CMOS technology are reviewed. An accurate model of the gate capacitance together with a numerical analysis and a design-oriented expression of the voltage harmonic distortion are presented. Finally, experimental data measured on an integrated capacitor are shown.

GATE STRUCTURES IN CMOS TECHNOLOGY

Fig. 1 shows 4 gate structures that can be employed as capacitors in a p-well CMOS process. The first two (1(a) and 1(b)) must operate in accumulation while the last two must be biased in strong inversion. The device in Fig. 1(a) can act as a floating capacitor. Fig. 1(b) shows an AC grounded capacitor. The device in Fig. 1(c) can be shielded from substrate noise by applying a fixed potential to the well, while the one shown in Fig. 1 (d) is a floating capacitor also available in a single channel technology.

Usually, some simple expressions are given for the intrinsic gate capacitance in strong inversion, for $V_{DS} = 0$:

$$C_{gs} = C_{gd} \cong \frac{1}{2} Cox; \quad C_{gb} \cong 0 \qquad (1a)$$

Moreover, in accumulation:

$$C_{gs} = C_{gd} = 0 \quad \text{and} \quad C_{gb} = C_{ox} \qquad (1b)$$

where Cox is the thin oxide intrinsic capacitance. The other intrinsic capacitances, C_{bs} and C_{bd} , are nonlinear [7] and depend on V_{BS} .

For the purpose of getting a nearly voltage-independent capacitance, a voltage bias must be provided to the MOS gate to keep it in accumulation or strong inversion. This is easy to realize for grounded and virtually grounded capacitors, as in the OTA-C and SC integrators shown in Fig. 2.

ACCURATE MODEL OF THE GATE CAPACITANCE

Most analytical models of the MOSFET are based on the charge sheet approximation, in which the thickness of the surface channel (in inversion or accumulation) is neglected [7]. For these models the gate-to-source capacitance (C_{gs}) is constant for $V_{DS} = 0$. So, in order to calculate the weak nonlinear behavior of gate capacitors in inversion and accumulation, an approach based on fundamental equations of the MOS structure must be followed.

0-7803-0593-0/92 $3.00 1992 IEEE

For the three terminal n-channel MOS structure, the voltage and electrical charge in terms of the surface potential (ψ_s) are given by the well-known expressions, valid for nondegenerate silicon [7]:

$$V_{GB} = V_{FB} + \psi_s - q'_c/C'_{ox} \tag{2}$$

$$q'_c = -\mathrm{sgn}(\psi_s)\,(2q\varepsilon_s N_A \phi_t)^{0.5}\cdot f(\psi_s) \tag{3}$$

where $f(\psi_s) = \left\{ e^{\frac{-\psi_s}{\phi_t}} + \frac{\psi_s}{\phi_t} - 1 + e^{\frac{\psi_s-(2\phi_F + V_{SB})}{\phi_t}} \right\}^{0.5}$,

V_{GB} is the gate-to-bulk voltage, q'_c is the total semiconductor charge per unit area and C'_{ox} is the oxide capacitance per unit area. The other variables have their usual meanings [7].

The total small signal gate capacitance per unit area is given by

$$C'_g = \frac{dq'_G}{dV_{GB}} = -\frac{dq'_c}{dV_{GB}} \tag{4}$$

where $C'_g = C'_{gs} + C'_{gd} + C'_{gb}$ if $V_{BS} = V_{DS} = 0$.

As previously stated, the gate structure should be biased in strong inversion or accumulation in order to obtain a nearly voltage-independent capacitance. So, the voltage harmonic distortion in these two regions will be analitically determined for $V_{BS} = V_{DS} = 0$.

a)**Strong inversion:** For $\psi_s \geq 2\phi_F$ the term $e^{-\psi_s/\phi_t}$ can be neglected in (3). From (2), (3) and (4), the value of C'_g at a bias voltage V_{GB} can be approximated by:

$$\frac{1}{C'_g} \cong \frac{1}{C'_{ox}}\left(1 + \frac{2\phi_t}{V_{FB} + \psi_s - V_{GB}}\right) \tag{5}$$

In analog circuits the MOS capacitor is typically driven by a charge source, as in SC circuits, or by a current source, as in OTA-C networks. From expressions (2), (4), (5) and assuming ψ_s constant, it can be shown that the second order harmonic distortion of the voltage, for a sinusoidal charge, is given by

$$\text{2ND HARM DIST} \cong \frac{\phi_t \cdot V_P}{2(V_R - V_{FB} - \psi_s)^2} \tag{6}$$

where V_R and V_P are the bias and peak values of the gate-to-bulk voltage, respectively, and $\psi_s \cong 2\phi_F$.

b) **Accumulation region:** If $\psi \leq 0$ equations (5) and (6) still hold, with $\psi_s \cong 0$.

EXPERIMENTAL RESULTS

A test-capacitor, made up of 500 thin oxide unity capacitors of 40 μm x 40 μm, has been fabricated in a 2μm CMOS n-well process. The main electrical parameters concerning the available CMOS process are a specific capacitance of 0.86 fF/μm^2, a well doping concentration of 1.9×10^{16} cm^{-3} and a threshold voltage of -0.6V for the PMOS transistor.

The experimental C-V characteristic of the test structure with source and well short-circuited, together with the theoretical C-V characteristic, are shown in Fig. 3. The latter was plotted from the data obtained by using expressions (2)-(4) and the typical values of process parameters referred to before. The difference between experimental and theoretical capacitance data in the depletion region (near the minimum of the capacitance curve) is explained by the nonuniform doping profile of the well.

Fig. 4 displays the total harmonic distortion (THD) experimentally measured,its values computed from Fourier analysis based on expressions (2)-(3) and the second harmonic relative magnitude computed from equation (6). Spectral analysis has revealed that the second order harmonic is the main responsible for distortion. It should be noted that for a 2.5V bias, the peak to peak signal in the MOS gate can be about 4V (in accumulation) and the THD remains below -40 dB. For a 5V bias the peak to peak signal can be about 9V for achieving a THD close to -40 dB. Similar results also apply to the strong inversion region (Fig. 4 (b)).

CONCLUSIONS

In spite of being a nonlinear element, the gate structure of the MOS transistor biased in inversion or accumulation provides a capacitance with the following advantages over double-poly capacitors: higher capacitance per unit area, better matching and full compatibility with any digital MOS process.

Harmonic distortion in gate capacitors is almost independent of technological parameters provided that they are biased in accumulation or strong inversion. Moreover, the approximate formula presented for the harmonic distortion can help the circuit designer predict a maximum voltage swing in order to maintain the THD at acceptable levels.

Analytical and experimental results have demonstrated that the THD can be lower than 1% for a voltage swing approximating the power supply voltage. Hence, for many applications, the harmonic distortion introduced by the weak nonlinearities of biased MOS gate capacitors can be kept low with little penalty in signal swing.

ACKNOWLEDGEMENT

The authors would like to thank F. Reichert from ELETROSUL for his help in measurements. They also acknowledge R. T. Gonçalves for devices characterization, Prof. A. Perin for his cooperation and Prof. J.C.M.Bermudez for valuable discussions.

REFERENCES

[1] E. Vittoz, "The design of high-performance analog circuits on digital CMOS chips", IEEE J. Solid-State Circuits, Vol. SC-20, no.3, pp. 657-665, June 1985.

[2] D.J. Allstot and W. Black, "Technological design considerations for monolithic MOS switched-capacitor filtering systems", Proc. of the IEEE, Vol. 71, no. 8, pp. 967-986, August 1983.

[3] M.A. Tan , and R. Schaumann, "Simulating general-parameter LC-ladder filters for monolithic realizations with only transconductance and grounded capacitors ", IEEE Trans. on Circuits and Systems, Vol. CAS-36, no. 2, pp. 299-307, February 1989.

[4] L. Pu and Y. Tsividis, "Transistor-only frequency-selective circuits", IEEE J. Solid-State Circuits, Vol. SC-25, no. 3, pp. 821-832, December 1990.

[5] S.T. Dupuie, S. Bibyk and M. Ismail, "A novel all-MOS high-speed continuous-time filter", Proc. of the International Symposium on Circuits and Systems, Portland, USA, pp. 675-678, 1989.

[6] C.G. Montoro and J.C.M. Bermudez, Switched-capacitor circuits fully compatible with digital Si-gate single poly technology, Proc. of the 31st Midwest Symposium on Circuits and Systems, St. Louis, USA, pp. 1-3, 1988.

[7] Y. Tsividis, *Operation and modeling of the MOS transistor*, New York, McGraw-Hill, 1987.

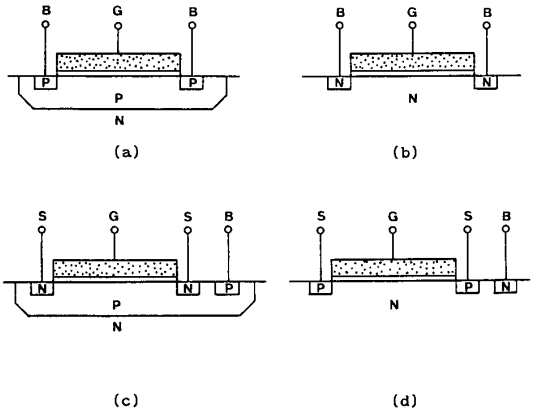

Fig. 1 - Gate structures in a p-well CMOS technology

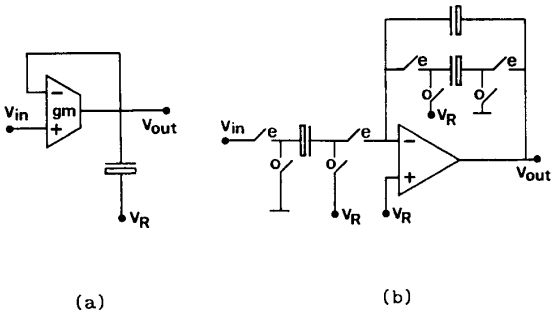

Fig. 2 - Bias schemes for a lossy integrator. All capacitors have a DC operating point equal to V_R
(a) OTA-C; (b) switched-capacitor [6].

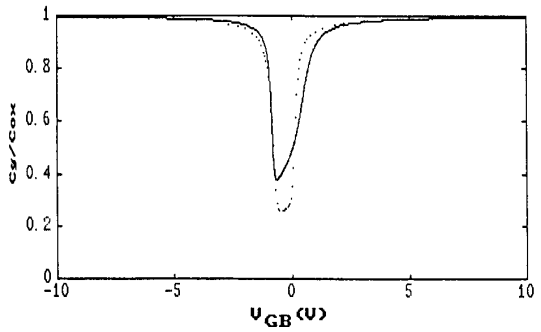

Fig. 3 - C-V characteristic of the test-capacitor
——— theoretical
..... experimental

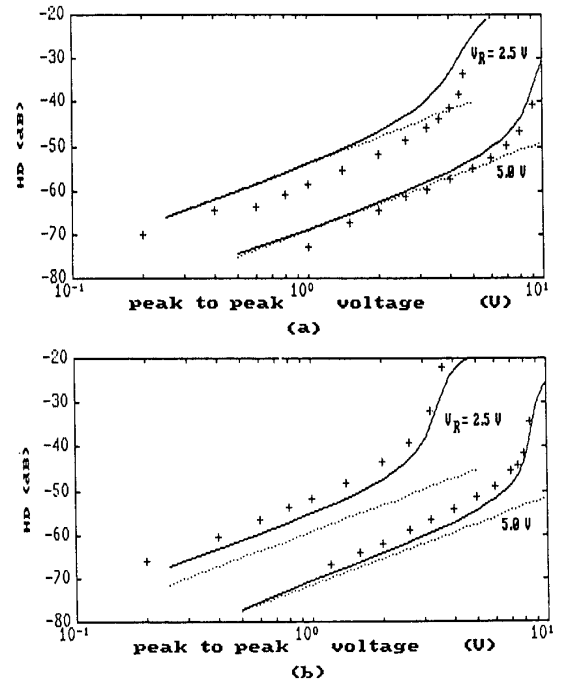

Fig.4 - Harmonic distortion for a measurement frequency of 2.5 KHz.
(a) accumulation (b) inversion
theoretical expression (6) for the second harmonic
——— THD computed from expressions (2) and (3)
++++++++ experimental THD