A LINEAR DIFFERENTIAL CMOS VxI CONVERTER

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ABSTRACT

A new CMOS circuit is proposed for the implementation of a linear VxI converter based on the square-law characteristic of MOS transistors. An analysis of the circuit concerning input voltage limits, frequency response and transistor mismatches is presented. Simulation results show that total harmonic distortion of the output current smaller than 1% can be obtained for differential input signals up to 3.8 Vp-p and supply voltages of ± 5V.

INTRODUCTION

Linear VxI transconductors have obtained increasing importance in continuous-time filtering [1,2], particularly in MOS technology. However, in order to obtain linearity of the output current for a reasonable input voltage range, special circuit topologies are required. Many of the good structures presented so far in the literature are based on the circuit shown in Fig. 1 [3-5]. Transistors M1 and M2 are assumed to be matched devices operating in saturation and in strong inversion. Under these conditions the approximate square-law current-voltage characteristic

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad (1)$$

is valid for MOS transistors, if the channel-length modulation effect can be neglected (long channel devices). The differential current $I_0 = I_1 - I_2$ in Fig. 1 can be expressed as [1]

$$I_0 = gm.V \qquad \text{for } |V| \le V_X\ ,\ V = V_1 - V_2 \qquad (2)$$

where $gm = 2\beta V_X$ is the transconductance of the cell and $\beta = \mu_n Cox\ (W/L)_1$. Therefore, satisfied the conditions just mentioned, this approach leads to linear OTA's with large differential input voltage range. The major drawback of the circuit in Fig. 1, however, is the difficulty to implement the floating constant voltage sources. This publication presents a new solution to this problem which allows large differential input signal amplitudes with very small output harmonic distortion.

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Circuit implementation. Fig.2 shows the new circuit proposed for the transconductor. The constant voltage sources are obtained from the gate-to-source voltages of the MOS transistors M3 and M4, which are biased in saturation with a constant current I_B. This is achieved in a very simple way: the drain current I_1 (I_2) of the input transistor M_1 (M_2) is mirrored through M5, M7, M10 and M11 (M6, M8, M13 and M14) and then subtracted at the source node which is common to M1 and M3 (M2 and M4). Consequently, the current through M3(M4) equals I_B and V_{GS3} is a constant whose value is given by

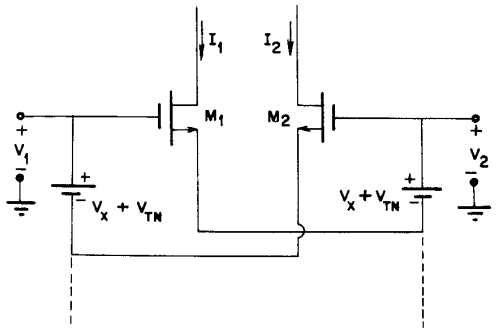


Fig.1 - Basic cell of the linear VxI converter.

$$V_{GS3} = V_X + V_{TN} = (2\ I_B/\beta_3)^{0.5} + V_{TN} \qquad (3)$$

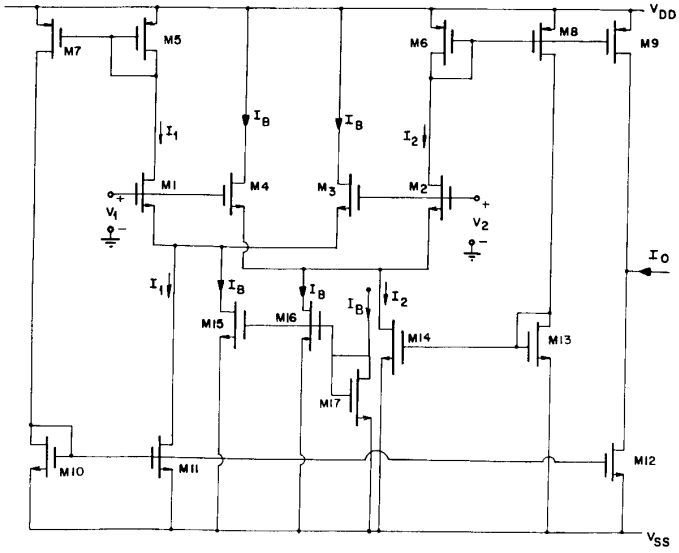
Hence, the value of V_X can be adjusted through the value of the bias current I_B. It should be noted that the proposed technique allows the control of the transconductance gm with process and temperature variations and also provides tuning capability. Furthermore, a high input impedance is obtained.

Input voltage limits. The input voltages V_1 and V_2 in the circuit of Fig.2 must be greater than a minimum value in order to guarantee that both M11(M14) and M15(M16) are in saturation. Also, the maximum values of these input voltages must be limited to keep M1 (M2) in saturation. It can be shown that these two conditions are satisfied, respectively, if

$$V_1 \ge V_X + V_{TN} + V_{SS} + V_X \cdot \max\left[\left(\frac{\beta_3}{\beta_{16}}\right)^{0.5},\ 2\left(\frac{\beta_1}{\beta_{11}}\right)^{0.5}\right] \qquad (4)$$

and

$$V_1 \le V_{DD} + V_{TN} + V_{TP} - 2V_X\left(\frac{\beta_1}{\beta_5}\right)^{0.5} \qquad (5)$$



TRANSISTOR	W(μm)	L(μm)
M1, M2	10	20
M3, M4	20	20
M5 - M9	80	4
M10-M14	40	4
M15-M17	80	20

PARAMETER	NMOS	PMOS	UNITY
VTO	0.8	-0.8	V
TOX	470 E-10	470 E-10	m
UO	600	220	cm^2/Vs
UCRIT	0.93E5	0.85E5	V/cm
VMAX	5 E4	3 E4	m/s
NSUB	6 E15	1.1E15	$1/cm^3$
GAMMA	0.43	0.53	$V^{0.5}$
NEFF	3.3	3.5	—

Fig.2 - CMOS VxI converter with simple current mirrors.

where max $[x_1,x_2]$ denotes the maximum value between x_1 and x_2. Expressions (2), (4) and (5) clearly show that the increase of the maximum allowable differential input voltage (V_X) reduces the common mode input voltage range. This compromise must be kept in mind during the design process.

Transistor mismatching effects. To analyze the consequences of mismatches in the MOS transistors we first consider the basic cell in Fig.1. It is easy to show that:

$$\frac{\Delta I}{I_{omax}} = \frac{\Delta\beta}{4\beta}\left(\frac{V}{V_X}\right)^2 + \frac{1}{2}\left(\frac{V}{V_X}\right)\left[\frac{\Delta\beta}{\beta} + \frac{\Delta V_B - \Delta V_{TN}}{V_X}\right] + \frac{1}{2}\left[\frac{\Delta V_B - \Delta V_{TN}}{V_X}\right] \qquad (6)$$

where $I_{omax} = I_0(V = V_X) = 2\beta V_X^2$ is the maximum output current in the linear range and $V_B = V_X + V_{TN}$. Of course, a more detailed analysis is necessary, since the basic cell in Fig.1 assumes the availability of constant voltage sources. This is clearly an approximation for the circuit in Fig.2. A more precise analysis is possible if the transistor mismatches are considered, as follows. The difference in V_{GS}'s (or V_B's) of M3 and M4 can be expressed as:

$$\frac{\Delta V_B}{V_X} = \frac{1}{2}\left[\frac{\Delta I_{3,4}}{I_B} - \frac{\Delta\beta_{3,4}}{\beta_3}\right] + \Delta V_{TN\ 3,4} \qquad (7)$$

where $\Delta I_{3,4}$ is the difference of currents of M3 and M4, $\Delta\beta_{3,4} = \beta_3 - \beta_4$ and $\Delta V_{TN3,4} = V_{TN3} - V_{TN4}$. The difference $\Delta I_{3,4}$ is given by:

$$\frac{\Delta I_{3,4}}{I_B} = \frac{1}{I_B}\left[\Delta I_B + \frac{\beta_1}{2}\left(V + V_X\right)^2\left(\frac{\Delta\beta_{eq}}{\beta_{eq}}\right) - \frac{\beta_1}{2}\left(-V + V_X\right)^2\left(\frac{\Delta\beta_{eq}}{\beta_{eq}}\right)_2 + r_1\left(V+V_X\right) - r_2\left(-V+V_X\right)\right] \qquad (8a)$$

where

$$\left(\frac{\Delta\beta_{eq}}{\beta_{eq}}\right)_i = \left(\frac{\Delta\beta_P}{\beta_P}\right)_i + \left(\frac{\Delta\beta_N}{\beta_N}\right)_i \quad , i = 1,2 \qquad (8b)$$

is the sum of the relative errors in the current mirrors of I_1 and I_2 and

$$r_i = \left(\beta_1\beta_P\right)^{0.5}\Delta V_{TPi} - \left(\beta_1\beta_N\right)^{0.5}\Delta V_{TNi} \quad i=1,2 \qquad (8c)$$

β_N and β_P are the β's of the N and P current mirrors and ΔV_{TPi} and ΔV_{TNi} represent the mismatches in the threshold voltages of transistors of the same type in the current mirrors of I_1 and I_2. The analysis of expressions (7) and (8) shows that second harmonic distortion is due only to β mismatches. The remaining terms represent a transconductance error and an offset output current.

High frequency limitations. OTA-C filters can have their frequency responses severely degraded if the frequency dependence of the transconductance value is not taken into account in the design [6]. A simplified small-signal analysis of the OTA structure in Fig.2 shows that, under the assumption of dominant pole approximation, a limit for the cutoff (3 dB) frequency of gm, f_{lim}, is given approximately by:

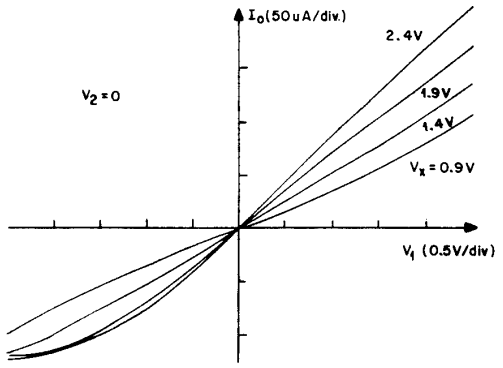


Fig.3 - DC transfer characteristic of the CMOS converter

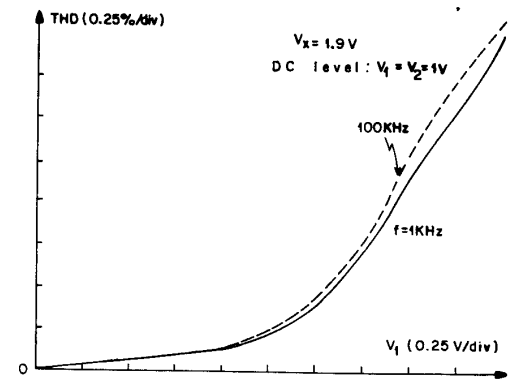


Fig.4 - Total harmonic distortion of the output current versus peak input voltage.

$$\frac{1}{f_{lim}} = \left(\frac{gm_1}{gm_3} + 1\right)\left(\frac{C_N}{gm_N} + \frac{C_P}{gm_P}\right) + \frac{C_P}{gm_3} \qquad (9)$$

Referring to Fig.2, gm_1 and gm_3 are the transconductances of M1 and M3, gm_N and gm_P the transconductances of the NMOS and PMOS transistors of the current mirrors, C_N (C_P) is the sum of the capacitances connected to the common-gate node of the N(P) current mirror and C_S is the total capacitance linked to the source node of the input transistor M1.

Simulation results. The VxI converter in Fig.2 has been simulated using SPICE. For the simulation, the simple current mirrors have been substituted by cascode ones, reducing the errors due to inadequate mirroring. Of course, in this case the allowable input voltage range is reduced, but a smaller total harmonic distortion of the output current is obtained. In SPICE circuit simulations, the electrical parameters and the dimensions shown in Fig.2 have been used, for $V_{DD} = -V_{SS} = 5$ V. Fig.3 shows a plot of the DC transfer characteristic of the converter for various values of the voltage V_X, leading to different transconductance values. It should be noted that, as previously mentioned, the allowable input voltages that assure linearity depend on the value of V_X. Fig.4 shows a plot of the total harmonic distortion versus peak input voltage. The DC level on both input terminals was necessary to ensure that the NMOS transistors of the current mirrors were biased in the saturation region over the entire input voltage range. Simulation results have shown that the total harmonic distortion can be less than 1% if the peak input differential voltage does not exceed the value of V_X, equal to 1.9V in this case. Fig.5 shows the frequency response of the OTA for a bias current equal to 19μA. The maximum gm cutoff frequency predicted by expression (9) was 8.7 MHz while the value measured from Fig.5 was about 6 MHz. Although expression (9) is not precise, it gives a good approximation to predict the influence of this high frequency parasitics on the behavior of OTA-C filters.

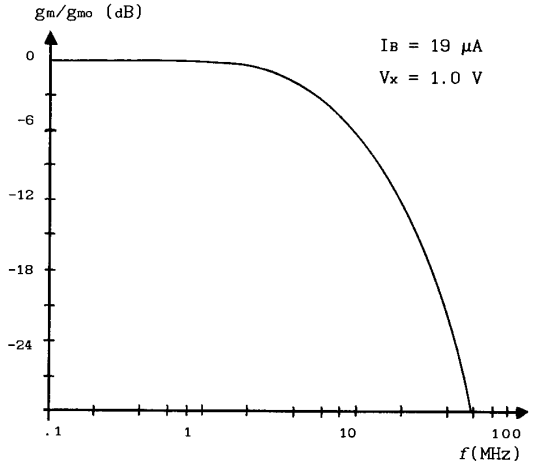


Fig.5 - Frequency response of the operational transconductance amplifier (g_{mo} is the low frequency value of gm).

CONCLUSIONS

A very simple CMOS circuit has been proposed to implement a linear OTA whose transconductance value can be easily adjusted by controlling the bias current. This circuit provides also a mean of obtaining an output current proportional to the square of the differential input voltage [4]. Analysis and simulation results have shown that the proposed circuit can perform as well as or even better than some VxI converters presented in the literature. For example, the OTA presented in ref [3], introduces a more complex circuit to obtain the same transfer function. Also, the allowable common mode input voltage range in the converter suggested here is greater than that presented in ref [4] for the same manufacturing process. It should be emphasized that a careful layout of the circuit must be planned in order to avoid harmonic distortion, specially the second harmonic, due to transistor mismatches.

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