Self-Consistent Models of DC, AC, Noise and Mismatch for the MOSFET

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ABSTRACT

This paper shows how the full compatibility of the ACM model with the quasi-Fermi potential formulation for the drain current allows the derivation of a very simple model of the MOSFET channel. As a result, consistent dc, ac, noise, and mismatch models for all operating modes of the MOSFET are described. Experimental results confirm the accuracy of both mismatch and noise models under various bias conditions.

***Keywords**:* MOSFET, analog design, matching, noise, compact models.

1 INTRODUCTION

Device mismatch and internal noise are accuracy-limiting factors for electronic circuits. Parallelism between the effects of mismatch and noise in circuits have been presented [1], and the limits on minimum power consumption, for a given speed and accuracy, imposed by mismatch and noise have been compared. Moreover, the lower supply voltages of modern MOS technologies contribute to increasing the impact of noise and mismatch on electronic systems.

Models to predict accuracy are fundamental in analog and digital IC design. MOSFET models must be consistent for series-parallel association and predict mismatch or noise under any bias condition. Traditional models are inconsistent, inaccurate, or too complex for predicting mismatch and noise. Simple one-equation models based on physical behaviour, such as the Advanced Compact MOSFET (ACM) model, provide a useful tool for hand design, rather than being restricted to computer simulation. To obtain general results for both mismatch and noise for all MOSFET bias regions we have used ACM to describe the transistor channel. Mismatch (spatial fluctuation) and noise (temporal fluctuation) are similar phenomena, both depending on process, device dimensions, and bias. Mismatch can be seen as a "dc noise".

In this paper, we show that the same formalism of carrier number fluctuation [2] can be applied to model mismatch and low-frequency noise. As a result, the parallelism between noise and mismatch effects at the circuit level will be highlighted. Also, the classical expression for thermal noise is demonstrated to be fully compatible with the result based on fluctuations of channel elements. The expressions for mismatch, flicker and thermal noise, and corner frequency presented here constitute a compact and consistent set of equations, very useful for design purposes.

2 THE ACM MODEL [3]

The fundamental approximation of the ACM model is the linear dependence of the inversion charge density Q'_I on the surface potential ϕ_S, which encompasses the weak, moderate, and strong inversion regions:

$$dQ'_I = \left(C'_b + C'_{ox}\right)d\phi_S = nC'_{ox}d\phi_S \ . \tag{1}$$

Here, n is the slope factor, slightly dependent on the gate voltage and C'_b, C'_{ox} are the depletion and oxide capacitances per unit area. The drain current in a long-channel transistor is calculated with the aid of (1) and the charge-sheet approximation [4]:

$$I_D = \frac{\mu W}{nC'_{ox}}\left(-Q'_I + nC'_{ox}\phi_t\right)\frac{dQ'_I}{dx} \tag{2}$$

where μ is the effective mobility, W is the channel width, and ϕ_t is the thermal voltage.

The other specificity of the ACM model is the use of the unified charge control model (UCCM) [5] to link the carrier charge density with the applied voltages

$$V_P - V_X = \phi_t\left[\frac{Q'_I}{Q'_{IP}} - 1 + \ln\left(\frac{Q'_I}{Q'_{IP}}\right)\right] \tag{3}$$

where $Q'_{IP} = -nC'_{ox}\phi_t$, $V_P = (V_{GB}-V_T)/n$ is the pinch-off voltage, and V_X is the channel potential. As shown in [6], the use of (2) in conjunction with (UCCM) (3) gives

$$I_D = -\mu\frac{W}{dx}Q'_I dV_X \ . \tag{4}$$

Consequently, the ACM model is fully consistent with the quasi-Fermi potential formulation for the drain current [4].

3 CONSISTENT SMALL-SIGNAL MODEL FOR THE MOSFET CHANNEL

The fluctuation of the drain current around its nominal value results from the sum of the contributions of local fluctuations along the channel, whatever their origin. To calculate the effect of local fluctuations on the drain current along the channel, we split the transistor into 3 series elements: an upper transistor, a lower transistor, and a small channel element of length Δx and area $\Delta A = W\Delta x$ (Fig. 1(a)).

Small-signal analysis allows one to calculate the effect of the local current fluctuation ($i_{\Delta A}$) on the drain current deviation (ΔI_d), as shown in Fig. 1(b). The current division between the channel element and the equivalent small-signal resistance of the rest of the channel gives $\Delta I_d = (\Delta x/L) i_{\Delta A}$. This very simple result for the current division, proportional to a geometric ratio, is a consequence of the quasi-Fermi potential formulation for the drain current, i.e., the conductance of the channel element and the transconductances of the upper and lower transistors are proportional to the local charge density. Thus, the square of the total drain current fluctuation is

$$(\Delta I_D)^2 = \sum_L (\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left(\frac{\Delta x}{L} i_{\Delta A} \right)^2 = \frac{1}{L^2} \int_0^L \Delta x (i_{\Delta A})^2 dx \quad (5)$$

since local current fluctuations along the channel are uncorrelated.

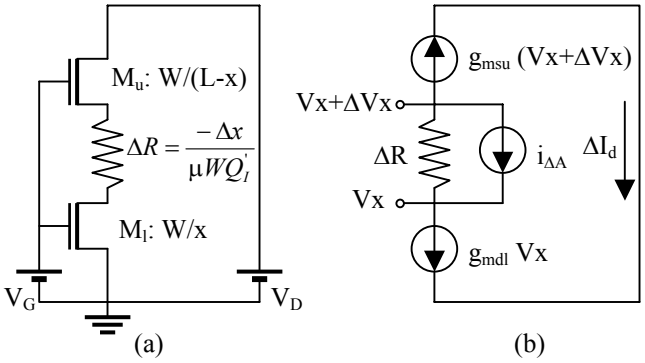

Fig. 1: Splitting of a transistor into three series elements (a) transistor equivalent circuit (b) small-signal equivalent circuit.

4 NUMBER FLUCTUATION MISMATCH MODEL

The relationship between local fluctuation of the inversion charge density and the local current fluctuation that follows from expression (4) is

$$i_{\Delta A} = I_D \frac{\Delta Q'_I}{Q'_I} \quad (6)$$

where $\Delta Q'_I$ is the fluctuation of the inversion charge density in the channel element of area ΔA. For the sake of simplicity we consider fluctuation in the number of carriers only, but the analysis can also be extended to include mobility fluctuation for the computation of the local current fluctuation.

From UCCM, equation (3), one can readily derive the relation between local charge density and threshold voltage fluctuations

$$\Delta Q'_I = C'_{ox} \frac{Q'_I}{Q'_I - nC'_{ox}\phi_t} \Delta V_T \ . \quad (7)$$

The variance $\overline{\Delta V_T^2}$ of the local fluctuation of the threshold voltage ΔV_T is calculated from the conventional expression [7]

$$\overline{\Delta V_T^2} = \sigma^2_{VT} = \frac{A^2_{VT}}{W\Delta x} \ . \quad (8)$$

Using (6), (7), and (8) we calculate $(i_{\Delta A})^2$ and inserting this result into (5), we obtain an expression for $\overline{\Delta I_D^2}$. With the aid of (2), the integration along the channel length in (5) changes into an integration on the channel charge density as

$$\sigma^2_{I_D} = \overline{\Delta I_D{}^2} = \frac{\mu C'_{ox} I_D A^2_{VT}}{nL^2} \int_{Q'_{IS}}^{Q'_{ID}} \frac{1}{nC'_{OX}\phi_t - Q'_I} dQ'_I \ . \quad (9)$$

Assuming, as in [7], Poisson statistics for the depletion charge fluctuation, then

$$A^2_{VT} = \frac{q^2}{C'^2_{ox}} (N.x_D) = \frac{q^2}{C'^2_{ox}} N_{oi} \quad (10)$$

where N is the average number of impurities per unit volume in the depletion region, x_D is the depletion depth, and $N_{oi}=Nx_D$ is the effective number of impurities per unit area in the depletion layer.

Finally, using (10) and integrating (9) from source to drain results in

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{q^2 N_{oi} \mu}{L^2 nC'_{ox} I_D} ln\left(\frac{nC'_{ox}\phi_t - Q'_{IS}}{nC'_{ox}\phi_t - Q'_{ID}} \right). \quad (11)$$

The result in (11) is essentially the same as that derived for flicker noise in MOS transistors in [6]. This is because mismatch is a “dc noise” and the physical origin of both

mismatch and flicker noise is fluctuation of fixed charges and localized states along the channel, respectively.

5 MISMATCH MODEL IN TERMS OF INVERSION LEVELS

A useful alternative expression for (11) is obtained if the charge densities at source and drain are expressed in terms of the normalized forward and reverse currents i_f and i_r. In the ACM model [3], the drain current is expressed as the difference between forward (I_F) and reverse (I_R) components

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) = I_S(i_f - i_r) \qquad (12)$$

where $I_S = \frac{1}{2}\mu C'_{ox} n\phi_t^2 (W/L)$ is the specific current, which is proportional to the geometric ratio W/L of the transistor. V_G, V_S, and V_D are the gate, source, and drain voltages, respectively. i_f and i_r are the normalized forward and reverse currents or inversion levels at source and drain, respectively. Using the relationship between inversion charge densities and currents [3], expression (11) can be rewritten as

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1+i_f}{1+i_r}\right) \qquad (13)$$

where we define N^* as in [6, 10]

$$N^* = \frac{-Q'_{IP}}{q} = \frac{nC'_{ox}\phi_t}{q} \ . \qquad (14)$$

From weak to strong inversion in the linear region, $i_f \cong i_r$, and (13) reduces to

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{1+i_f} \ . \qquad (15)$$

In weak inversion, $i_f << 1$; thus, the first order series expansion of (13) leads to

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \qquad (16)$$

for either saturation or nonsaturation.

6 MISMATCH MEASUREMENTS

Current mismatch of 24 NMOS 30μm x 1.2μm transistors was measured on a test circuit in the ES2 1.2μm CMOS DLM process, using the circuit shown in figure 2. M_{REF} was kept the same for all measurements while the remaining 23 transistors were used as M_i for data acquisition.

Figure 3 presents the mismatch power normalized to the dc power ($SD^2(I_D)/I_D^2$) for drain-to-source voltage ranging from 20mV (linear region) to 1V (saturation), for different inversion levels. Simulated curves (dotted lines) have been determined from expression (13), with i_r calculated through ACM long-channel model [3]. The average number of impurities per unit area (N_{oi}) is estimated as 6.1×10^{12} cm^{-2}; the resulting A_{VT} calculated from (10) is about 29mV-μm. Specific current (I_S) for the devices under test is 1.2μA. It should be emphasized that drain current mismatch results from geometrical and technological fluctuations; however, for most cases, the dominant factor that affects current mismatch can be associated with V_T mismatch. A remarkable result shown in Fig. 3 is the increased mismatch in strong inversion ($i_f >> 1$) as the MOSFET operating region moves from the linear region to saturation. This result is a consequence of the distributed V_T fluctuation along the channel. Indeed, for strong inversion and saturation, the part of the channel closer to the drain plays a less important role in charge fluctuation along the channel than the part of the channel closer to the source.

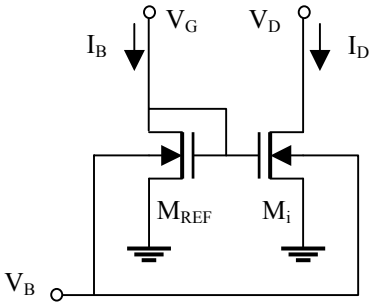

Fig. 2: Test circuit: M_{REF} is the reference transistor while M_i is the transistor under test. I_B (V_B, V_D) is a current (voltage) source.

Figure 4 shows the measured and simulated dependence of current matching on inversion level for linear (V_{DS}=50mV) and saturation (V_{DS}=1V) regions. Transistors were used here in series association of 2 devices, for short channel effects reduction. In the bias range from 10μA to 100μA mismatch seems to increase for the linear region. This behavior is attributed to an effective reduction of the drain-to-source voltage due to voltage drops in contact and diffusion resistances.

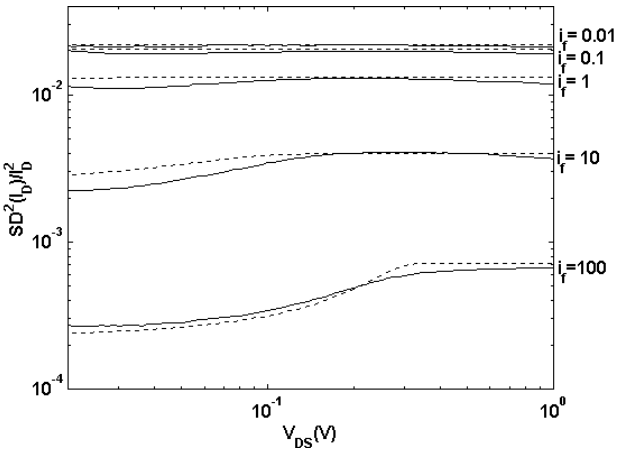

Fig. 3: Normalized current mismatch power. Bulk was kept at zero volts. (Measurements: —; simulation: ---.)

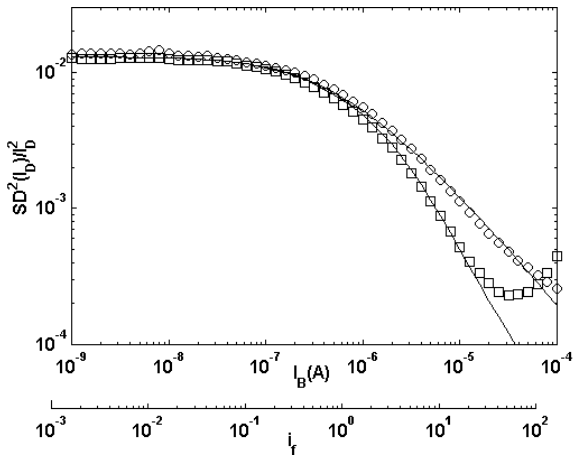

Fig. 4: Dependence of measured current matching on inversion level for linear (□- V_{DS}=50mV) and saturation (O- V_{DS}=1V) regions. Bulk was kept at zero volts. Solid lines represent theoretical expression (13).

7 NUMBER FLUCTUATION FLICKER NOISE MODEL

Flicker noise or simply *1/f* noise displays a power spectral density (PSD) of the form $S(f)=K/f^{\beta}$, with K, β constants, $\beta \cong 1$ [2, 6]. The normalized PSD of the noise current S_{I_d}/I_D^2 presents a plateau in weak inversion and decreases in strong inversion [6, 8].

Moderate and weak inversion are very important for modern low-voltage and low-power design; however, some of the available models of flicker noise do not give correct results in weak or moderate inversion. Spice models NLEV=0 or 1 [9] wrongly predict the dependences of the noise performance in terms of the bias point. In model NLEV=0, S_{I_d}/I_D^2 tends toward infinity in weak inversion. Spice NLEV=1 gives a constant S_{I_d}/I_D^2 for all the operation regions. The BSIM3v3 noise model [10] shows the correct behavior for the S_{I_d}/I_D^2 ratio from weak to strong inversion and is consistent for series and parallel association. However, the BSIM3v3 noise model interpolates flicker noise in moderate inversion [10] and it has the drawback of having 3 fitting parameters.

The physics-based compact model of [6]

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{ot}\mu}{L^2 n C'_{OX} I_D} \cdot \frac{1}{f} \ln\left(\frac{nC'_{OX}\phi_t - Q'_{IS}}{nC'_{OX}\phi_t - Q'_{ID}}\right) \qquad (17)$$

is formally equivalent to the mismatch model (11). The parameter N_{ot} is the equivalent density of oxide traps defined [6] by

$$N_{ot}[cm^{-2}] = \frac{k_B T N_t(E)}{\gamma} \qquad (18)$$

where $N_t(E)$ [$cm^{-3}eV^{-1}$] is the density of oxide traps per unit volume and unit energy and γ[cm^{-1}] is the attenuation coefficient of the electron wave function in the oxide [6]. For $N_t(E)$=4x$10^{16}$$cm^{-3}eV^{-1}$, k_BT=0.026eV and $1/\gamma$=1Å (10^{-8}cm), N_{ot} is of the order of $10^7 cm^{-2}$ [6].

Some *1/f* noise measurements have been performed in MOS transistors covering all regions of operation. In all cases, the PSD closely follows a *1/f* dependence. This is consistent with the assumption of a uniform spatial distribution of the traps inside the oxide. Noise spectra were acquired from 0.3 to 30Hz, where the PSD of the flicker noise is considerably higher than the PSD of the thermal noise and the effect of the ac line is avoided. For the calculation of the theoretical model, the charge densities $Q'_{IS(D)}$ were estimated with a circuit simulator using the ACM model [6]. The parameter N_{ot} of the model in (17) is adjusted to best fit the measurements, with the result $\overline{N}_{otN} = 2x10^7 cm^{-2}$, $\overline{N}_{otP} = 3x10^7 cm^{-2}$, for the NMOS and PMOS transistors, respectively. Fig. 5 contains simulation and measurements of normalized flicker noise PSD (S_{I_d}/I_D^2) for a saturated NMOS of a 0.8µ CMOS process, with an aspect ratio W/L=200µm/5µm that allows one to comfortably characterize noise in weak inversion. Note here the plateau in weak inversion, a result in close agreement with the theory.

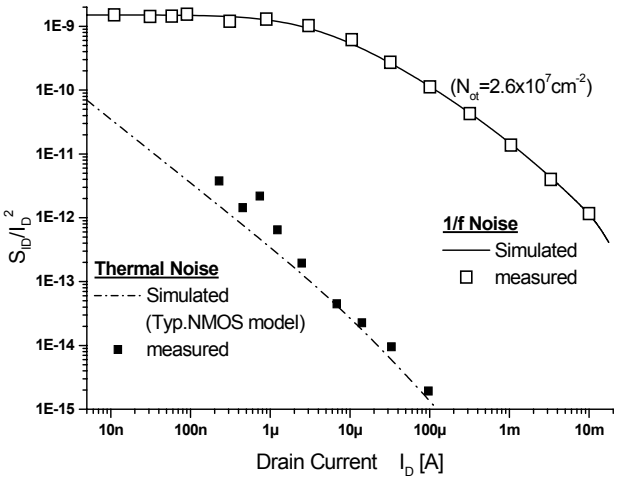

Fig. 5: Normalized flicker (thermal) PSD S_{I_d}/I_D^2 at f=1Hz for a saturated NMOS transistor(W/L=200µm/5µm).

8 THERMAL NOISE MODEL

According to the classical theory [4], the power spectral density of the thermal noise current of the channel element $\Delta R=-\Delta x/\mu WQ'_I$ is

$$\frac{(i_{\Delta A})^2}{\Delta f} = 4k_B T \frac{\left(-\mu W Q_I'\right)}{\Delta x}. \qquad (19)$$

Substituting (19) into (5) and integrating, results in

$$\frac{(\Delta I_D)^2}{\Delta f} = -\frac{4k_B T \mu}{L^2} Q_I \qquad (20)$$

where $Q_I = W\int_0^L Q_I' dx$ is the total channel charge, which can be expressed in terms of Q_{IS}', Q_{ID}' [3, 4]. Using the ACM model to approximate (20) for a saturated transistor, it is possible to rewrite the PSD S_{iw} of the thermal noise:

$$S_{iw} = \frac{(\Delta I_D)^2}{\Delta f} = \gamma n k_B T . g_m \qquad (21)$$

with γ=2 in weak inversion, and γ=8/3 in strong inversion. $g_m = 2I_S\left(\sqrt{1+i_f}-1\right)/n\phi_t$ is the gate transconductance of the transistor. Eq. (21) is a classical approximation for thermal noise in an MOS channel.

The corner frequency at which the flicker noise and thermal noise have the same value has particular importance in analog design. It can be calculated directly in terms of Q_{IS}', Q_{ID}' from eqs. (17, 20) but a simple approximation can be derived from (21), and expressing (17) in terms of the inversion level as in section 5:

$$f_c \cong \frac{\pi}{2} f_T . \frac{N_{ot}}{N^*} . \qquad (22)$$

Note that the corner frequency in eq. (22) is related to the transition frequency f_T of the transistor, which results a useful approximation for the designer. In Fig.5 and in Fig. 6, we show the predicted and measured thermal noise, and corner frequency of an NMOS transistor.

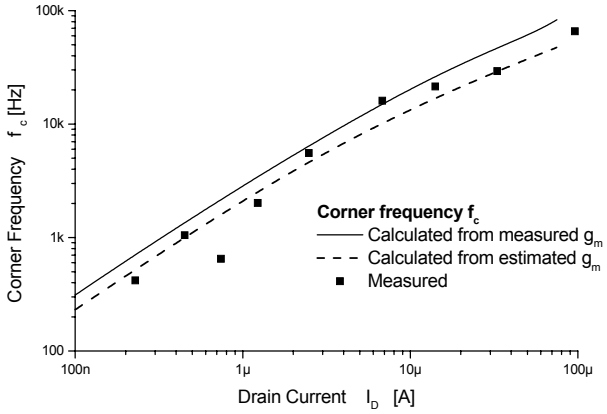

Fig. 6: Estimated and measured value of the corner frequency f_c, for a W/L=200µm/5µm NMOS transistor.

9 SUMMARY

Formally equivalent mismatch and low frequency noise models for the MOS transistor, continuous in all operating regions, have been developed. An approach, based on fluctuation of carrier number was used to integrate all the contributions of small fluctuating elements along the transistor channel. This approach along with the description of the dc characteristics of MOSFET's from the ACM model resulted in compact easy-to-use formulas for mismatch and *1/f* noise that cover all operating regions. Experimental results confirmed the accuracy of our model under various bias conditions. It is expected that this work will highlight the parallelism between mismatch and noise in the design of accurate circuits.

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