Consistent parameter extraction using different MOSFET models

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CIRCUITOS
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- Extraction from BSIM6 simulations

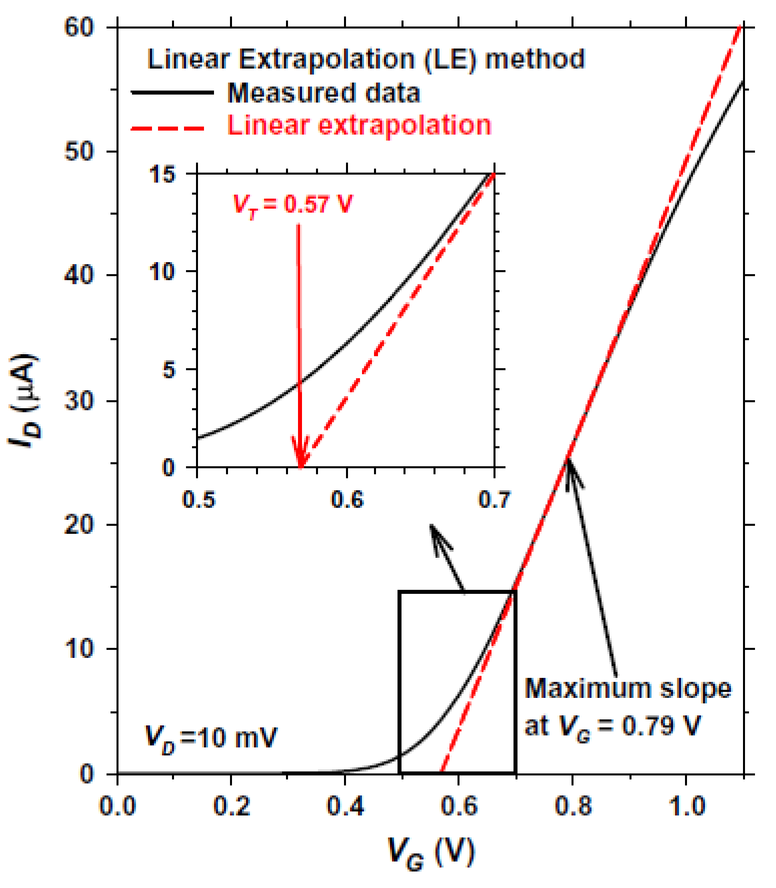
On the ‘definitions’ of the threshold voltage

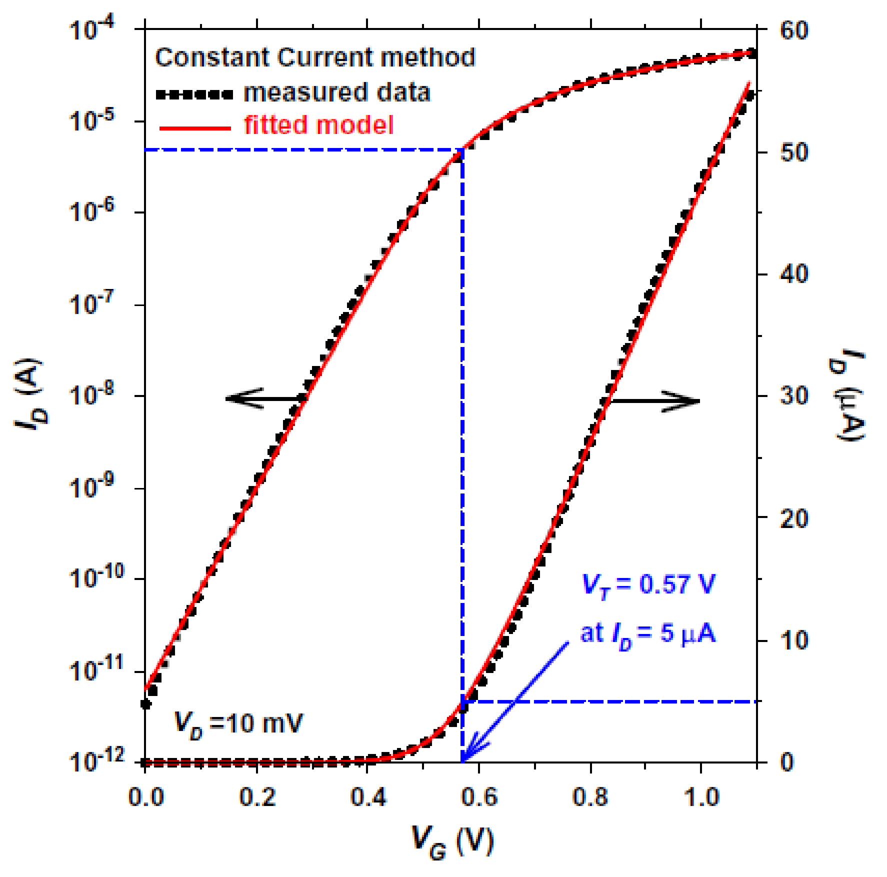
- Surface potential based $\phi_s = 2\phi_F + V_C$
- Qualitative: gate voltage at which ***significant*** drain current starts to flow
- Procedural based (details on next slide)

Other approaches:

- Splitting the threshold: define weak, moderate and strong inversion VTs
- Deconstructing the threshold: surface potential models don’t use VT as parameter!

The standard VT extraction methods

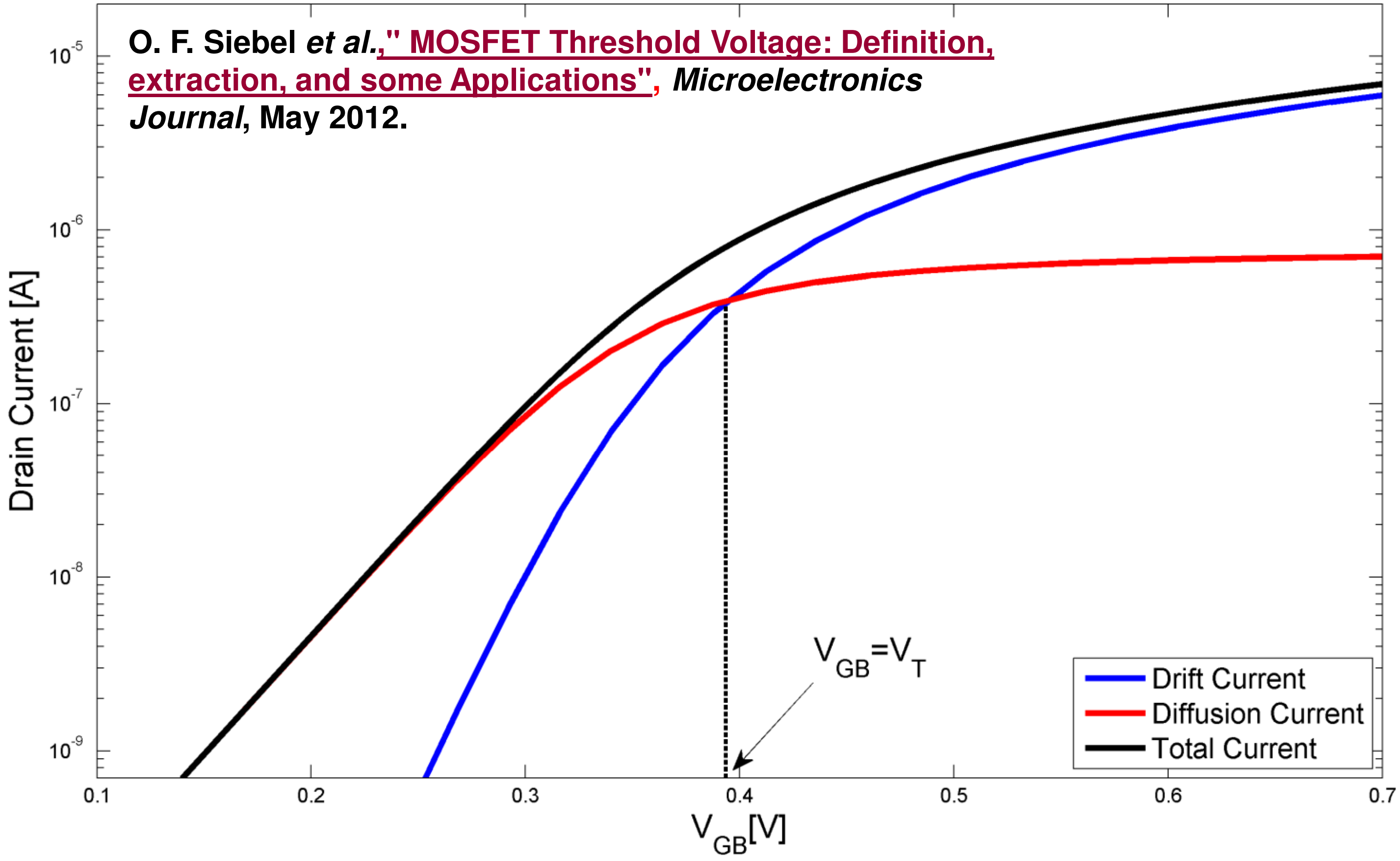




PROBLEM: **missing link between extracted threshold and surface potential value!**

A. Ortiz-Conde *et al*, " Revisiting MOSFET threshold voltage extraction methods", *Microelectronics* *Reliability*, 2012

Current based definition of threshold 1

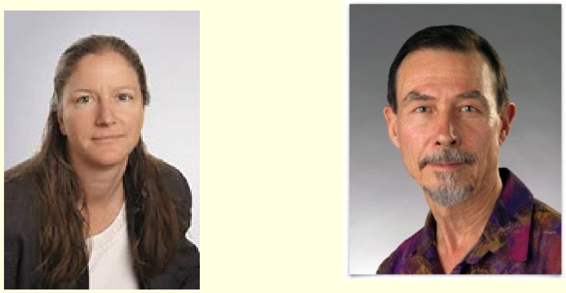

O. F. Siebel *et al.*," **MOSFET Threshold Voltage: Definition, extraction, and some Applications",** ***Microelectronics Journal*, May 2012.**

MOSFET OPERATION: Drain current split into diffusion and drift components vs. gate voltage for a MOSFET operating in the linear region with $V_{DS}=\phi_t/2=13$mV.

Current-based definition of threshold 2

- **Sound modeling:** To accurately extract V_T it is essential that the MOSFET model includes the drift and diffusion transport mechanisms, both important near the threshold condition.
- Extraction methods based solely on the strong (SI) or weak (WI) inversion models are inherently inaccurate since to determine the threshold voltage (which is found between the SI and WI regions) experimental data are extrapolated from only one of these two operating regions.

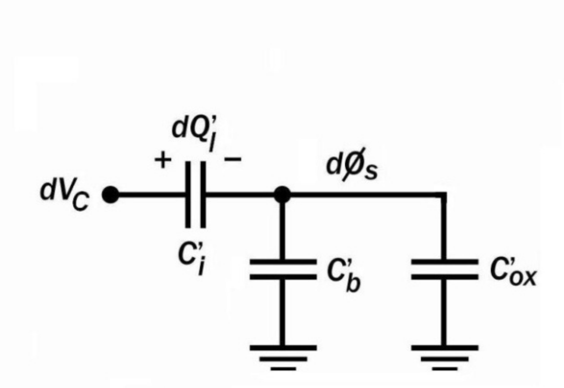
Current based definition of threshold 3



M. A. Maher and C. A. Mead, “A physical charge-controlled model for MOS transistors,” *Advanced Research in VLSI*, MIT Press

Take $I_{drift} = I_{diff}$ to define the threshold.

$$Q'_{ITH} = -(C'_{ox} + C'_b)\frac{kT}{q} = -nC'_{ox}\frac{kT}{q}$$



C'_{ox} C'_b are the oxide and depletion capacitances per unit area

The carrier charge density at threshold is the effective channel capacitance per unit area times the thermal voltage, or the thermal charge per unit area

Charge-based all-region MOSFET model 1

Long-channel MOSFET

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

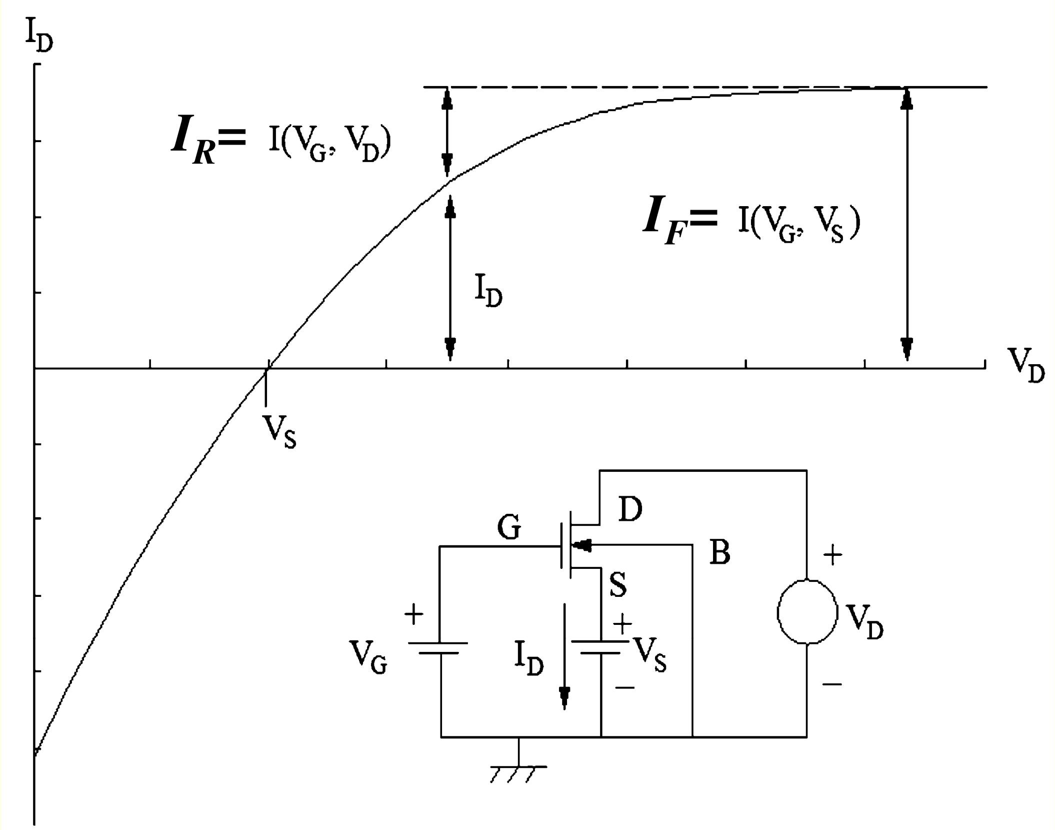
I_F: forward current

I_R: reverse current

Specific or normalization current I_S

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L}$$

$$\phi_t = \frac{kT}{q} \qquad n = 1 + \frac{C'_b}{C'_{ox}}$$



C'_{ox} C'_b oxide and depletion capacitances per unit area

Charge-based all-region MOSFET model 2

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$q'_I = \frac{Q'_I}{-nC'_{ox}\phi_t}$$

Normalized inversion charge density

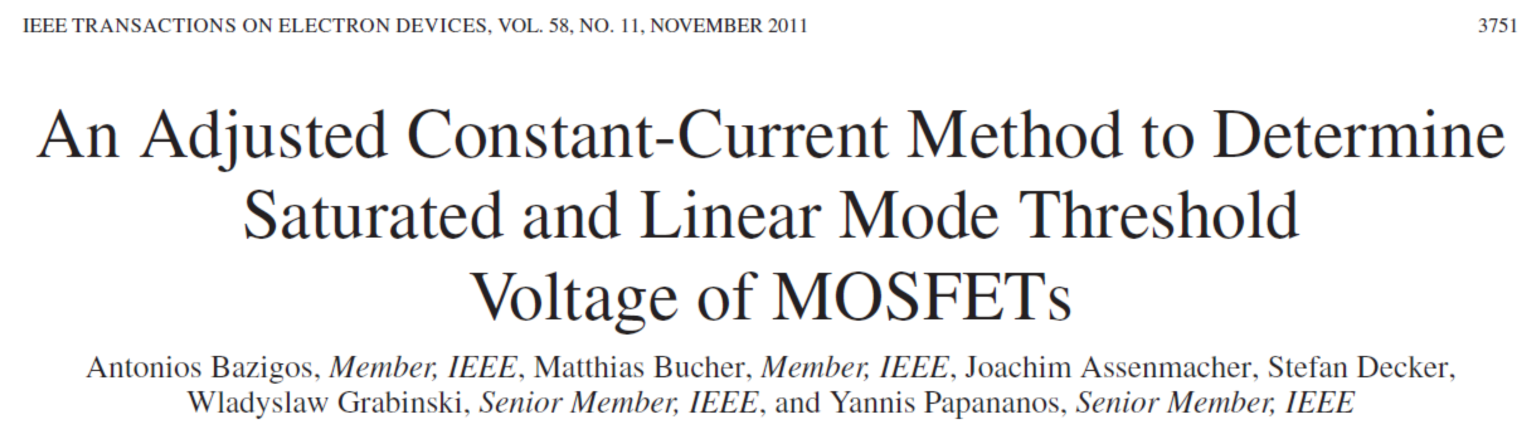
$$\boxed{i_{f(r)} = {q'_{IS(D)}}^2 + 2q'_{IS(D)} \Rightarrow q'_{IS(D)} = \sqrt{1+i_{f(r)}} - 1}$$

Drift Diffusion

Threshold condition at the source:

$$\boxed{q'_{IS} = 1 \rightarrow i_f = 3}$$

Difference between the EKV approach and ours


IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 11, NOVEMBER 2011 3751

An Adjusted Constant-Current Method to Determine Saturated and Linear Mode Threshold Voltage of MOSFETs

Antonios Bazigos, *Member, IEEE*, Matthias Bucher, *Member, IEEE*, Joachim Assenmacher, Stefan Decker,
Wladyslaw Grabinski, *Senior Member, IEEE*, and Yannis Papananos, *Senior Member, IEEE*

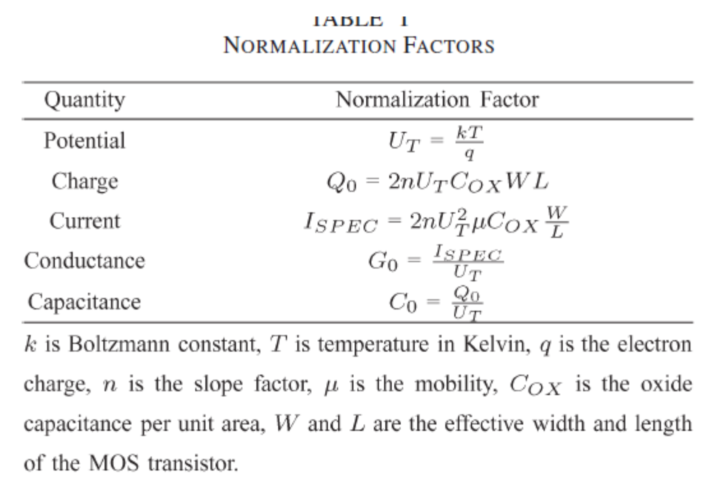


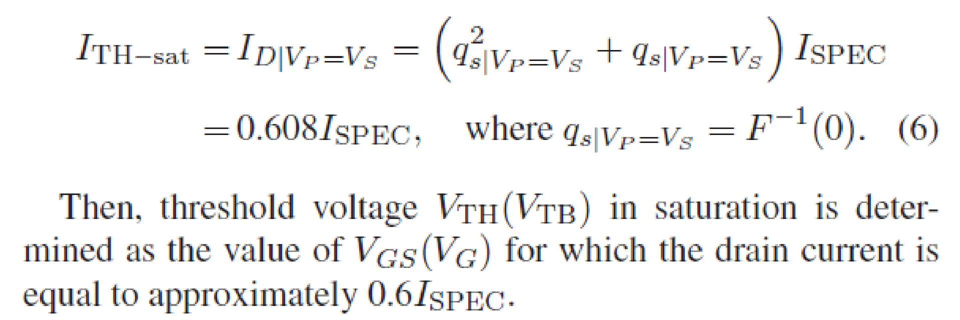
TABLE I
NORMALIZATION FACTORS

Quantity	Normalization Factor
Potential	$U_T = \frac{kT}{q}$
Charge	$Q_0 = 2nU_T C_{OX} WL$
Current	$I_{SPEC} = 2nU_T^2 \mu C_{OX} \frac{W}{L}$
Conductance	$G_0 = \frac{I_{SPEC}}{U_T}$
Capacitance	$C_0 = \frac{Q_0}{U_T}$

k is Boltzmann constant, T is temperature in Kelvin, q is the electron charge, n is the slope factor, μ is the mobility, C_{OX} is the oxide capacitance per unit area, W and L are the effective width and length of the MOS transistor.

Our approach $I_{TH} = 3I_S = 1.5(W/L)\mu C'_{ox} n\varphi_t^2$

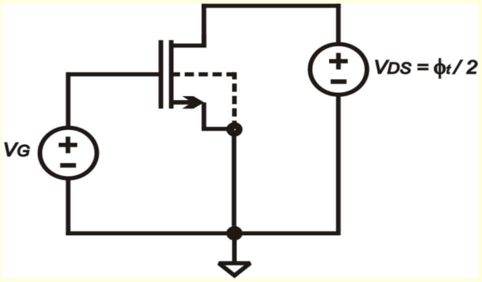
EKV $I_{TH} = 0.608 I_{SPEC} = 1.216 (W/L)\mu C'_{ox} n\varphi_t^2$


$$I_{\mathrm{TH-sat}} = I_{D|V_P=V_S} = \left(q^2_{s|V_P=V_S} + q_{s|V_P=V_S}\right) I_{\mathrm{SPEC}}$$

$$= 0.608 I_{\mathrm{SPEC}}, \quad \text{where } q_{s|V_P=V_S} = F^{-1}(0). \quad (6)$$

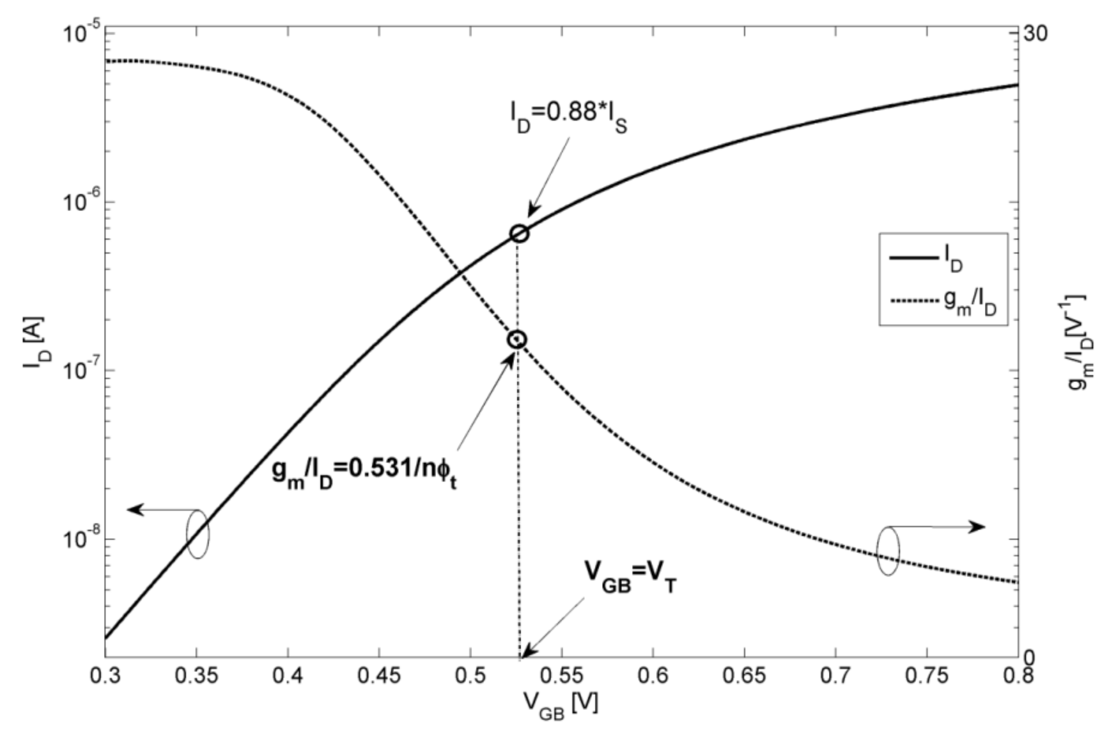
Then, threshold voltage $V_{\mathrm{TH}}(V_{\mathrm{TB}})$ in saturation is determined as the value of $V_{GS}(V_G)$ for which the drain current is equal to approximately $0.6 I_{\mathrm{SPEC}}$.

g_m/I_D V_T-extraction procedure



$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{g_{ms}-g_{md}}{nI_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}$$

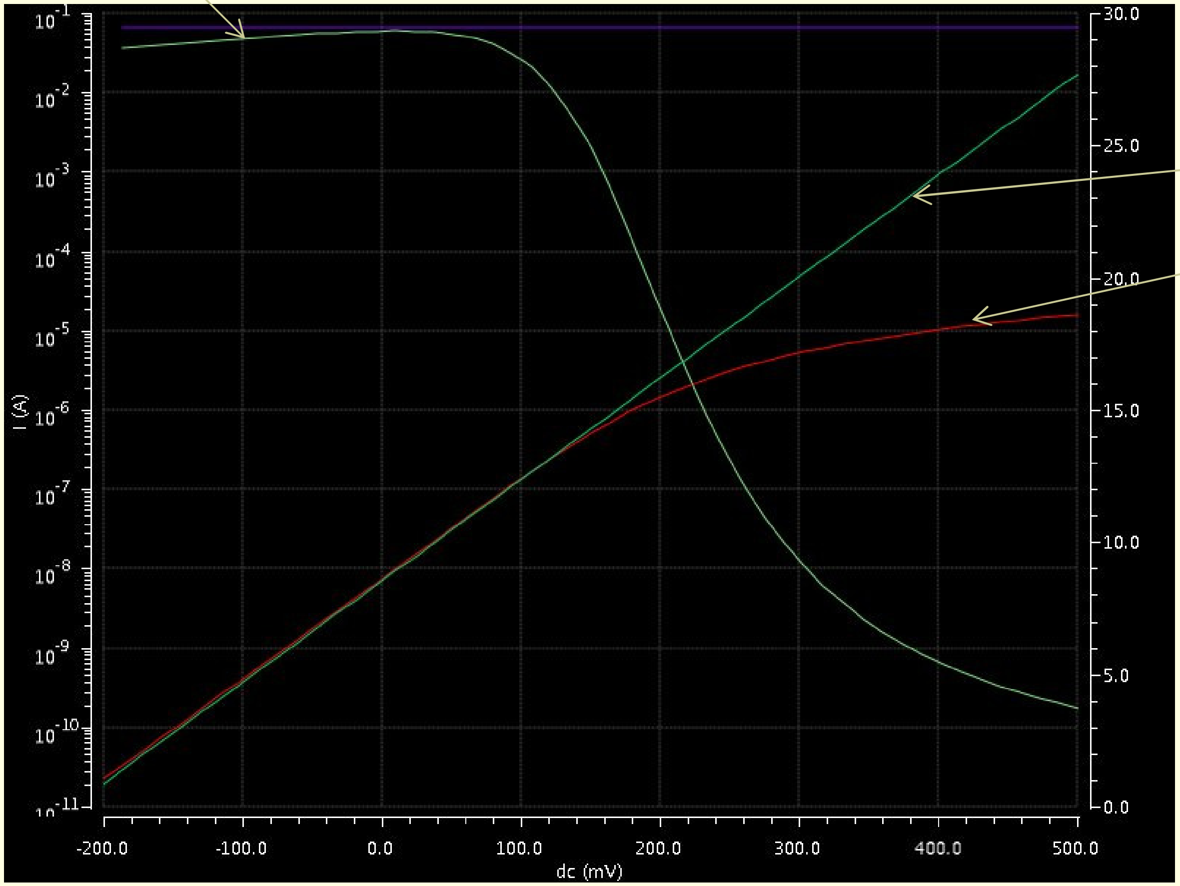
$$\left.\frac{g_m}{I_D}\right|_{V_{DS}\to 0} = \frac{1}{n\phi_t\sqrt{1+i_f}}$$



Thus, at threshold (i_f =3)
g_m/I_D is ½ of its maximum value
($n=n(V_G)\cong$ constant)

For V_{DS} = (1/2)kT/q, g_m/I_D =0.531 $(g_m/I_D)_{max}$ and I_D=0.88*I_S

g_m/I_D V_T-extraction for a 3.5/0.5 nMOSFET simulated by BSIM6



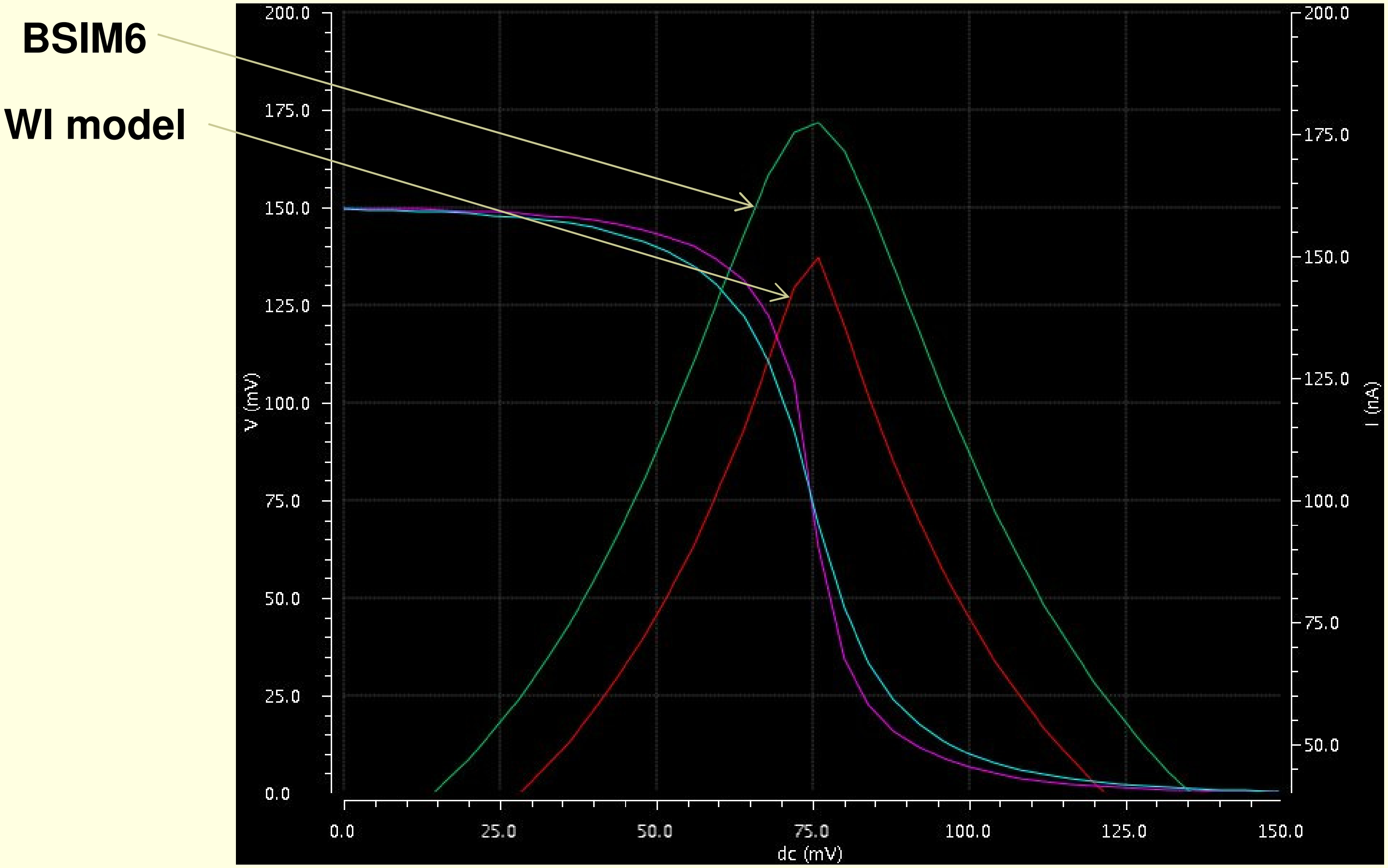
Gm/ID from BSIM6

VT0 = 227 mV
n=1.315

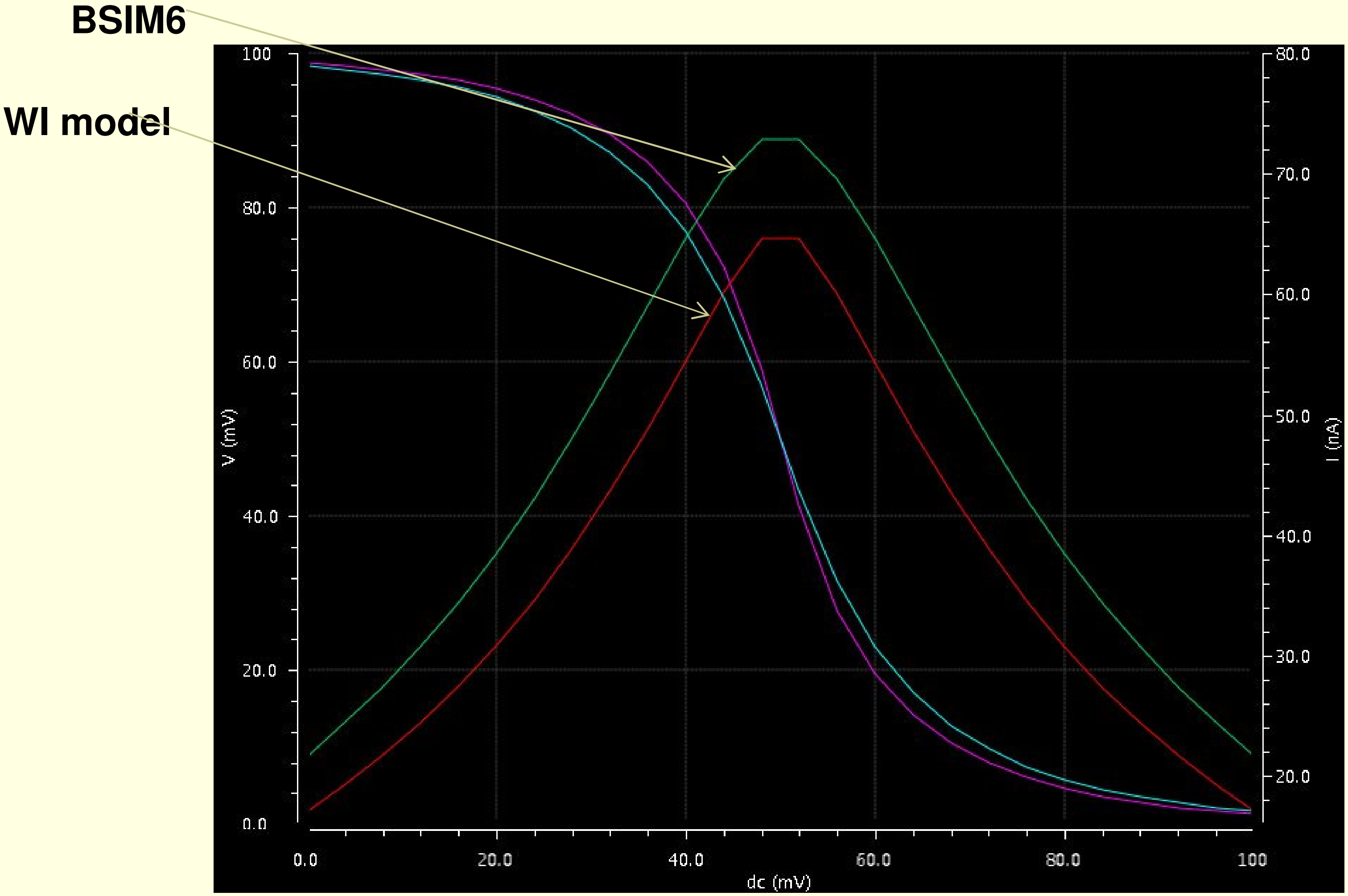
WI model

BSIM6

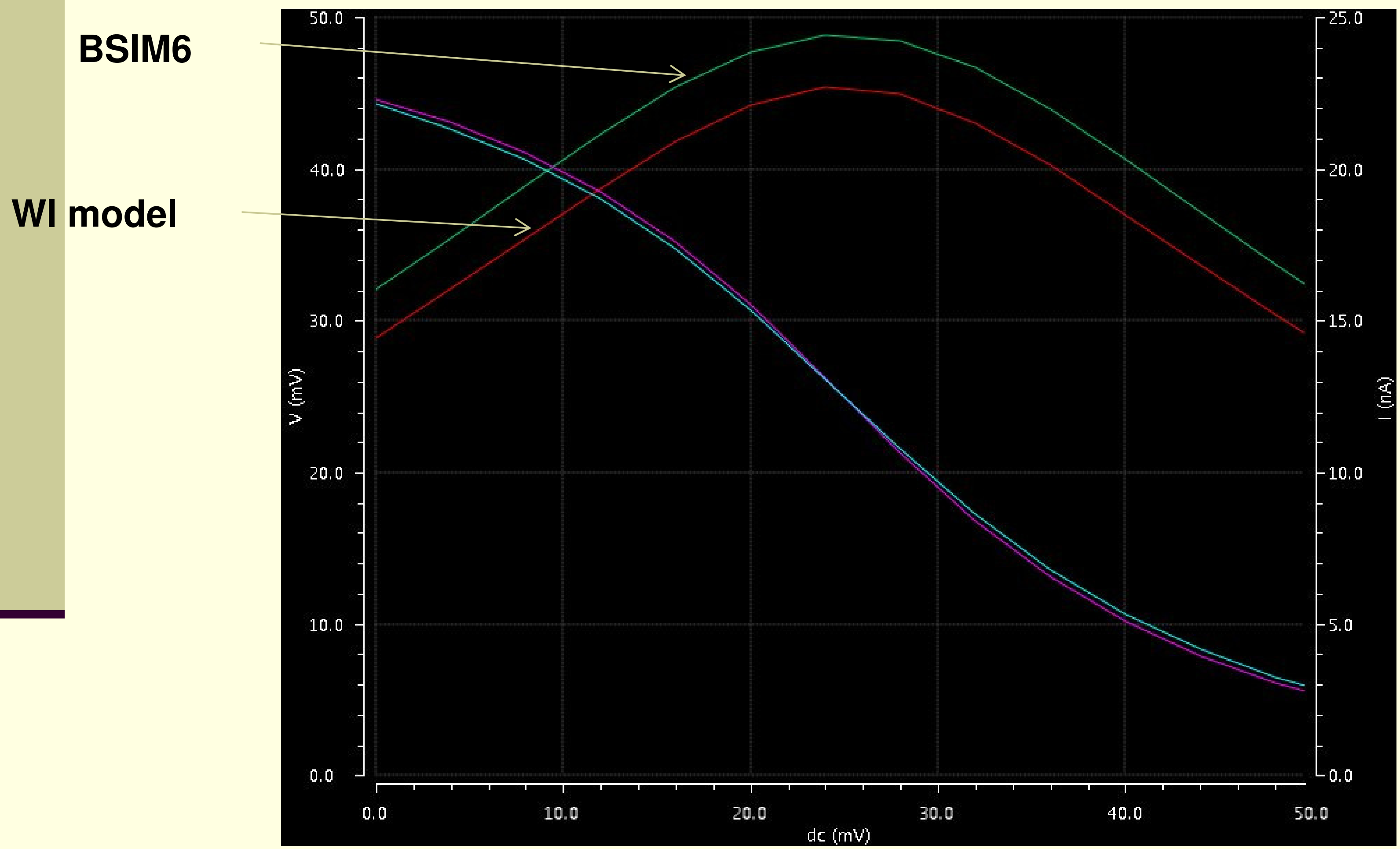
CMOS inverter at VDD = 150 mV



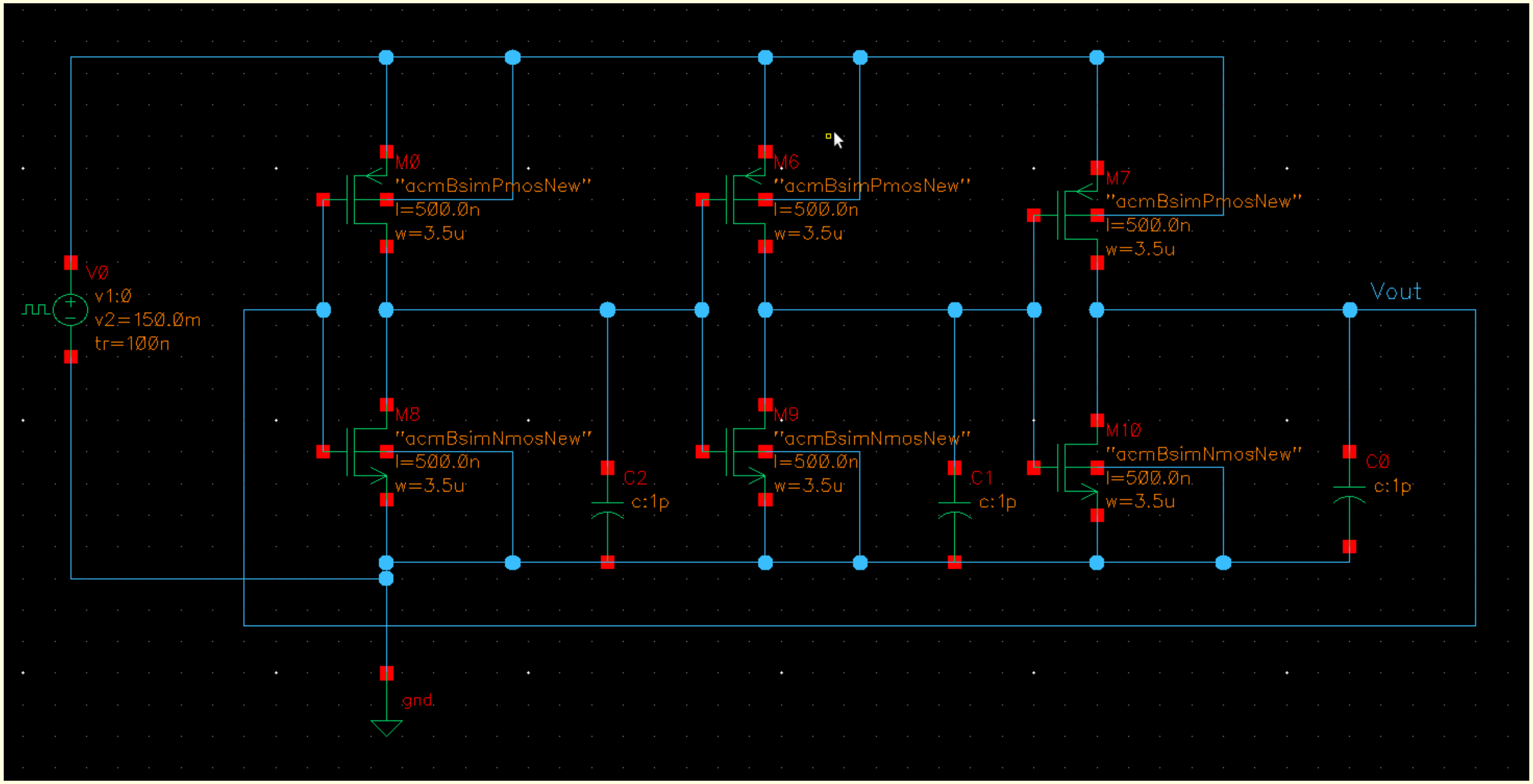
CMOS inverter at VDD = 100 mV



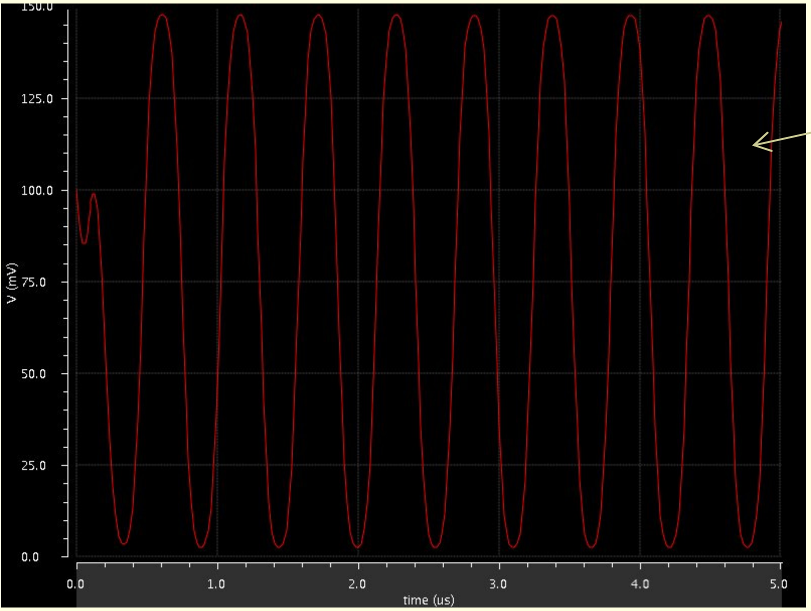
CMOS inverter at VDD = 50 mV



Ring oscillator

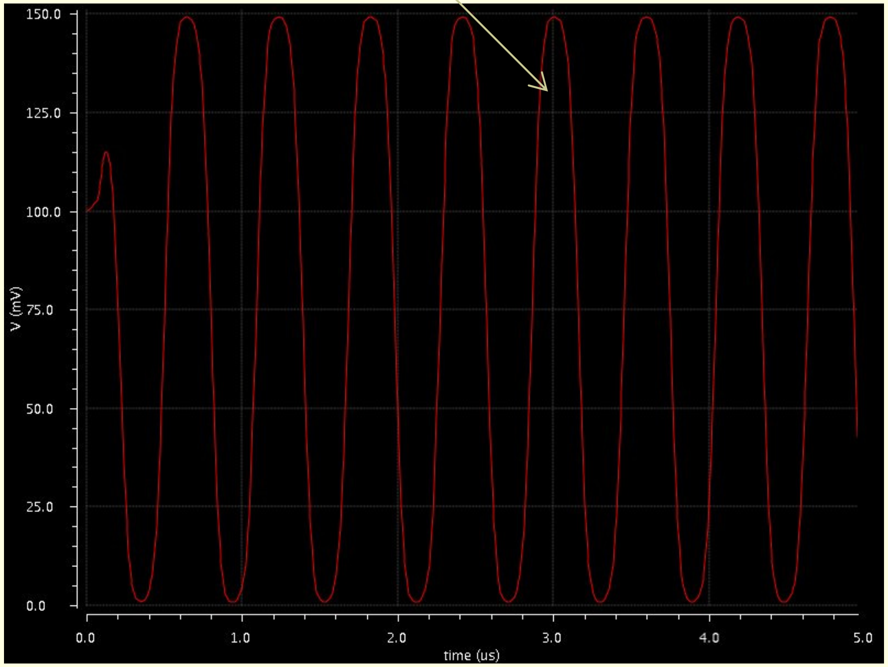


Transient simulation of the ring oscillator

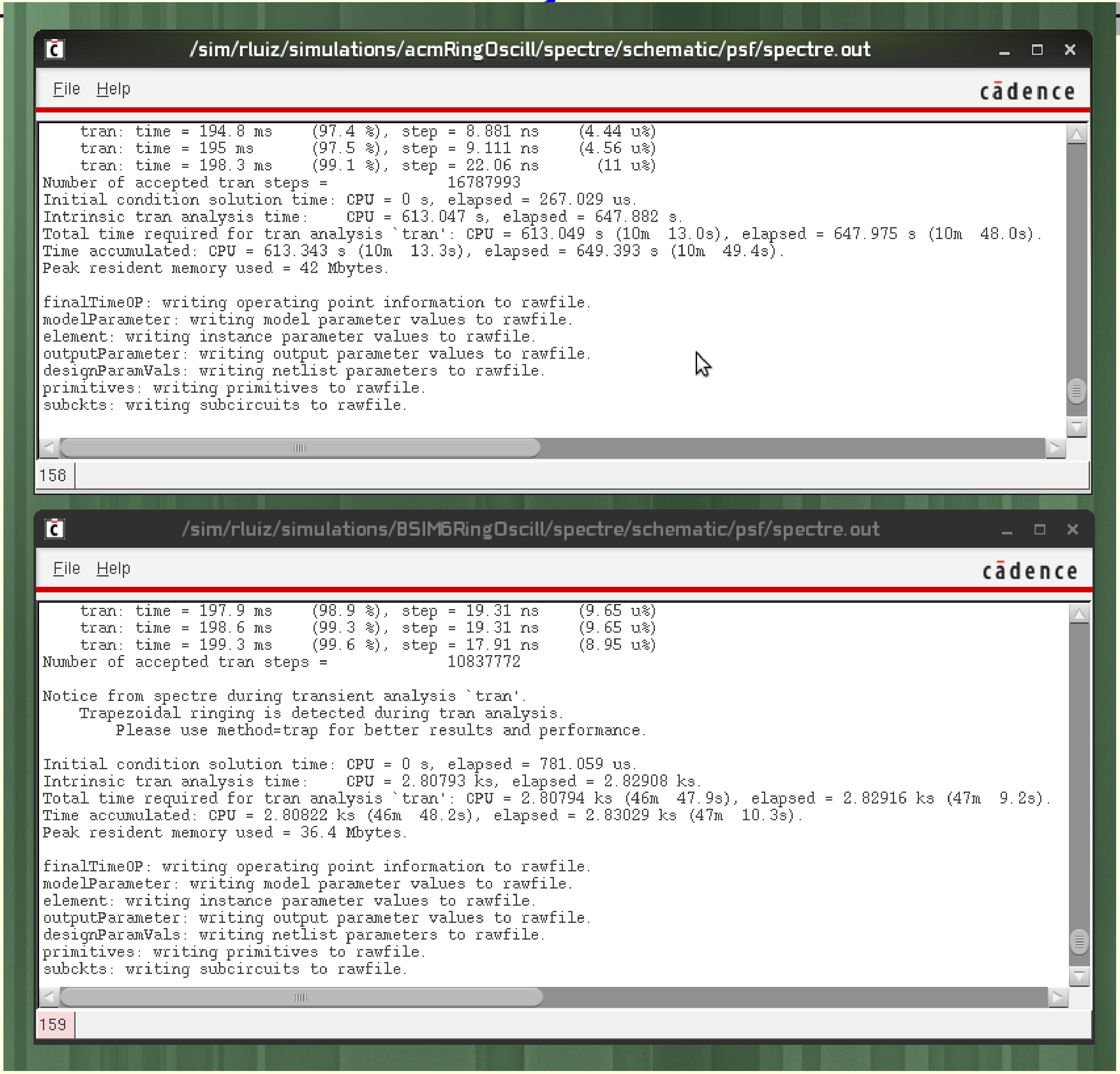


BSIM6

WI model



Transient time analysis: BSIM6 vs. WI model



```
    tran: time = 194.8 ms    (97.4 %), step = 8.881 ns    (4.44 u%)
    tran: time = 195 ms      (97.5 %), step = 9.111 ns    (4.56 u%)
    tran: time = 198.3 ms    (99.1 %), step = 22.06 ns      (11 u%)
Number of accepted tran steps =             16787993
Initial condition solution time: CPU = 0 s, elapsed = 267.029 us.
Intrinsic tran analysis time:    CPU = 613.047 s, elapsed = 647.882 s.
Total time required for tran analysis `tran': CPU = 613.049 s (10m  13.0s), elapsed = 647.975 s (10m  48.0s).
Time accumulated: CPU = 613.343 s (10m  13.3s), elapsed = 649.393 s (10m  49.4s).
Peak resident memory used = 42 Mbytes.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```

```
    tran: time = 197.9 ms    (98.9 %), step = 19.31 ns    (9.65 u%)
    tran: time = 198.6 ms    (99.3 %), step = 19.31 ns    (9.65 u%)
    tran: time = 199.3 ms    (99.6 %), step = 17.91 ns    (8.95 u%)
Number of accepted tran steps =             10837772

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.

Initial condition solution time: CPU = 0 s, elapsed = 781.059 us.
Intrinsic tran analysis time:    CPU = 2.80793 ks, elapsed = 2.82908 ks.
Total time required for tran analysis `tran': CPU = 2.80794 ks (46m  47.9s), elapsed = 2.82916 ks (47m  9.2s).
Time accumulated: CPU = 2.80822 ks (46m  48.2s), elapsed = 2.83029 ks (47m  10.3s).
Peak resident memory used = 36.4 Mbytes.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```

Conclusions

- The fundamental problem in switching between transistors models is to consistently determine the parameters of the different models.
- The gm/ID procedure in the linear region allows determining accurately the most critical MOS parameters: the threshold voltage, the slope factor, and the specific current.
- Examples comparing simulations carried out with BSIM6 model and a simple weak inversion MOSFET model show good agreement for very low voltage circuits.

Acknowledgments

- CADENCE Academic network for providing the CADENCE licenses
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