

Switched Inverter- A New Technique for Sample Data Low-Voltage and Low-Power Applications

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Abstract

-- In this paper, a new technique called 'Switched Inverter' for analog sample data signal processing is proposed. The circuit is based on the conventional CMOS inverter operating as a transconductor. The proposed circuit does not require linear capacitors and employs switches that operate at fixed channel voltage. Owing to the use of inverters, the proposed structure presents class-AB operation. A 8'th taps FIR filter has been designed in a standard 0.35- μm CMOS technology at 0.6V supply.

I. Introduction

Generally, the conventional sampled data circuits such as switched capacitor (SC) [1] and Switched-Current (SI) [2] are not low supply voltage operating circuit due to the conduction gap of the switch [3] shown in Fig.1. Therefore many techniques such as switch op-amp [3,4], and switched MOSFET [5,6], have been developed to overcome the switch problem in switched capacitor and switched current, respectively. The switched MOSFET [5,6] suffers from the resistive load to the active element " transistor works in triode region" as shown in Fig. 2(b).

This paper presents a novel topology of sampled data circuits for low-voltage and low-power applications. To reduce supply voltage and power consumption, a minimalist design style based on inverters and switches is proposed. In the new circuit, the switches operate at fixed

channel voltage, which improves the accuracy of the proposed cell. Moreover, the core cell consumes low power due to class-AB operation.

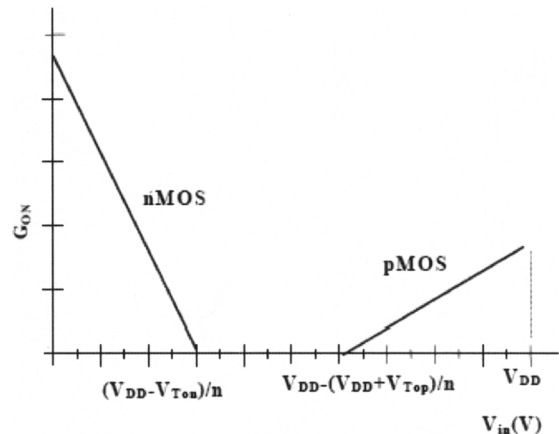


Fig.1. On-conductance of a CMOS switch.

The paper is organized as follows: Section II describes the SI and SM techniques. The new S/H circuit is described in Section III. The simulation results are shown in Section IV. Concluding remarks are drawn in Section V.

II. Current Mode Sample Data Circuits

Both S/H circuits shown in Fig. 2 operate as current mirrors when the switches are closed. In Fig. 2 (b), assuming the op-amp to be ideal, transistors M_1 and M_2 are both biased with the same set of voltages. Therefore, neglecting transistor mismatch, the output current I_0 is an inverted replica of the input current I_{in} .

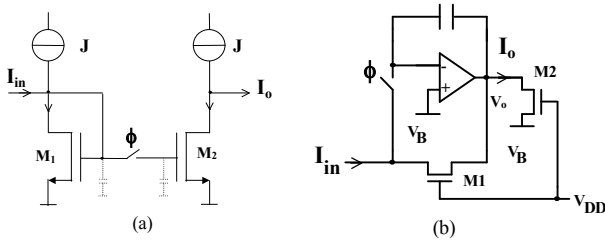


Fig. 2 (a). Conventional SI S/H cell [2].
(b). Switched-MOSFET S/H circuit [5,6].

In the track mode of both circuits, the input current is fed to the cell. The current is memorized as a voltage across the holding capacitor. In the hold mode, the switch opens and the voltage is held on the capacitor. The output current is equal to its value on the previous clock phase.

The proper operation of the current mirror in Fig. 2(a) requires the transistors to operate in saturation while the transistors in Fig. 2(b) have to operate in the triode region.

III. Switched-Inverter Circuit

The S/H circuit consists of 4 identical CMOS inverters, a holding capacitor, and a switch as shown in Fig. 3. A CMOS inverter is the simplest possible implementation of a transconductor. The dotted inverters provide non-inverted or inverted replicas of the input current. The holding capacitor is not required to be linear. The S/H circuit operates as follows.

- Sample mode - After the switch has been closed, the input of Inv-4 is charged to a voltage v_{g2} such that the difference between the currents flowing through the n-channel and p-channel transistors in Inv-4 equals the input current. The intermediate inverters (Inv-2 and Inv-3) compose an inverting unity gain amplifier, as shown in Fig. 4. In effect, because the current “I” flowing out of transconductor (inv-2) is flowing into transconductor (inv-3), $v_{g2} = -v_{g1}$ must follow. The input current is memorized as a voltage across the holding capacitor C_h . The high transconductance of the complete cell, given by $-g_{m4}A_{V1}$ (g_{m4} is the

transconductance of Inv-4 while A_{V1} is the voltage gain of Inv-1), ensures an almost constant input voltage for the S/H cell, which is equal to the threshold voltage (V_B) of the inverter.

- Hold mode – When the switch opens, the voltage held on the capacitor keeps v_{g1} and v_{g2} constant. The inputs of the dotted inverters are v_{g1} and v_{g2} ; therefore, as long as the outputs of the dotted inverters ensure saturation of the transistors, the output currents I_{o1} and I_{o2} are non-inverted and inverted copies of I_{in} .

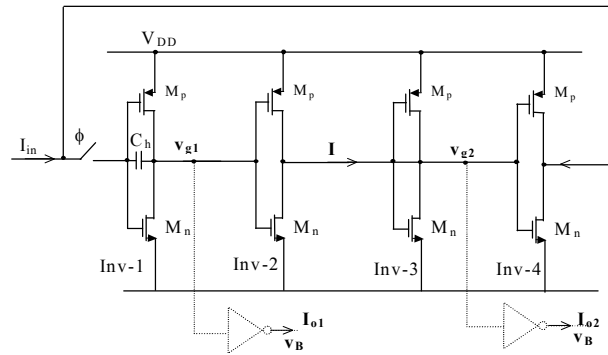


Fig. 3. Sample and hold circuit of S-Inv technique.

Since the channel voltage of the switch is fixed to V_B , both charge injection and settling time are signal-independent, which reduces the sampling error. The dimensions of the inverters can be mask-programmed to allow for programmability of the S-Inv cells.

The ac analysis of the circuit in Fig. 3 leads to the transfer function of the cell, which can be approximated to a single-pole transfer function as:

$$\frac{I_{o2}(s)}{I_{in}(s)} \cong -\frac{1}{1 + \frac{s}{A_{Vp1}}} \quad (1)$$

with $p_1 = g_{o4}/A_{V1}C_h$, and $A_V = \frac{g_{m1}g_{m4}}{g_{o1}g_{o4}}$. The 1% settling time of the S/H cell is equal to $4.6 * C_h/g_{m4}$.

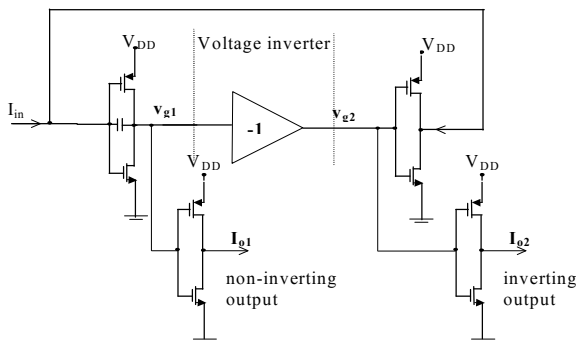


Fig. 5. The S-Inv at sampling mode.

IV. Circuit Design and Simulation

The proposed S/H circuit has been designed with MOSFET parameters of the TSMC 0.35- μm CMOS technology. The transistors operate in weak inversion due to very low supply voltage ($V_{DD} \cong V_{THn} = 0.6\text{V}$, $V_{THp} = -0.77\text{V}$). A threshold voltage mismatch factor $A_{VTn(p)} = 8.2$ (14.9) mV/ μm and a current mismatch factor $A_{\beta n(p)} = 0.2\%$ (0.4%) μm have been considered for circuit design. The mismatch model [7] has been used to determine the minimum transistor area. The dimensions $48\mu\text{m}/1.75\mu\text{m}$ for the n-MOS transistors and $144\mu\text{m}/1.75\mu\text{m}$ for the p-MOS transistors result in a 0.1% standard deviation for the inverter current. The dimensions of the CMOS switch are $0.7\mu\text{m}/0.35\mu\text{m}$ and $2\mu\text{m}/0.35\mu\text{m}$ for the n and p-channel transistors, respectively. The holding capacitor is 0.5pF. The clock frequency is 10 kHz and the amplitude is 0.9V, slightly higher than the power supply to provide an adequate switch conductance. The threshold voltage of the inverter is $V_B = 224\text{mV}$. Fig. 6 shows the non-inverted and inverted outputs of the S/H cell for a 400nA (peak value), 0.5kHz input current. The biasing current for each inverter is around 6.5nA.

The designed S-Inv S/H circuit is employed for 8-taps FIR filter. The FIR tape coefficients are $a_1 = a_8 = -0.0698$, $a_2 = a_7 = 0.1142$, $a_3 = a_6 = 0.2233$ and $a_4 = a_5 = 0.3254$ by using MATLAB routine. The simulations have been run with SMASH. The frequency response of the designed FIR filter is shown in Fig. 7

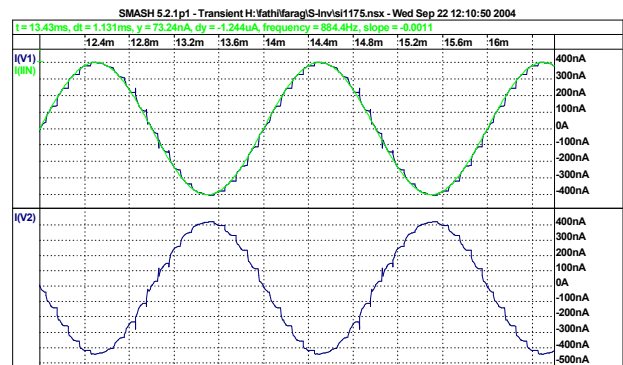


Fig. 6. Non-inverted and inverted outputs of the S/H cell.

V. Conclusion

A new topology for sampled data circuit named switched inverter has been introduced. The S-Inv technique has been tested for very low voltage and ultra-low power consumption. In the S-Inv technique, the switches operate at constant channel voltage, which alleviates the distortion errors due to voltage-dependent charge injection and switch conductance. An 8 taps FIR sample data filter has been designed and simulated using the proposed technique. The simulation results shows the applicability of the proposed technique. The circuit has been designed and simulated by using a TSMC 0.35- μm technology with 0.6V supply voltage. The overall power consumption of the proposed S/H circuit is 60 nW/tap. The initial stage of this research has shown very encouraging results for the application of the S-Inv circuit to low-power low-voltage analog circuits.

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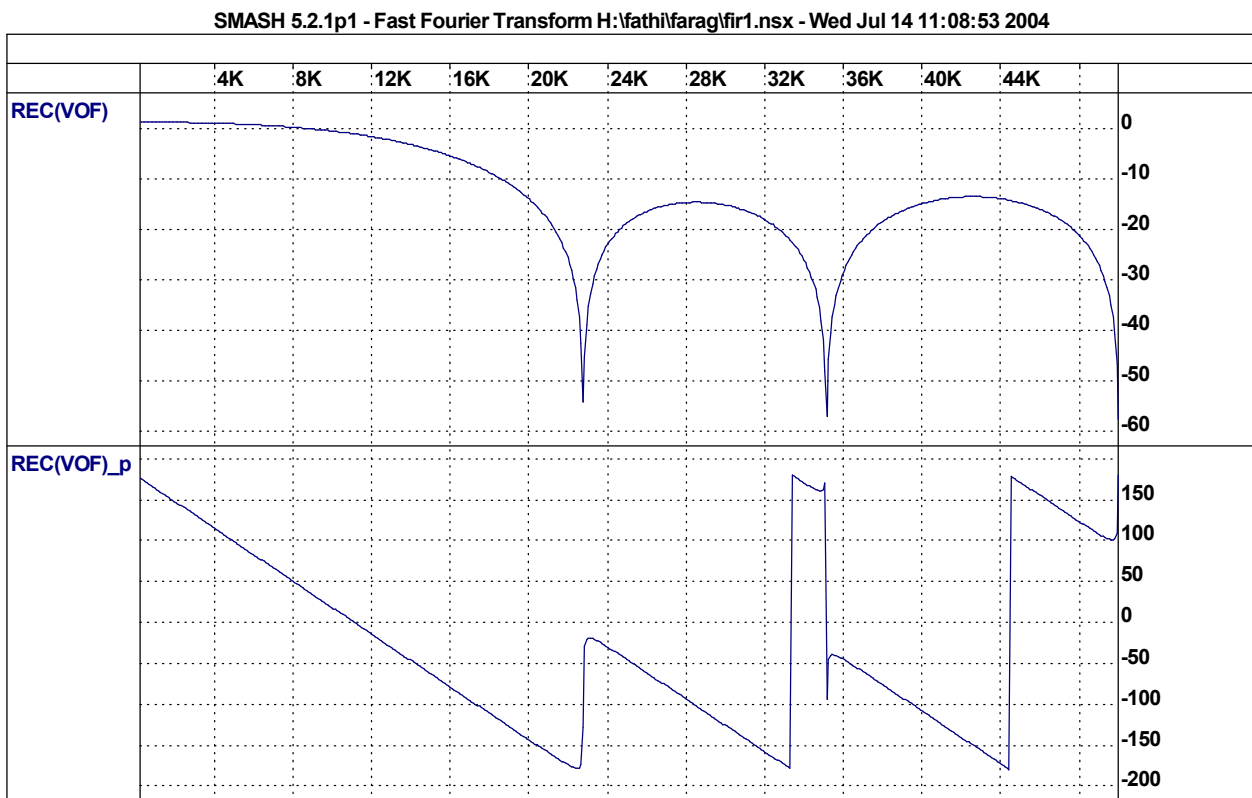


Fig. 6. The FIR frequency response