DESIGN OF AN ULTRA-LOW-POWER CURRENT SOURCE

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ABSTRACT

This paper presents the design of an ultra low-power self-biased current source. We have designed a 400pA current reference in both 1.5µm and 0.35µm CMOS technologies. The association of a very simple topology, an efficient design methodology, and low output conductance trapezoidal transistors has resulted in area of 0.046mm^2 and power consumption around of 2nW. Experimental results for the 1.5µm CMOS technology validate the design and show that the current source can operate from supply voltage down to 1.2V with a regulation better than 8%/V of supply voltage.

1. INTRODUCTION

The increasing demand for inexpensive very-low-power portable and implantable medical applications has resulted in the integration of low-voltage CMOS analog circuits compatible with standard VLSI technologies [1], [7]. This tendency has motivated the development of systematic methodologies for analog design. Furthermore, efficient, simple and easy-to-design analog circuit structures are highly desirable [2], [4], [6].

CMOS analog design based on the inversion level technique has been shown to be a robust alternative for high performance in very-low-power [3] and low-voltage circuits [2]. This technique uses the current as the main design variable. Thus, analog circuits based on such a design technique require a self-biased current source (SBCS) to operate at the nominal inversion level. Moreover, the generation of on-chip current references avoids the need for an extra pad to communicate with the external environment.

Several SBCS circuits are found in the literature [4] - [7], but a design methodology for easy reuse or design is not available yet. Our SBCS is based on the circuits proposed in [4], [5], [6], and [7], which have the same current dependence on temperature. Despite the simplicity of the circuit proposed in [4], it uses a resistor that for small currents (pA-nA) consumes a very large silicon area. To avoid the need for a resistor, the authors of [6] use a MOSFET working in the triode region to replace the resistor. Even though simple, the SBCS of [6] is not suitable for low voltage operation, as pointed out in [7]. Another implementation of an SBCS is presented in [5] but the large current gains and operation in strong inversion of some of its transistors degrade its power efficiency. Reference [7] presents another proposal of an SBCS, a less simple structure than the previously mentioned ones. The circuit in [7] uses a self-cascode MOSFET (SCM) in strong inversion and a PTAT voltage reference generated by means of a current ratio. Although appropriate for low voltage operation, the power efficiency of the current source in [7] is not high due to the use of slightly more complex structures and operation in strong inversion of some transistors.

This paper presents the design of a self-biased current source dedicated to technology-independent inversion level biasing, which is suitable for low-voltage and very low power applications. Our SBCS circuit uses MOSFET's only and can operate down to 1V supply voltage (in sub-0.18µm technologies this circuit can operate from 0.6V) and exhibits low sensitivity to supply voltage.

In Section 2, the ACM model [8] and the concept of inversion level are summarized. We develop the basic design equations for the SBCS using the ACM model in Section 3. Section 4 introduces the low-voltage CMOS SBCS. The design methodology to obtain the dimensions of the MOSFET's is formulated in Section 5. As a design example, a very low power SBSC is implemented in both 1.5µm and 0.35µm CMOS processes and the associated simulation and experimental results are presented in Section 6. Finally, concluding comments are presented in Section 7.

2. THE ACM MODEL

In the design methodology of the self-biased current source, we have employed ACM, a current-mode MOSFET model that uses the concept of inversion level [8]. According to the ACM model, the drain current can be split into the forward (I_F) and reverse (I_R) currents

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where

$$I_S = I_{SQ}\left(\frac{W}{L}\right) = I_{SQ}(S) \tag{2.a}$$

$$I_{SQ} = \mu C'_{ox}\, n \frac{\phi_t^{\,2}}{2} \tag{2.b}$$

$I_F(I_R)$ depends on gate and source (drain) voltages. In forward saturation, $I_F >> I_R$; consequently, $I_D \cong I_F = I_S i_f$. I_S is the normalization (specific) current and I_{SQ} is the sheet specific current (I_S for $W = L$), $i_{f(r)}$ is the forward (reverse) inversion level, and µ, n, C'_{ox}, ϕ_t, and $W/L=S$ are the mobility, slope factor, gate oxide capacitance/area, thermal voltage, and the transistor aspect ratio, respectively. The relationship between current and voltage is given [8] by

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \quad (3)$$

$$V_P \cong \frac{V_G - V_{T0}}{n} \quad (4)$$

where V_P is the pinch-off voltage and V_{TO} is the zero bias threshold voltage. More details about (1)-(4) can be found in [8].

The self-biased current-source circuit proposed here is an extractor of normalization (specific) current I_{SQ} [5] optimized for low-voltage and very low power applications.

3. DESIGN EQUATIONS FOR SCM AND SBS

The core of the SBCS is the SCM shown in Figure1. The V-I characteristic of the SCM is very appropriate for building low-voltage analog blocks such as current references and sub-100mV PTAT voltage references [3] – [7].

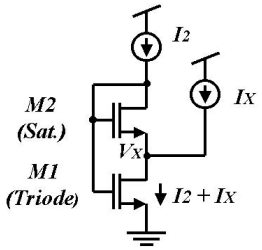


Figure 1. Schematic of the SCM connected in diode configuration (V_{B1}=V_{B2}=0).

The design equations (7)-(9) that describe the V-I characteristic of the SCM have been deduced using (1)-(3) and the schematic in Fig. 1. According to (1), the drain currents of M_1 and M_2 can be expressed as functions of the forward and reverse inversion levels

$$I_2 \cong I_{F2} = I_{S2} i_{f2} \quad (5)$$

$$I_{D1} = I_{F1} - I_{R1} = I_{S1}(i_{f1} - i_{r1}) = I_2 + I_x \quad (6)$$

Since V_{P1}=V_{P2}=V_P and V_{D1}=V_{S2}, then i_{r1}= i_{f2} [5]; thus, from (5) and (6) we can find the relationship between i_{f1} and i_{f2}

$$i_{f1} = i_{f2}\left[1 + \frac{S_2}{S_1}\left(1 + \frac{I_x}{I_2}\right)\right] \quad (7)$$

with the ratio I_X/I_2 defined by the gain of a PMOS current mirror.

The application of (3) to M_2 results in

$$\frac{V_P - V_x}{\phi_t} + 1 = \left(\sqrt{1+i_{f2}} - 1\right) + \ln\left(\sqrt{1+i_{f2}} - 1\right) \quad (8)$$

while, for M_1

$$\frac{V_P}{\phi_t} + 1 = \left(\sqrt{1+i_{f1}} - 1\right) + \ln\left(\sqrt{1+i_{f1}} - 1\right) \quad (9)$$

Equations (7), (8), and (9) with five unknowns (V_P, i_{f1}, i_{f2}, I_x/I_2 and V_X) have been instrumental in the development of the design methodology of the SBCS. If we assume that a voltage generator sets V_X at a given value and a (PMOS) current mirror defines I_x/I_2, the inversion levels i_{f1} and i_{f2} as well as the currents are readily determined. In the following, we show the implementation of a reference voltage for V_X.

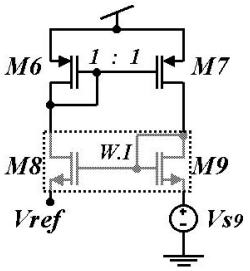


Figure 2. Self-biased structure (SBS)

The self-biased structure in Fig. 2 can be used to generate V_X at the intermediate node of the SCM [4]. The voltage V_{ref} can be calculated using (3) and assuming M_8-M_9 in weak inversion saturation. Noting that V_{P8}=V_{P9}, I_{D8}=I_{D9}, and V_{ref} =V_{S8}, then

$$V_{ref} = V_{S9} + \phi_t \ln(K) \quad \text{where } K = \frac{S_8}{S_9} \quad (10)$$

In our circuit topology, V_{S9} can be either zero or a PTAT voltage generated by means of a second SCM operating in weak inversion, as shown in Fig. 3. The application of expressions (7-9) to the SCM composed of M_3 and M_4 operating in weak inversion gives

$$V_{S9} = \phi_t \ln\left(1 + 2\frac{S_4}{S_3}\right) \quad (11)$$

Both PTAT voltage references expressed by (10) and (11) are immune to supply voltage as well as to technological parameters variations as long as the transistors operate in weak inversion. According to expression (11), in weak inversion the SCM can operate as a very-low-voltage PTAT reference, which is independent of current level and technology.

The previous equations and some considerations for design will be used in Section 5 to develop a design methodology appropriate for low voltage and very low power.

4. THE PROPOSED LOW-VOLTAGE SBCS

A simple version of our SBCS circuit is shown in Fig. 3, where V_{S9} can be either zero or $V_{X(WI)}$. We propose a simple power efficient SBCS circuit that replaces the resistor of the implementation in [4] with an SCM operating in moderate inversion to achieve the requirements of low current and low voltage operation.

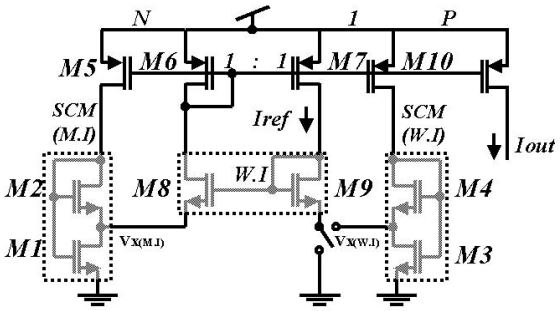


Figure 3. Self-biased current source circuit

When the switch in Fig. 3 is connected to ground, the PTAT voltage reference is produced by an intentional offset (K≠1 in Fig. 3) between MOS devices M_8 and M_9 both biased in weak inversion. In this case, the PTAT voltage is given by (10), with V_{S9}=0. This circuit simple topology is appropriate for applications where moderate performance is tolerated. Also, this circuit is stable for $K>1$ and is very accurate for $K \geq 10$ [7].

Another form for implementing the PTAT voltage reference can make use of a second SCM (M_3, M_4) biased in weak inversion and K=1; thus, $V_{ref}=V_{S9}$, with V_{S9} given by (11). This second implementation results in improved symmetry and matching of the structure and allows a simple implementation of M_8-M_9 with trapezoidal transistors [10], which are employed to improve regulation of the current reference without requiring a large silicon area.

5. DESIGN METHODOLOGY

The design specifications of the current reference are usually the minimum supply voltage (V_{DDmin}), power dissipation, silicon area, and sensitivities, in addition to I_{ref}, the value of the current itself.

The design methodology can be based on a maximum power supply or a current reference (I_{ref}) value, and the transistor dimensions are optimized to achieve low voltage operation.

This methodology can be applied to either the simple topology (switch connected to ground), or the symmetric topology (switch connected to node $V_{X(WI)}$) in Fig. 3.

The minimum supply voltage, which is determined by the constraints imposed by the two leftmost branches in Fig. 3, can be written as

$$V_{DD} \geq \max\{|V_{DSsat,P}| + V_{GS,M1}, |V_{GS,P}| + V_{DSsat,M8} + V_x\} \quad (12.a)$$

where $V_{DSsat,M8} \cong 100$mV since M_8 operates in weak inversion. The p-channel transistors are sized in order to operate in weak inversion, with an inversion level close to 1 or smaller; therefore, $|V_{DSsat,P} \cong 100\ \text{mV}|$ and $V_{GS,P} \cong V_{TP}$. Since V_X is less than 100 mV, and M1 operates in moderate inversion with $V_{GS,M1} \cong V_{TN} + 100$ mV we can use the first-order approximation

$$V_{DD} \geq \max\{|V_{TP}|, V_{TN}\} + 200mV \quad (12.b)$$

for the minimum supply voltage. Of course, expression (12.b) is a rough approximation for the minimum supply voltage.

In our design methodology, we have chosen the SCM to operate in moderate inversion with i_{f2}=3 or, equivalently, $V_{P2}=V_{x(M.I)}$ (please, see (8)). If $V_{S9}=0$, we can calculate i_{f1} from equation (9) or, equivalently, solve

$$1+\ln(K) = x + \ln(x) \quad (13)$$

for $x = \left(\sqrt{1+i_{f1}} - 1\right)$. Once x has been calculated for a given K, e. g. K=10, one can proceed to calculate S_2/S_1 from (7)

$$\frac{S_2}{S_1} = \frac{(x+1)^2 - 4}{3(1+1/N)} \quad \text{and} \quad S_2 = \frac{NI_{ref}}{3I_{SQ}} \quad (14)$$

For a current reference $I_{ref} << I_{SQ}$, $S_9=1$ keeps M_9 in weak inversion and the factor N defines a trade-off between power consumption and area. The aspect ratio (S_P) of the PMOS transistors M_5-M_7 (M_{10}) is calculated using (2.a), and a proper choice of the inversion level, usually less than 1 for low voltage applications.

For the design of the symmetric topology we have used the same previous methodology with K=1, and S_3, S_4 calculated from (11) for a given V_{S9}.

The sensitivity of the circuit to supply power is associated with the Early effect of M_7 and M_8. The Early effect can be reduced using long channel lengths that, however, demand large silicon area. One approach to obtaining long channel lengths with moderate area is the trapezoidal transistor proposed in [10].

6. RESULTS

To verify the design methodology and performance of the proposed circuit, the two topologies in Fig. 3 have been designed for both AMS-0.35µm and AMI-1.5µm CMOS technologies. A comparison of simulated results is given in Table I, Fig. 4 and Fig. 5 for I_{ref}=400pA, N=1, K=9→x=2.345, S_9=1, S_2/S_1=1.2 and for S_4/S_3=4. The transistor dimensions for the symmetric topology in AMI-1.5µm are presented in Table II.

A symmetric SBCS was implemented in a 1.5µm CMOS technology and occupies an area of 230x200µm^2. Simulation and experimental results are compared in Fig. 4(b) and Fig. 5(b). These results validate the design and show that the SBCS can operate from supply voltage slightly lower than $V_{TN}+|V_{TP}|$.

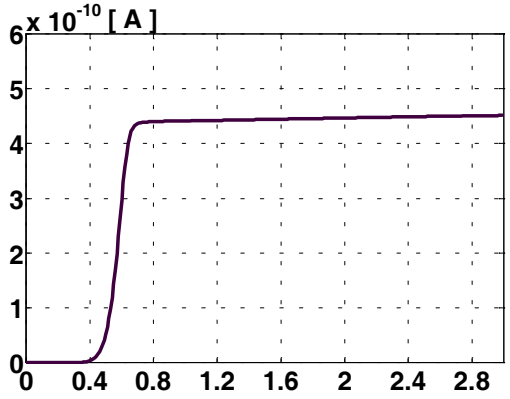
The measured sensitivities of the PTAT reference voltage and of the reference current to V_{DD} are below +0.1%/V and +8%/V, respectively. The average current reference of a five sample set with two different layouts is 410pA with maximum deviation of ±10% at 1.2V of supply voltage.

Table I: Summary of simulation results

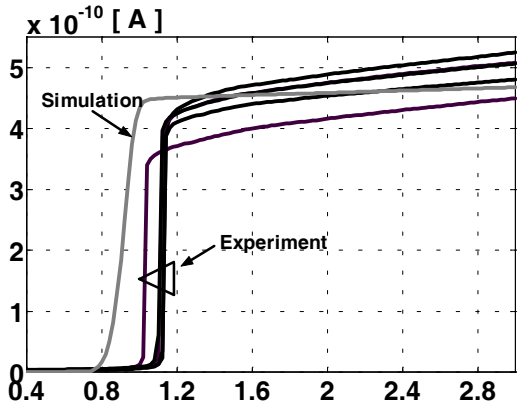
Parameter	Simple topology, K=9		Symmetric topology, K=1		Unit
	0.35µ	**1.5µ**	**0.35µ**	**1.5µ**	
V_{DDmin}	0.7	1.1	0.7	1.1	*V*
Power (V_{DDmin})	1.0	1.65	1.35	2.1	*nW*
V_{PTAT} PSRR(DC)+ at $V_{DD} \geq V_{DDmin}$	>70	>75	>90	>95	*dB*
Vref sensitivity toV_{DD}	+0.55	+0.87	+0.02	+0.03	*%/V*
Vref sensitivity to T	+0.3	+0.32	0.3	0.32	*%/°C*
Iref sensitivity to V_{DD}	+1.2	+2.7	+1.0	+2.5	*%/V*
Iref sensitivity to T	+0.06	+0.047	+0.06	+0.047	*%/°C*
$I_{SQN(P)_{0.35u}} = 65(22)nA$		$I_{SQN(P)_{1.5u}} = 28(10)nA$			

Table II: Transistor dimensions for the symmetric topology (AMI-1.5µm).

Parameter	M_1	M_2	M_3	M_4	$M_{5\text{-}7(10)}$	$M_{8\text{-}9}$
W [µm]	4	4	40	10	4	10
L [µm]	900	1080	10	10	16	10

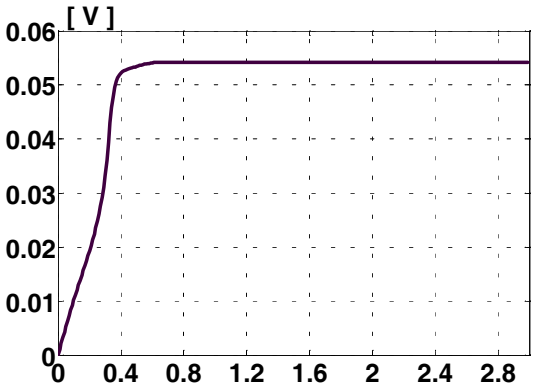


(a) Symmetric topology AMS- 0.35µm (Simulation)

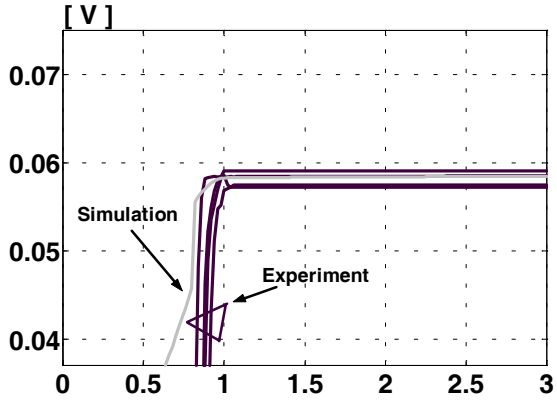


(b) Symmetric topology AMI-1.5µm

Figure 4. Current reference against supply voltage



(a) Symmetric topology AMS- 0.35µm (Simulation)



(b) Symmetric topology AMI-1.5µm

Figure 5. . PTAT voltage reference (Vx(w.i)) against supply voltage

7. CONCLUSIONS

A low-voltage low-power self-biased current-source has been proposed. Design equations based on the ACM model in any inversion level have been provided. The proposed circuits are process-independent and reproducible in any standard CMOS technology. Simulation and experimental results have shown that the self-biased current sources provide low-voltage, ultra-low-power operation and low sensitivity to changes in the supply voltage. The SBCS and design methodology proposed here are especially suited for very-low-power applications.

8. ACKNOWLEDGEMENTS

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