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Design of a Temperature-Compensated Voltage Reference based on the MOSFET Threshold Voltage

Daniel E. Silva Piovani
daniel.piovani@floripadh.com

Márcio Cherem Schneider
marcio@eel.ufsc.br

Topics

1. Temperature dependence of gate voltage in a diode connected MOSFET.

2. Compensation of temperature dependence through inversion level.

3. Voltage reference topology and design.

4. Simulations and measurements.

5. Conclusions.

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Temperature dependence of gate voltage in a diode connected MOSFET
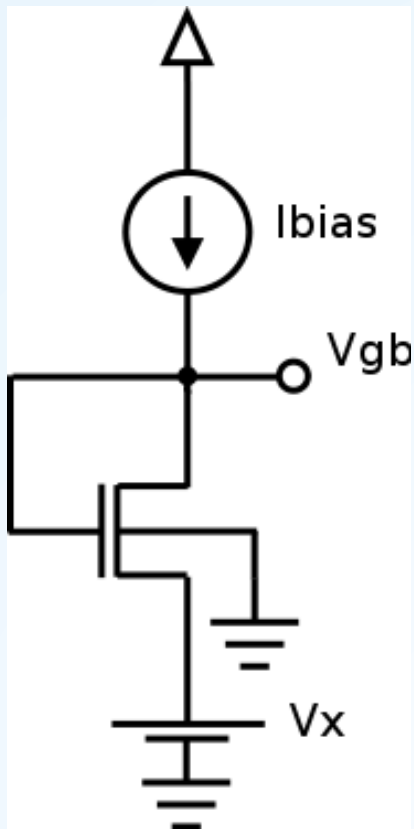
$$UICM: \quad \frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{i_{f(r)} + 1} - 2 + \ln\left(\sqrt{i_{f(r)} + 1} - 1\right) \quad (1)$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = F\left(i_{f(r)}\right) \qquad V_P \simeq \frac{V_{GB} - V_{TH}}{n}$$

$$V_{REF} = V_{GB} = V_{TH} + V_X + n\,\phi_t\,F\left(i_f\right) \quad (2)$$

1. $V_{TH} = V_{TH0} + \kappa_T T$, $\kappa_T < 0$ Linear Approximation

2. $V_X = \beta\,\phi_t$, $\beta > 0$ Source voltage proportional to thermal voltage

$$V_{REF} = V_{GB} = V_{TH0} \underbrace{+\kappa_T T}_{CTAT} + \underbrace{n\phi_t\left[\beta + F\left(i_f\right)\right]}_{PTAT} \quad (3)$$

V_{TH0} Threshold voltage at 0 K.

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Compensation of temperature dependence through inversion level

$$V_{REF} = V_{GB} = V_{TH0} \underbrace{+\kappa_T T}_{CTAT} + \underbrace{n\phi_t \left[\beta + F\left(i_f\right) \right]}_{PTAT} \quad (3)$$

$$\frac{\partial V_{REF}}{\partial T} = 0 \quad \rightarrow \quad \text{considering} \quad F(i_f) \text{ indepedent of temperature.}$$

$$F\left(i_f\right) = -\left(\frac{\kappa_T T}{n\phi_t} + \beta \right) = -\left(\frac{\kappa_T q}{n k_B} + \beta \right) \quad (4)$$

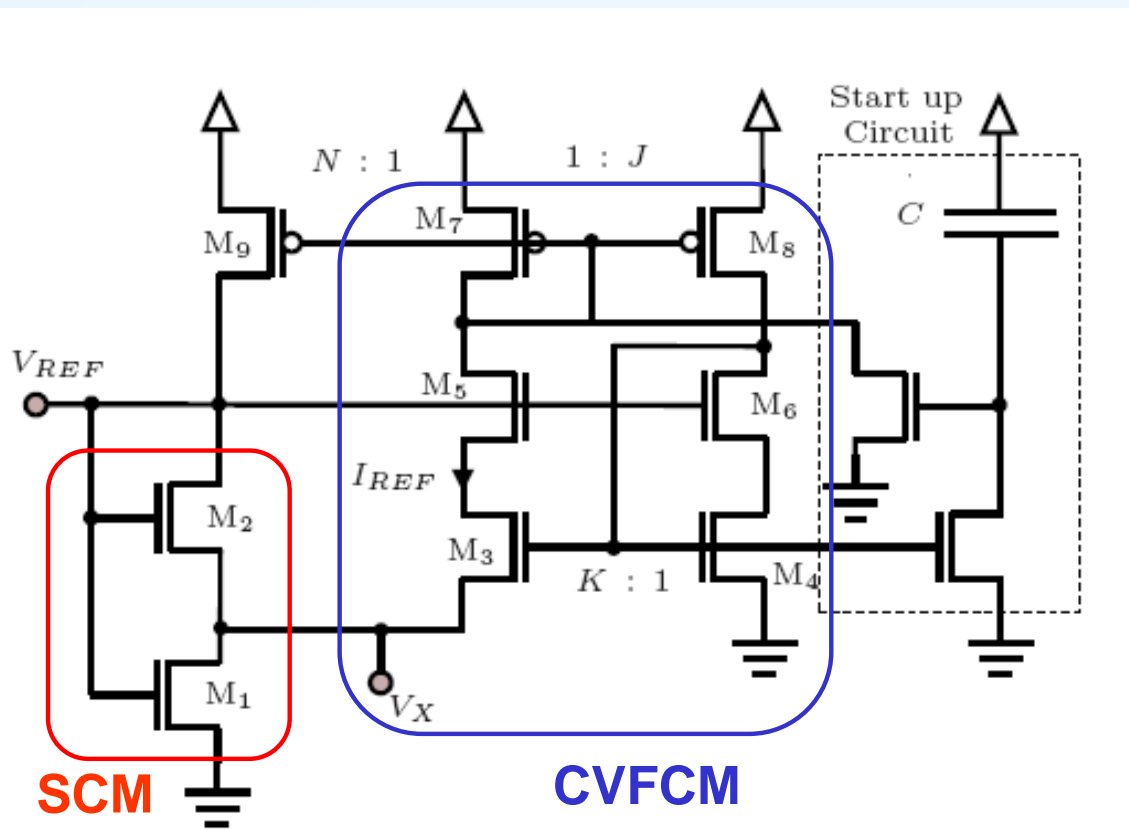Uncertainty in the slope factor value and its shift with temperature
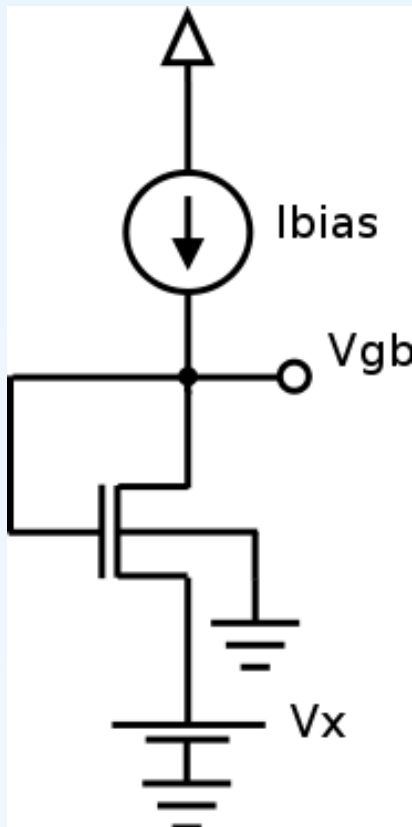
Design Challenge $\rightarrow$ biasing the MOSFET diode with a constant inversion level over the operating temperature range.

$$i_f = \frac{I_D}{I_{SQ} S} \quad \Longrightarrow \quad I_D \propto I_{SQ}$$

Drain current proportional to the specific current for constant i_f

Voltage reference topology and design

Self-biased Current Source

SCM

CVFCM

SCM : Self-cascode MOSFET (M_{1-2})

CVFCM : Cascode voltage follower

current mirror (M_{3-8})

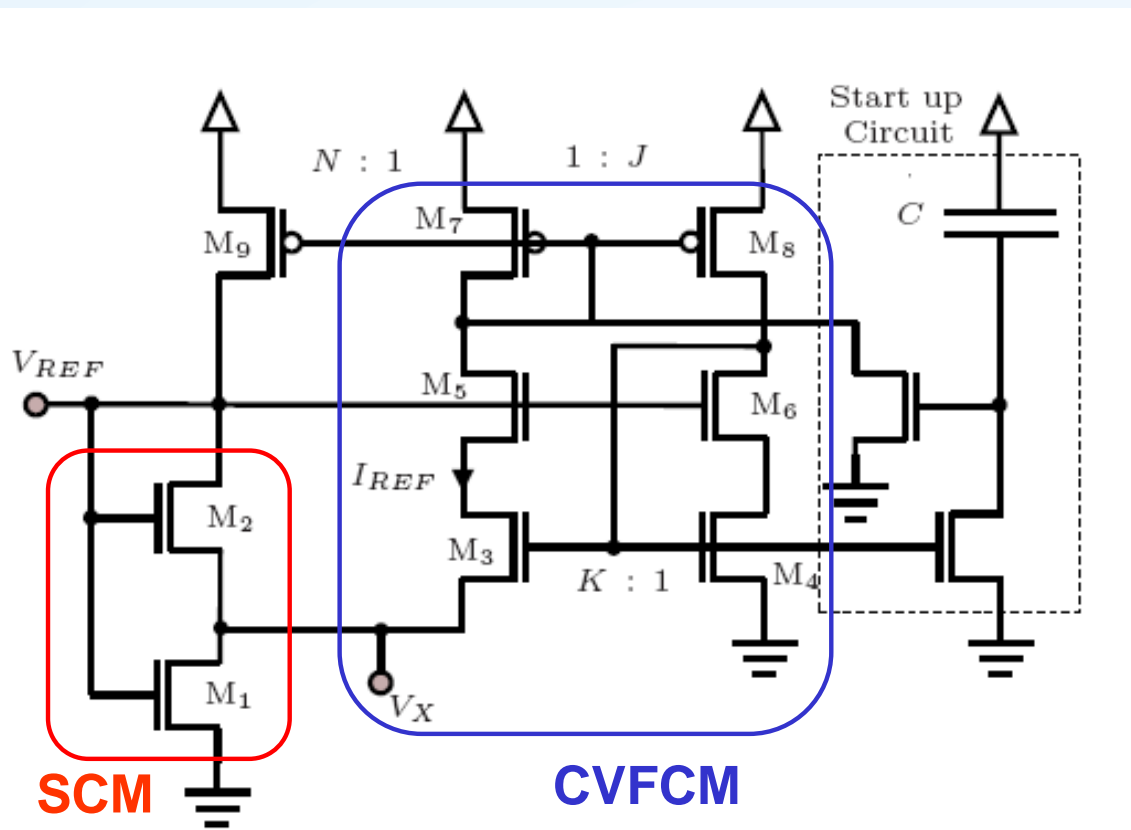### Strategy 1

Use the SBCS current to bias a MOSFET diode.

Strategy 2

Design the SCM inversion levels for compensating the temperature dependence of V_{GB} of M_{1-2}.

E. Camacho-Galeano, C. Galup-Montoro, and M. Schneider. A 2-nW 1.1-V self-biased current reference in CMOS technology. *IEEE Transactions on Circuits and Systems II: Express Briefs.*

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Voltage reference topology and design

Self-biased Current Source

SCM

CVFCM

CVFCM

$$V_X = \phi_t \left[F(i_{f3}) - F(i_{f4}) \right] \simeq \phi_t \ln[JK] \ \textbf{\textit{W.I.}}$$

SCM

$$V_X = \phi_t \left[F(i_{f1}) - F(i_{f2}) \right]$$

Design value for V_X is aprox. $3\phi_t$ ($\beta = 3$).

Inversion level compensation

$$\kappa_T = -1.528 \ mV / K \ (CMOS \ 0.5 \ \mu m)$$

$$F(i_{f2}) = -\left(\frac{\kappa_T q}{n k_B} + \beta \right) = 11.17 \rightarrow i_{f2} \simeq 120$$

$$I_D = I_{SQN} S_2 i_{f2} \rightarrow S_2 = 3/100 \quad I_{D2} = 160 \, nA$$

$$N = 2 \rightarrow I_{REF} = 80 \, nA$$

E. Camacho-Galeano, C. Galup-Montoro, and M. Schneider. A 2-nW 1.1-V self-biased current reference in CMOS technology. *IEEE Transactions on Circuits and Systems II: Express Briefs.5*

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Simulations

1. Temperature Coefficient (TC)

2. Line Regulation (PSRR DC)

3. PSSR AC

4. Power Consumption

5. Minimum Operation Voltage

6. Startup Time

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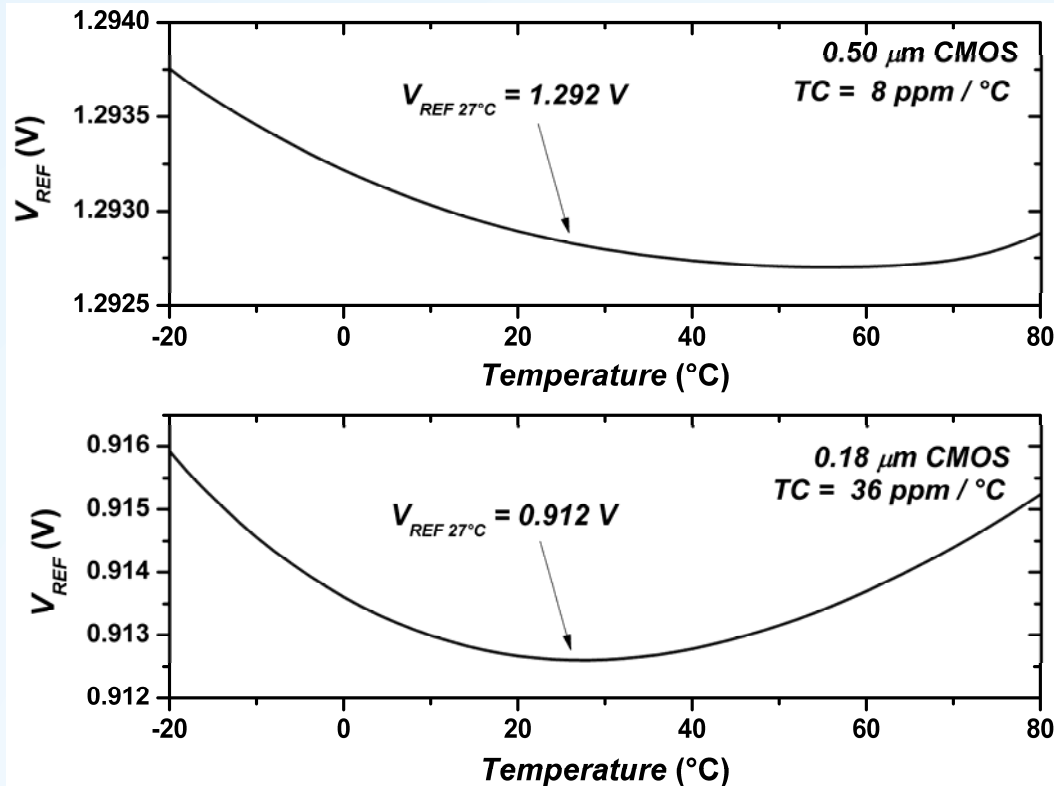
Simulations

Figure 1 – Simulated output voltage (V_{REF}) as a function of the temperature .
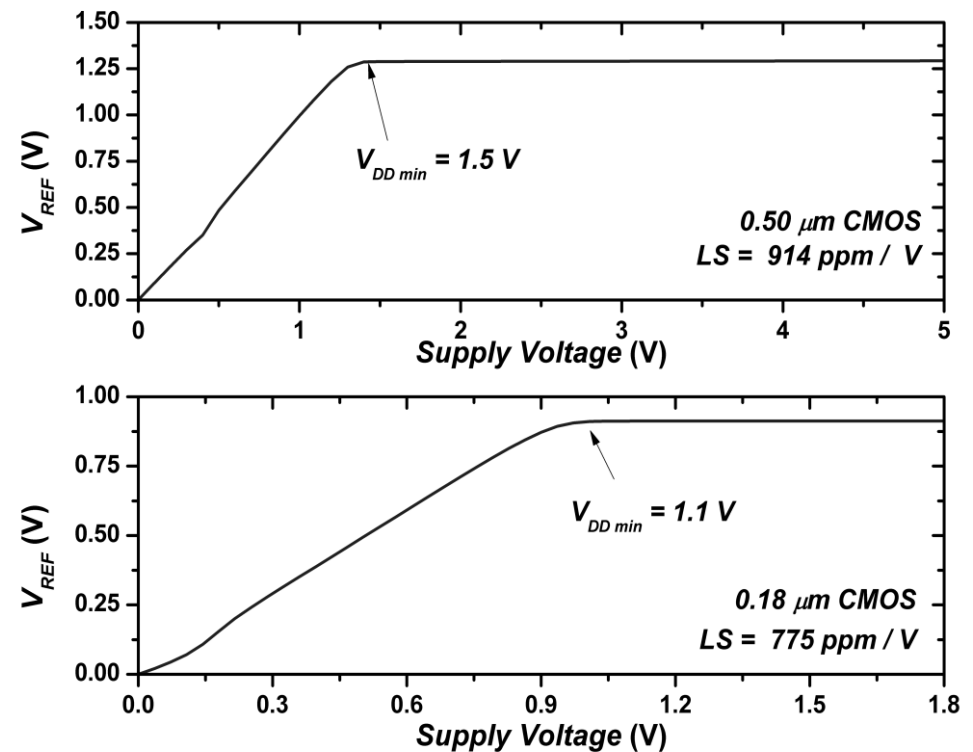
Figure 2– Simulated output voltage (V_{REF}) at room temperature as a function of the power supply.
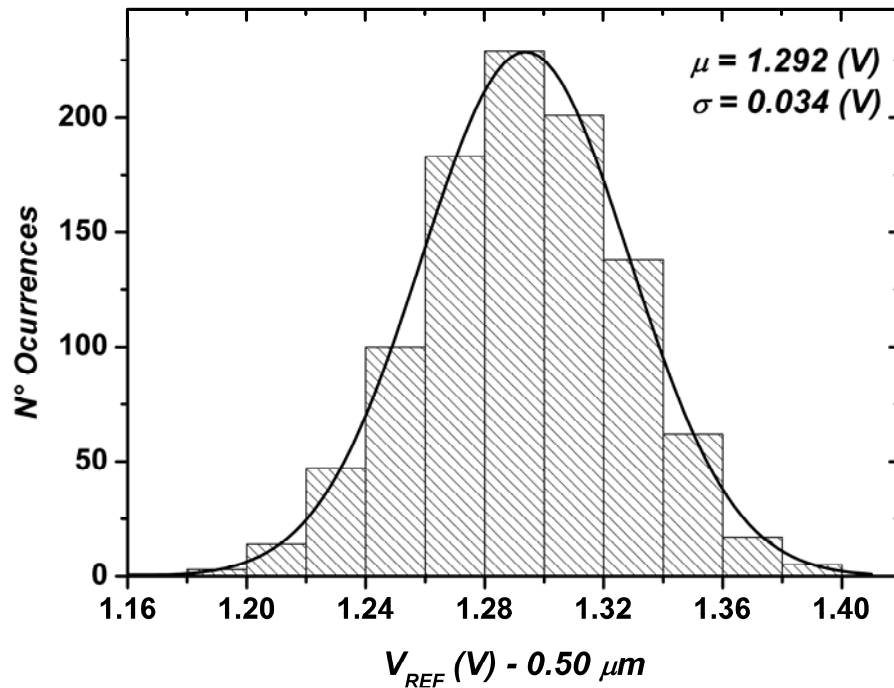
Simulations

Figure 3 – Distribution of the voltage reference obtained from Monte Carlo simulations for the 0.50 μm technology.
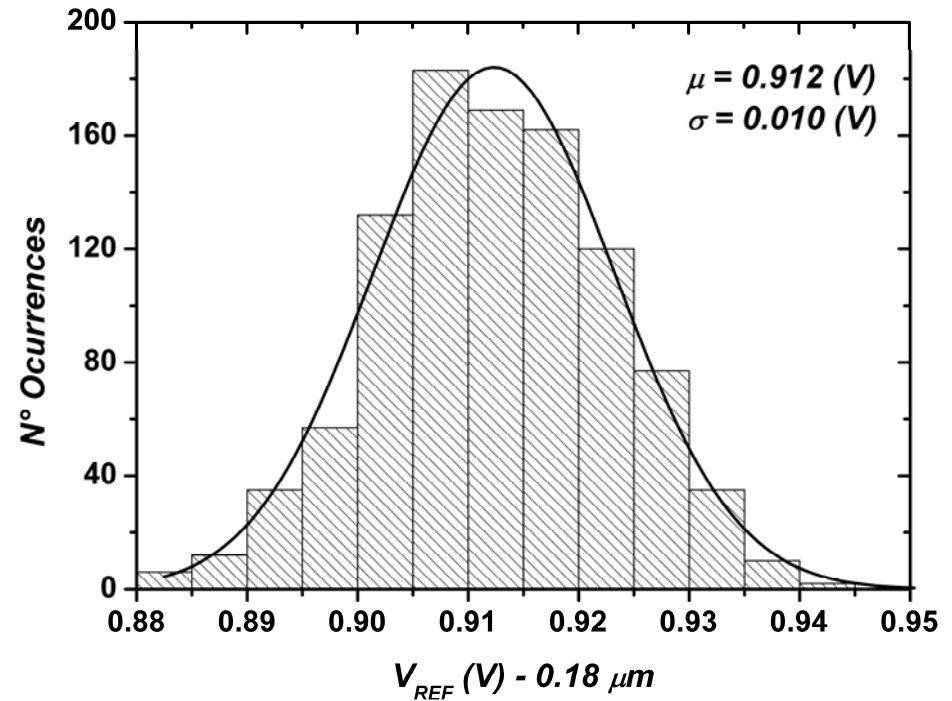
Figure 4– Distribution of the voltage reference obtained from Monte Carlo simulations for the 0.18 μm technology.

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Measurements
(The ugly truth and the not so ugly ...)

1. Difference between the simulated and the measured current. From 79 nA to 50.5 nA.
2. Difference between the simulated and the measured voltage reference. From 1.292 to 1.166 V.
3. The voltage reference was over compensated showing a PTAT characteristic.

1. Low standard deviation in the measured samples, σ = 3.9 mV (five samples).
2. Voltage reference presents linear dependence on the temperature, trimming technique could be applied to adjust the compensation ratio.
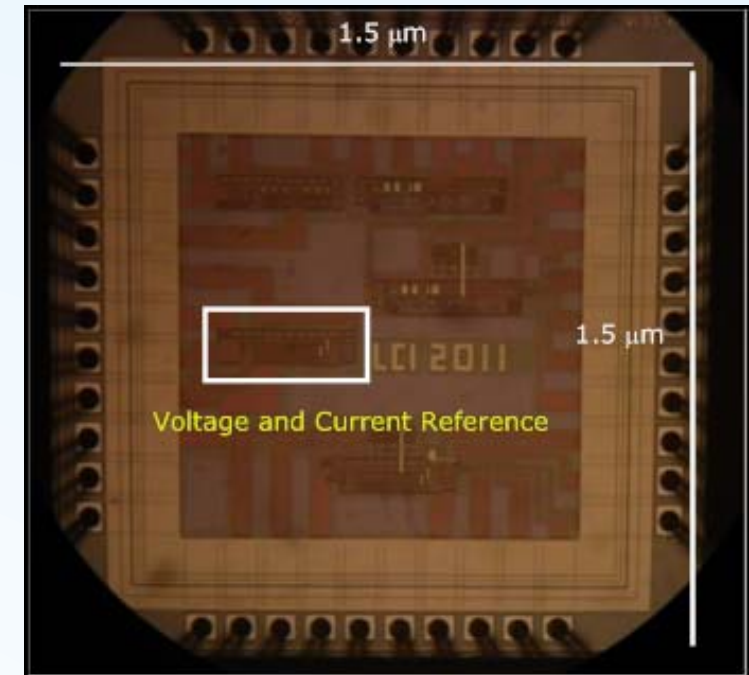
Figure 5 – Micrograph of the IC fabricated in CMOS 0.50 μm.

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Measurements
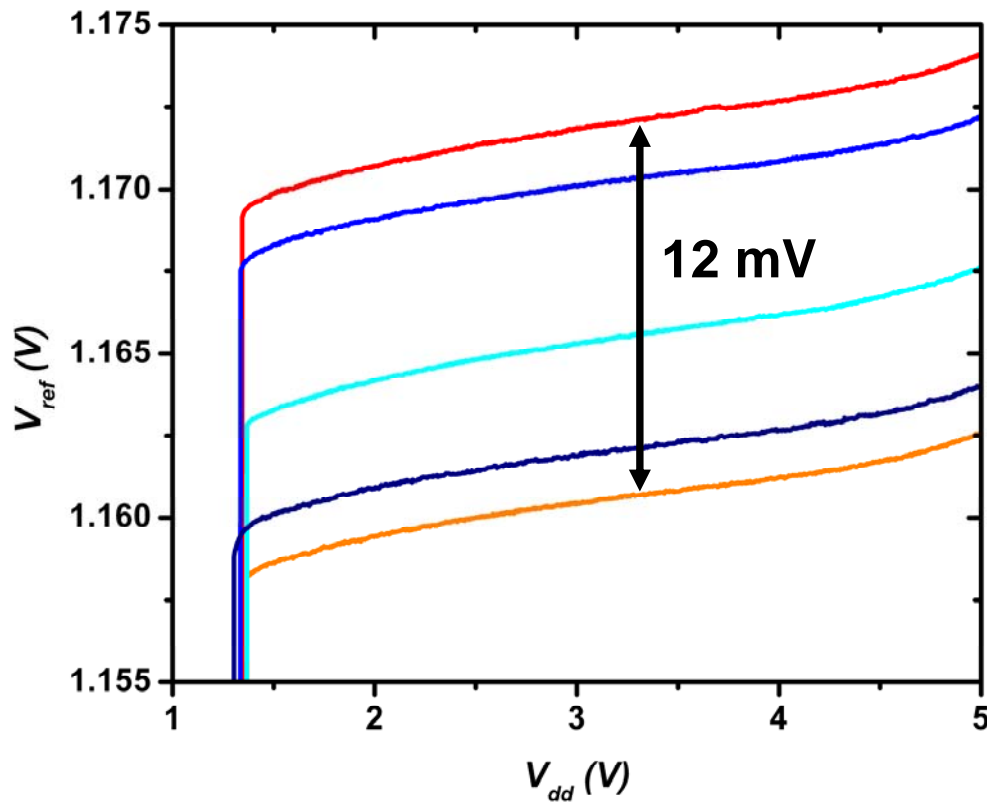## (The ugly truth and the not so ugly ...)

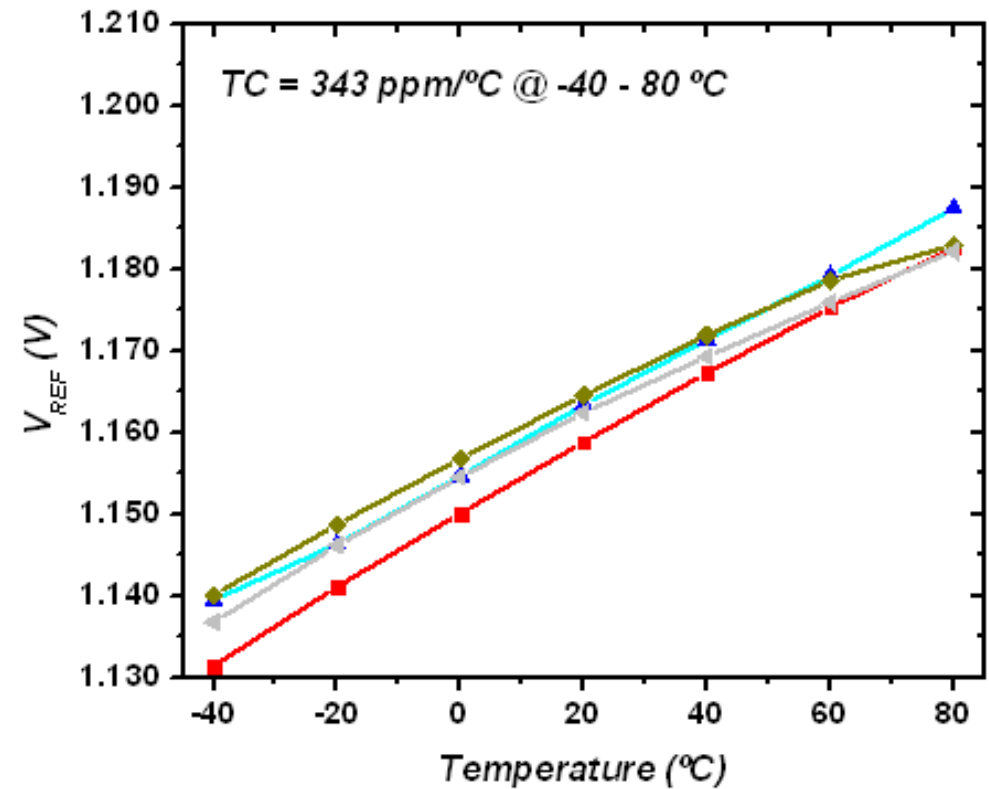**Figure 6 – Measured voltage reference for the 5 samples as a function of the supply voltage.**

Figure 7 – Measured voltage reference in four samples as a function of the temperature.

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Results

	Simulation	Measurements (5 IC)
Temp. range	-20 - 80 ºC	-20 - 80 ºC
V_{DD}	1.5 – 5 V	1.4 – 5 V
V_{REF}	1.292 V	1.166 V ($\sigma = 3.9\ mV$)
I_{REF}	79 nA	50.5 nA ($\sigma = 0.84$ nA)
Power @ 25 ºC	465 nW @ 1.5 V	303 nW @ 1.5 V
TC(V_{REF})	8 ppm/K	342 ppm/K
LS (V_{REF})	912 ppm/V	1032 ppm/V
PSRR	-59 dB @ 100 Hz	Not measured yet
Chip Area	0.027 mm^2	

Conclusions

- A design methodology for a MOSFET-only temperature-compensated voltage reference was presented.

- The presented results shows a promising use of this kind of voltage-current reference in applications where area, power consumption and supply voltage are critical constraints.

- If precision in the voltage reference temperature dependence is required, a trimming technique can be easily added to the circuit.
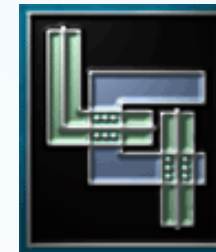
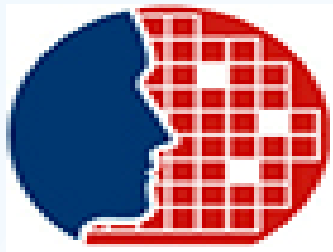**Universidade Federal de Santa Catarina**

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Thanks for your attendance

¿¿ Questions ??