Design of a Temperature-Compensated Voltage Reference based on the MOSFET Threshold Voltage

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ABSTRACT

In this paper, the analysis and design of a temperature-compensated reference based on the MOSFET threshold voltage is presented. The circuit, which core is a specific current generator, explores the temperature behaviour of the gate-bulk voltage of an NMOS transistor. The transistor is chosen to operate in a region where a PTAT voltage compensates the CTAT characteristic of the threshold voltage. The design is validated through simulation results in different standard CMOS processes. For a low power 0.18 μm CMOS process, the voltage reference is 0.912 V and the current reference is 78.68 nA. The temperature coefficient of the voltage reference is 36 ppm/°C in the range from -20 to 80 °C. The line sensitivity is 775 ppm/V for a supply voltage range of 1.1 - 1.8 V, and the power supply rejection ratio (PSRR) is -55 dB at 1 kHz. The power dissipation is 346 nW at room temperature. The chip area is 0.0084 mm².

Categories and Subject Descriptors
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General Terms
Design.

Keywords
CMOS, voltage-current reference, analog design, compact model, low-power low-voltage.

1. INTRODUCTION

Voltage and current references are some of the most important building blocks in integrated circuits. Their use covers operational amplifiers, comparators, A/D and D/A converters. Traditionally, bandgap references are widely used in integrated circuits [3,11,17]. Depending on the particular topology the output voltage is around 1.2 to 1.3 V, which is close to the theoretical bandgap voltage of silicon at 0 K. Taking advantage of the parasitic bipolar transistors present in CMOS standard technology this kind of circuit was adapted to the CMOS process. However, the advance of the technology and the search for ultra low power circuits results in a reduction of the supply voltage to sub-1V operation, thus reducing the applicability of the bandgap references. One approach to obtain a bandgap reference with sub-1-V operation is presented in [2]. Its drawback is the necessity of resistors of several hundred megohms to achieve low-power operation.

In the last years, the focus of the reference circuits is pointing to the CTAT (complementary to absolute temperature) behaviour of the MOSFET threshold voltage [7]. A great number of papers were published following this new direction [1, 6, 9, 12, 15]. However, none of these papers use compact model equations, confining the design to the MOSFET operating in either weak or strong inversion, thus, hindering designers from finding the best trade-off between power consumption and circuit area. This work explores compact model equations using the inversion coefficient to help the design of temperature-compensated references. A simple design procedure, applied to the design of a low-power, low-voltage reference in two different CMOS standard technologies is presented. Our circuit uses the resistor-less specific current generator described in [4] to generate a voltage reference.

This paper is organized as follows: after the introduction, a review of a compact MOSFET model is presented in Section 2. Then, in Section 3, the operating principle and the equations for temperature compensation is shown. Section 4 is dedicated to develop the circuit configuration and design. Simulation results are presented in Section 5 and finally, in Section 6 some final remarks are elaborated.

2. MOSFET MODEL

According to the all-region MOSFET model, the drain current of a long channel transistor can be split into the symmetric forward (I_f) and reverse (I_r) components, which are dependent on the transistor sheet specific current (I_{SQ}), aspect ratio (S = W/L), and forward (i_f) and reverse (i_r) inversion levels.

\[ I_D = I_F - I_R = I_{SQ} S (i_f - i_r) \] (1a)

\[ I_{SQ} = \mu C_{ox} n \frac{\phi_H^2}{2} \] (1b)
At this point, two linear approximation are made to obtain simple equations for the reference voltage and its dependence on the temperature. The first one, is the linear approximation of the pinch-off voltage around $V_{GB} \approx V_{TH}$ giving by,

$$V_P \approx \frac{V_{GB} - V_{TH}}{n}$$

(6)

where $n$ is the slope factor [8].

The second linear approximation is about the dependence of the transistor’s threshold voltage on the temperature, which is considered to decrease linearly, represented by,

$$V_{TH} = V_{TH0} - \kappa_T T$$

(7)

where $V_{TH0}$ is the extrapolated threshold voltage at $T = 0 \, \text{K}$ and $\kappa_T$ is the temperature coefficient for $V_{TH}$. For a first hand-made calculation $\kappa_T$ can be inferred from the BSIM3V3 model parameter $\kappa_{F1}$ [16].

Applying (6) and (7) in (5), the reference voltage ($V_{REF}$) can be expressed as,

$$V_{REF} = V_{GB} = V_{TH0} - \kappa_T T + n[V_X + \phi_t F(i_f)]$$

(8)

In [6] the $V_X$ voltage is set to zero, but we can set this node to a voltage with a PTAT characteristic, allowing the temperature compensation with lower values of inversion level as shown in [12, 15]. This can be achieved if $V_X$ is proportional to the $\phi_t$ ($V_X = \beta \phi_t$). Considering $V_X$ with a PTAT characteristic, expression (8) can be modified to

$$V_{REF} = V_{TH0} - \kappa_T T + n[\phi_t (\beta + F(i_f))]$$

(9)

In order to have a temperature compensated voltage reference, the following condition must be satisfied:

$$\frac{\partial V_{REF}}{\partial T} = 0$$

(10)

From (9), it is easy to demonstrate that this condition is obtained when the CTAT term $\kappa_T T$ equals the PTAT term $n\phi_t (\beta + F(i_f))$, inferring the existence of a $i_f$ value which cancel the temperature dependence of $V_{REF}$.

$$F(i_f) = -\frac{\kappa_T T}{n\phi_t} + \beta = -\frac{\kappa_T q}{nk_B} + \beta$$

(11)

The design challenge is to produce a constant inversion level over the operating temperature range to get a continuous compensation. To achieve this behaviour let us analyze the definition of the inversion level and its temperature dependence. According to (1a) the forward inversion level of a saturated MOSFET depends on the drain current ($I_D$), the sheet specific current ($I_{sq}$) and the aspect ratio ($S = W/L$). Neglecting variations of the aspect ratio and the slope factor ($n$) with the temperature, to get an inversion level independent from temperature variations, the drain current must be proportional to the specific current.

4. CIRCUIT CONFIGURATION

The schematic of the voltage reference circuit, illustrated in Fig. 2, is the self-biased current source (SBSC) presented in [4], which generates a current proportional to the specific current. The cores of the SBSC are the self-cascode MOSFET circuit (SCM - transistors $M_1, M_2$) and the cascode voltage follower current mirror circuit (CVFCM - transistors...
Table 1: Transistor Sizes for the 0.18-µm and 0.50-µm CMOS voltage reference.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Process</th>
<th>Value (W / L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M_1</td>
<td>0.5-µm CMOS</td>
<td>3 µm / 40 µm = (3 µm / 20 µm) × 1/2, 3.5µm / 60 µm = (3.5 µm / 20 µm) × 1/3</td>
</tr>
<tr>
<td>M_2</td>
<td>0.5-µm CMOS</td>
<td>3 µm / 100 µm = (3 µm / 20 µm) × 1/5, 3.5 µm / 80 µm = (3.5 µm / 20 µm) × 1/4</td>
</tr>
<tr>
<td>M_3</td>
<td>0.5-µm CMOS</td>
<td>720 µm / 2 µm = (30 µm / 2 µm) × 24, 480 µm / 2 µm = (20 µm / 2 µm) × 24</td>
</tr>
<tr>
<td>M_4</td>
<td>0.5-µm CMOS</td>
<td>60 µm / 2 µm = (30 µm / 2 µm) × 2, 40 µm / 2 µm = (20 µm / 2 µm) × 2</td>
</tr>
<tr>
<td>M_5-M_6</td>
<td>0.5-µm CMOS</td>
<td>20 µm / 20 µm = (20 µm / 20 µm) × 1, 20 µm / 20 µm = (20 µm / 20 µm) × 1</td>
</tr>
<tr>
<td>M_7-M_8</td>
<td>0.5-µm CMOS</td>
<td>50 µm / 20 µm = (10 µm / 20 µm) × 5, 20 µm / 20 µm = (20 µm / 20 µm) × 1</td>
</tr>
<tr>
<td>M_9</td>
<td>0.5-µm CMOS</td>
<td>100 µm / 20 µm = (10 µm / 20 µm) × 10, 40 µm / 20 µm = (20 µm / 20 µm) × 2</td>
</tr>
</tbody>
</table>

Figure 2: Schematic of the proposed voltage reference circuit.

M_3, M_4, M_5, M_6, M_7, and M_8. Transistor M_0 acts as a current source to bias the SCM. The bulks of the NMOS transistors are connected to ground, while those of the PMOS transistors to V_{DD}. The reference voltage is obtained from V_{GD} (= V_{REF}) of the SCM. M_2 is designed to operate at an inversion level (i_f) that compensates the CTAT behaviour of the threshold voltage (V_{TH}), according to (11).

4.1 Circuit Design

CMOS standard technologies 0.50-µm and 0.18-µm were employed for the design of the voltage references, as in Fig. 2. The threshold voltage and specific current were extracted using the methodology described in [8], obtaining 0.858 V and 0.623 V for V_{TH} and 63 nA and 107 nA for I_{SQ}, for the 0.5-µm and 0.18-µm technologies respectively. All the design equations are described in [4]. The operating point of the SBC circuit is established when the SCM and CVFCM have the same V_X voltage, which depends on the ratio of currents determined by the current mirrors. The reference current (I_{REF}) generated for both SBCS was set to 80 nA. In our design the CVFCM is operating in weak inversion. The value of V_X was set to 3φ_L. Applying (11) for V_X = 3φ_L, (β = 3), n = 1.2 and the κ_T of the technologies (κ_T0.50µm = 1.528 mV/K - κ_T0.18µm = 0.907 mV/K), the inversion levels were 120 and 30 for the 0.50µm and 0.18µm technologies, respectively. With the values of the inversion levels and N, we could calculate the aspect ratio of transistors M_1 and M_2. N was set to 2 with the aim of reducing the area of the SCM. Transistor areas were chosen greater than 60 µm^2 to reduce mismatch effects, with a channel length of at least 2 µm. Some adjustments had to be done with the aid of the simulator for the determination of final transistor dimensions. The main reasons for this fine tuning are: approximation (6), valid for inversion levels around i_f = 3, and the uncertainty in the n value and its shift with temperature, which has an important impact on the determination of i_f when (11) is applied. Table 1 gives transistor widths (W) and lengths (L).

4.2 Minimum Supply Voltage

The minimum supply voltage (V_{DDmin}) is determined by the constraints imposed by the two leftmost branches in Fig. 2, which can be written as

\[ V_{DDmin} > \max \{ |V_{DSat,M_0}| + V_{REF}, |V_{GS,M_4}| + V_{DSat,M_5} + |V_{DSat,M_5} + V_X \} \] (12a)

where the saturation voltages of M_3, M_5 and M_4 are lower than 125 mV since all transistors operate with 0.5 < i_f < 2. The right branch is not in the critical path for the minimum power supply determination because transistor M_4 is set to weak inversion whereas M_1 is set to strong inversion, imposing the relationship V_{GS,M_4} > V_{GS,M_4}. V_X was chosen equal to 3φ_L and M_7 has the same inversion level as M_4 (i_f ≃ 1); therefore, the voltage V_{GS,M_7} ≃ V_{TH}. With the last design considerations expression (12a) can be approximated by (12b).

\[ V_{DDmin} > \max \{ V_{REF} + 125 mV, |V_{TH}| + 350 mV \} \] (12b)

Although (12b) is a rough approximation, it is very useful for predicting the minimum supply voltage required to turn on the current reference circuit.

5. SIMULATION RESULTS

The designed reference circuits are validated with Cadence® simulations, using BSIM3V3 model provided by the foundries. DC and AC simulations were run to extract the nominal current and voltage reference values, the temperature coefficient (TC), the line sensitivity (LS), and the power supply rejection ratio (PSRR). Figure 3 shows the
simulated reference voltage as a function of the temperature in the range from -20 to 80 °C. The nominal reference voltage was 1.292 mV for the 0.50-μm and 912.5 mV for the 0.18-μm CMOS technologies. The calculated temperature coefficients were very small 8 ppm/°C and 36 ppm/°C, respectively. The calculated temperature coefficients were very small 8 ppm/°C and 36 ppm/°C, respectively. The nominal reference current was 79.05 nA for the 0.50-μm and 78.68 nA for the 0.18-μm CMOS reference, both very close to the design value of 80 nA. Figure 4 exhibits the simulated reference voltage at room temperature as a function of the supply voltage. The minimum supply voltage is 1.4 V for the 0.50-μm and 1.5 V for the 0.50-μm CMOS technology respectively.

Table 2: Simulated Performance of the designed low-power CMOS voltage reference.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.50-μm CMOS</th>
<th>0.18-μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp. range</td>
<td>-20 - 80 °C</td>
<td>-20 - 80 °C</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5 - 5 V</td>
<td>1.1 - 1.8 V</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>1.292 V</td>
<td>0.912 V</td>
</tr>
<tr>
<td>$I_{REF}$</td>
<td>79.05 nA</td>
<td>78.68 nA</td>
</tr>
<tr>
<td>Power</td>
<td>465 nW (@1.5 V)</td>
<td>346 nW (@1.1 V)</td>
</tr>
<tr>
<td>Room temp.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TC ($V_{REF}$)</td>
<td>8 ppm/°C</td>
<td>36 ppm/°C</td>
</tr>
<tr>
<td>LS ($V_{REF}$)</td>
<td>912 ppm/V</td>
<td>775 ppm/V</td>
</tr>
<tr>
<td>LS ($I_{REF}$)</td>
<td>0.44 %/V</td>
<td>1.35 %/V</td>
</tr>
<tr>
<td>PSRR</td>
<td>-59 dB (@100 Hz)</td>
<td>-72 dB (@100 Hz)</td>
</tr>
<tr>
<td></td>
<td>-49 dB (@1 kHz)</td>
<td>-55 dB (@1 kHz)</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.027 mm$^2$</td>
<td>0.0084 mm$^2$</td>
</tr>
</tbody>
</table>

To study the dependence of the circuit outputs on process variations, corners and Monte Carlo simulations were performed. For the Monte Carlo analysis, mismatch and process variations were assumed, using a Gaussian distributions for the statistical parameters determination considering a 6σ range. Table 3 presents the corners simulations results, showing a great dispersion of the $V_{REF}$ value due to process variations. However, the $V_{REF}$ thermal coefficient did not present significant variation, explained by the fact that both the threshold voltage thermal coefficient and the inversion level have low dependence on process variations.

Monte Carlo simulations, depicted in Fig. 5 and Fig. 6, show a standard deviation of 34 mV and 10 mV, presenting a variation coefficient ($σ/μ$) of 2.6 % and 1.1 %, for the 0.50-μm CMOS and 0.18-μm CMOS respectively.

6. CONCLUSIONS

To validate the procedure, two different CMOS standard technologies were used to design current-voltage references. The simulation results agreed very well with theory; moreover, a great reduction in area was achieved comparing with published work [5, 6, 10, 13, 15]. Variations in both the reference voltage/current and in the temperature coefficient due to process variation were evaluated through Monte Carlo
simulations, which showed a small deviation of the temperature coefficient in the tested technologies. Variations in the reference value could be corrected through a trimming approach.

7. ACKNOWLEDGMENTS
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8. REFERENCES