Wideband Ring VCO for Cognitive Radio Five-Port Receiver

Francisco de Assis Brito Filho
LSI-TEC IC Design House
Rua Paes Leme, 524, 9o. andar
São Paulo, SP, Brazil, 05424-904
britofilho@ieee.org

Fernando Rangel de Sousa
Federal University of Santa Catarina
Electrical Engineering Department
Florianopolis, SC, Brazil, 88040-900
fernando.rangel@eel.ufsc.br

ABSTRACT

This paper presents an wideband ring VCO for cognitive radio five-port based receivers. Also presents testbenches to demonstrate the improvement of five-port architecture in homodyne receivers. A three-stage differential topology using transmission gates was adopted to implement the VCO in order to maintain wide and linear tuning range and a low phase-noise. Monte-carlo analysis were performed for evaluating the phase-shift response, which should be 120^o between stages. Those analysis will be used to develop a behavioral model of the VCO with focus on five-port receiver simulations allowing time-saving. It was observed a fairly linear correlation between control voltage and oscillation frequency in the range between 200 MHz and 1800 MHz. The VCO was designed for IBM 130nm CMOS technology.

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: Miscellaneous

General Terms

Design

Keywords

Cognitive Radio, Software Defined Radio, Five-Port, RF Receivers, Wideband Receivers, Wideband Oscillators, Ring VCO

1. INTRODUCTION

Many communication systems like TV broadcast, internet and cellphone mobile data transmission needs wide frequency bandwidth. For suitable signal reception, wideband receivers are necessary. Also, the receivers should present a wide frequency tuning range because of the large number of channels to be selected, which is often achieved by means of voltage controlled oscillator (VCO). Recently a new concept of efficient spectrum usage has gained attention, the Cognitive Radio (CR). It is a revolutionary technology that aims the use of unoccupied spectrum spaces while maintaining the rights of the primary services for their first users through continous spectrum sensing [1]. CR systems are developed in a Software Defined Radio (SDR) platform and current SDR requirements are wideband, larger frequency tuning range, low power consumption, low cost and reconfigurability [2].

An way to implement a SDR platform is using a RF frontend to translate RF signal to a baseband signal then process the information. Homodyne receivers may be an way to implement this RF frontend with the characteristics needed for SDR implementation like low cost, low power consumption and integrability [3]. However hetereodyne receivers have some problems that may become the architecture impracticable like DC offsets and high sensibility to even order distortions. An homodyne receiver implementation based on five-port correlator may improve its performance attenuating those problems. This type of implementation is known as five-port receiver [4].

In this paper we propose an wideband ring VCO for a five-port receiver, that can be used for SDR receiver implementation. Section II provides considerations about RF receivers and proposes a five-port receiver for SDR implementation, comparing it with a quadrature homodyne receiver and showing its improvement. The wideband VCO suitable for five-port receivers is showed and their analysis is provided in section III. Section IV presents the results and discussions for the proposed VCO. Finally, conclusions are drawn in section V.

2. SDR RECEIVER CONSIDERATIONS

There are basically two types of receivers: heterodyne and homodyne. The former transposes the RF frequency to an intermediary frequency (IF) for selectivity improvement purposes. The latter translates the RF frequency directly into baseband for further processing the information [5]. Heterodyne receivers were the most used in the last decades but due to their complexity and more difficult integrability, homodyne receivers have gained space in today receiver arquitetures that needs low cost, low power consumption and integrability [3].

2.1 Homodyne Wideband Receivers

A quadrature receiver is a common homodyne receiver implementation, providing inphase and quadrature information of the input signal. This kind of implementation is suitable for modern digital modulations and preserve signal

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integrity for signal modulated in phase or in frequency [5]. However, homodyne receivers have two major problems: DC offset and high sensibility to even order distortion.

A testbench was made for demonstrating those problems in a homodyne quadrature receiver. In Figure 1, the block diagram of this testbench is shown, in which a 16-QAM modulated RF signal and the local oscillator (LO) quadrature signals are injected at the receiver model input. The base-band components of the downconverted signal are considered as the testbench outputs. In order to observe the even order distortion phenomena, the second-order interception point (IIP2) of the mixers was varied. The 16-QAM signal and receiver blocks were developed as Verilog-AMS behavioral models. The testbench was made in ELDO/SPICE and was simulated with Mentor Graphics ADvanceMS and Eldo-RF tools. In Table 1, the parameters used on the testbench for 16-QAM signal, mixers and local oscillator are presented.

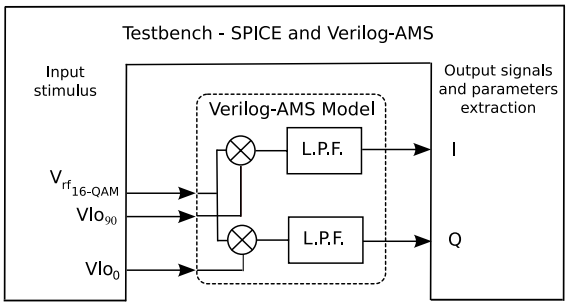

Figure 1: Testbench block diagram for output constellation extraction in a homodyne quadrature receiver.

RF Output Power (dBm)	-20
LO Power (dBm)	0
Frequency (MHz)	1000
Mixers IIP2 (dBm)	-20 a 20
Mixers IIP3 (dBm)	5

Table 1: Parameters used in testbench of Figure 1

The receiver output constellation is shown in Figure 2, from which it can be observed a shift of the constellation center as the mixer IIP2 decreases. That shift can be interpreted as a DC offset due to system second-order non-linearity. See also that 16-QAM output signal constellation is more distorted for lower IIP2. This is due the influence of harmonics and the intermodulation product (IM2) of second-order.

In the next subsection it will be presented an architecture that proposes to mitigate those problems.

2.2 Homodyne Five-Port Receiver

A five-port receiver is a circuit that has three basic blocks: vector basis generator[1], frequency converters and digital signal processing [4]. The vector basis generator should supply

[1]The use of vector basis is not rigorously correct, since the group of vectors contain, in this case, three linearly dependent vectors. However, it is used in this paper for the reader's better understanding

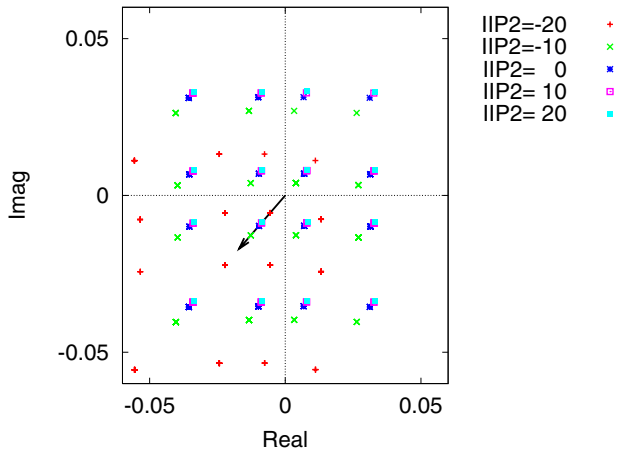

Figure 2: 16-QAM output constellation shift due second-order non-linearities

three signals phase-shifted in 120 degrees. The frequency converters translate the RF signal in three base-band signals proportional to the projections of the input signal over the vector of the basis. After the analog-to-digital conversion, the signals are digitally processed in order to provide I and Q components.

In this work it was used an implementation of the five-port receiver with mixers for frequency conversion and a ring VCO like vector basis generator. This type of VCO generates the vector basis without additional components and can be seen in section 3. The digital processing can be implemented by software in the SDR context. Figure 3 shows this implementation.

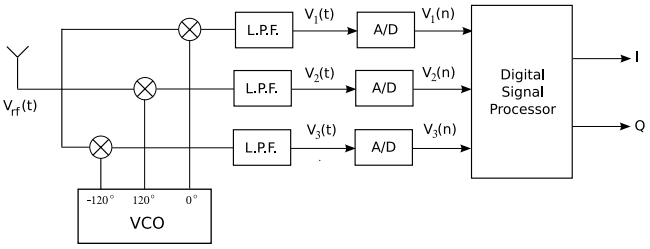

Figure 3: Five-port Receiver architecture

The complex envelope components I and Q are calculated by the weighted sum of the measured voltages at the five-port outputs:

$$I(n) = a_i.V_1(n) + b_i.V_2(n) + c_i.V_3(n) \quad (1)$$

$$Q(n) = a_q.V_1(n) + b_q.V_2(n) + c_q.V_3(n) \quad (2)$$

The weighted constants can be obtained before or during receiver operation by one of the many calibration methods for five-port or six-port correlators available [6, 7].

A testbench similar to that used for quadrature receiver was used for five-port receiver, as can be seen in Figure 4. The parameters used were the same as those of the quadrature receiver, summarized in Table 1.

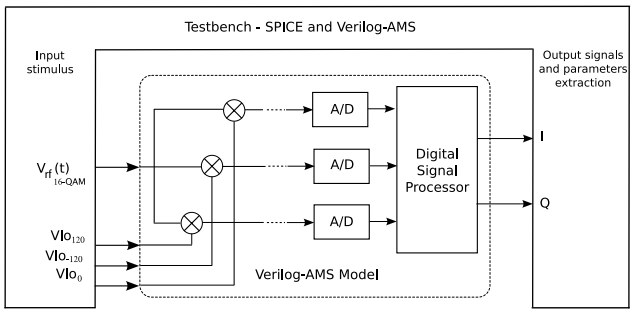

Figure 4: Testbench for output constellation extraction in a five-port receiver.

The output constellation signal is presented in Figure 5. Differently of quadrature architecture, the output constellation does not shift, remaing centered at the origin.

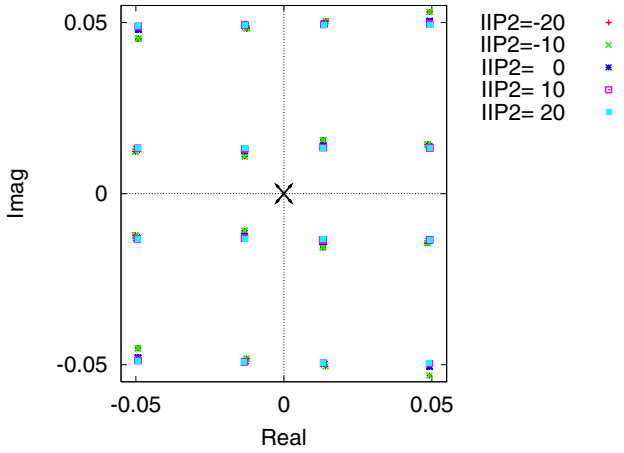

Figure 5: 16-QAM Output Constellation with second-order non-linearity effects reduction in a five-port receiver.

In addition, the five-port receiver has a better immunity for adjacent channels interferer signals [7] that may contribute to receiver distortion.

3. WIDEBAND VCO FOR FIVE-PORT RECEIVER

In previous section, a five-port based receiver was proposed for SDR implementation. That receiver needs a vector basis generator to provide a 120 degree phase-shifted outputs. In this work we propose an wideband ring VCO to implement the like basis generator. This VCO generates three outputs phase-shifted in 120 degrees without additional circuitry.

In order to generate 120-degree phase-shifted outputs, a three-stage ring VCO is needed, since the phase contribution of each delay cell is $360/N$, being N the number delay cells. Since today mixers have differential inputs configuration (e.g. gilbert cell based mixers), a ring VCO differential topology is needed. Is known that differential topology presents worse phase noise than single-ended topology [8], but it is possible to improve the phase noise performance of differential ring VCOs by using a saturated-type delay-cell [9]. The mechanism for frequency tuning is made by transmission gate that has a wide and linear tuning capability [10]. In this work it was used a differential saturated-type delay-cell with transmission gates as frequency tuning mechanism. Figure 6 shows this circuit.

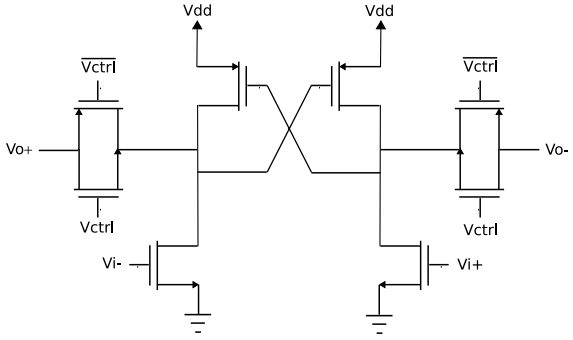

Figure 6: Delay-cell

The delay-cell is an input NMOS differential pair, a PMOS positive feedback pair and a transmission gate which connects the output of one delay-cell to the next one.

The delay-cell can be partitioned in two main blocks: the main delay-cell and the tuning mechanism. The main delay-cell is made by a differential latch and the tuning mechanism by transmission gate. The ring VCO is showed in figure 7 and is implemented by three delay-cells in order to provide three outputs phase-shifted in 120 degrees.

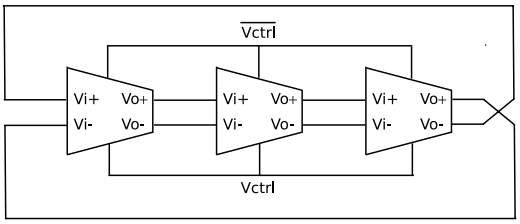

Figure 7: Three-stage differential ring VCO

In the next subsections will be made analysis of the two delay-cell components: the differential latch and the transmission gate.

3.1 Differential Latch

The differential latch is implemented by a Differential Cascade Voltage Switch Logic (DCVSL) Circuit, that is always composed by differential inputs and differential outputs with cascaded feedback PMOS transistors which forces the circuit operation in *full switching* mode. This type of logic circuit uses complementary inputs to get complementary outputs using a pair of NMOS pull-down network [11]. Aiming to get better phase-noise since its directly correlated with the number of active components [8], we used the simplest way of NMOS pull-down network, a simple pair of NMOS transistors making the circuit a differential latch.

The Figure 8 presents the main delay-cell composed by a differential latch used for implementing the DCVSL. When

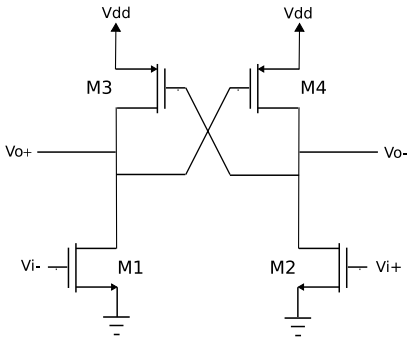

Figure 8: Main delay-cell made by a differential latch

$Vi+ =' 1'$, $Vi- =' 0'$, M2 is ON and M1 is OFF. Then M3 change from cuttoff region to saturation and $Vo+$ switchs to HIGH logic level while $Vo-$ is in LOW logic level. When $Vi+ =' 0'$, $Vi- =' 1'$, M1 is ON and M2 is OFF. Then M4 changes from cutoff region to saturation, and $Vo-$ switchs to HIGH logic level while $Vo+$ is in LOW logic level. The operation of this circuit describes a *full switching* operation that enables a better phase-noise in differential delay-cell.

3.2 Transmission Gate

The transmission gate is the better choice for oscillators that needs tuning in an wide frequency range [10]. The transmission gate resistance varies in function of applied voltage at transistor gate. This resistance variation is the mechanism for frequency tuning in the VCO. The relationship between resistance and voltage is non-linear and due to transistors alternate between triode and saturation regions periodically, it is not straightforward to determine its equivalent resistance. The Figure 9 shows the transmission gate with a rising unit step signal at input and a time-delayed signal at output, which is connected to a capacitor large enough compared to parasitic capacitance. Assuming this process with a first-order time constant model and measuring the delay time t_d, the effective resistance of transmission gate is obtained as 3.

$$R_{eff} = \frac{t_d}{C_L.ln(2)} \quad (3)$$

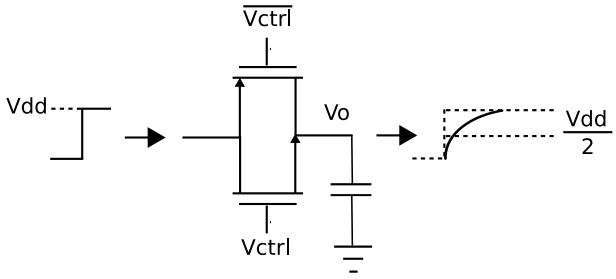

Figure 9: Model for effective resistance calculation of the transmission gate

In 3 is seen that, with a fixed value capacitor C_L is possible to obtain R_{eff} value by simulation, calculating the delay time t_d.

4. RESULTS AND DISCUSSIONS

In order to analyze the VCO behavior were performed RF and monte-carlo simulations using Mentor Graphics Eldo-RF circuit simulator.

The methodology used was to elaborate testbenches to measure the VCO frequency tuning range, the VCO phase-noise and the outputs phase-shift variations by monte-carlo analysis. The testbenches were implemented in Eldo-RF.

4.1 VCO frequency tuning range

This test shows the VCO frequency tuning range and its correlated control voltage. The testbench varies the input control voltage and extract the VCO frequency. The testbench results can be seen in Figure 10.

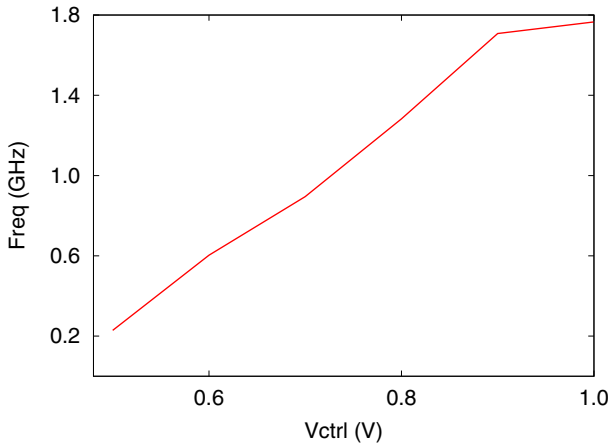

Figure 10: Frequency x control voltage

The VCO frequency tuning range is from 200 MHz to 1.8 GHz. The range is wide 1600 MHz and can be suitable for Cognitive Radio, Software Defined Radio applications and other wideband applications that needs wide frequency tuning range. The control voltage vary from 0.5 to 1.0 V. For voltages between 1.0 and 1.2 there is a saturation due to 1.2V supply voltage and this control voltages may tune the same frequency then the control voltage range for the VCO is limited from 0.5 to 1.0 V.

To achieve this frequency tuning range were use minimum 130nm technology sizes for transistor length and width, which are L=0.12μm and W=0.16μm.

4.2 VCO phase-noise

This test shows the VCO phase-noise. The testbench was implemented using BSIM4 noise models provided by IBM Process Design Kit for 130 nanometer CMOS technology and was simulated by Eldo-RF using specific functions for extract phase-noise in function of frequency offsets.

The VCO phase-noise is -107 dBc/Hz at 1 Mhz offset frequency. Future works may include a more detailed noise analysis but in this work was not the focus because in the first moment the interest is to validate the VCO for five-port receiver that needs large tuning range, wideband and a good phase variations model as more important figures of merit at present moment research.

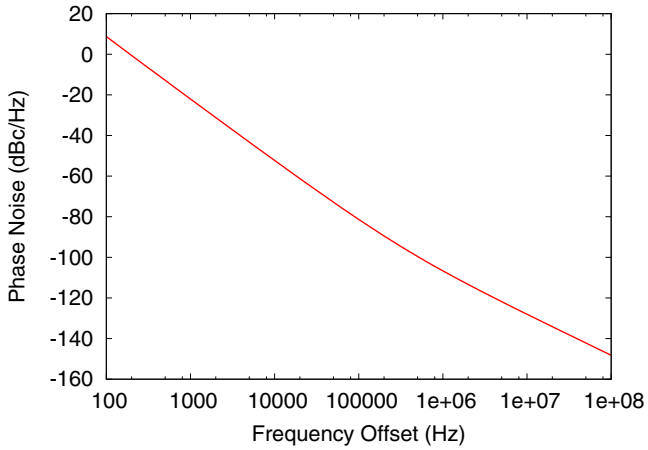

Figure 11: VCO phase-noise

4.3 Outputs Phase-shift monte-carlo analysis

VCO outputs phase-shift variations is important in five-port works because are used as variables by calibration methods [6] that configures the five-port receiver for correct RF detection without DC offsets, even order distortion or adjacent channel interferences.

In order to verify VCO outputs phase-shift variations were made monte-carlo analysis. Those analysis were made as function of parametric variations until 25% in W and L transistor dimensions and also in terms of threshold voltage mismatch. Those statistics simulations were made with Eldo-RF and used 2000 samples in monte-carlo analysis.

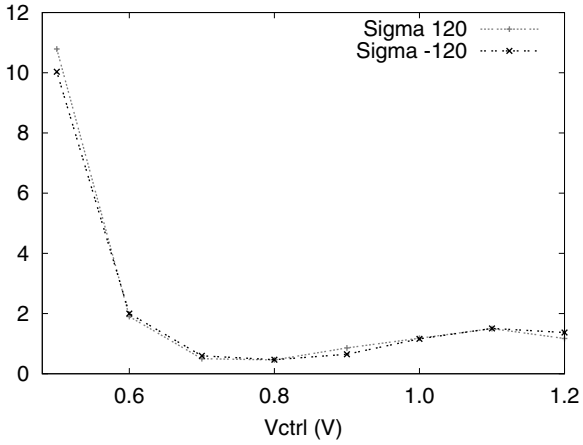

Figure 12: Standard Deviation in function of control voltage

Figure 12 shows a summary of these variations, with standard deviation provided by monte-carlo analysis in function of VCO control voltage. See that standard deviation (in degrees) increases when control voltage is reaching transistor threshold voltage, which means that process variations contribute more significantly in moderate and weak inversion transistor regions for outputs phase-shift variations.

These results enables to develop a model to predict five-port receiver operation in function of phase variations. Furthermore, the development of a VCO behavioral model providing phase distribution of the outputs allow a reduction in time spent with simulations of five-port receivers, because there is no need to simulate the VCO subcircuit together in SPICE maintaining a good fidelity in the results.

5. CONCLUSIONS

A five-port receiver can be an alternative to implement receivers for RF systems that needs wideband and wide frequency tuning range like cognitive radio and SDR applications. This type of receiver needs an wideband VCO with 120 degree phase-shifted outputs. A ring VCO with differential saturated-type delay-cell and tuned by transmission gate was implemented in IBM CMOS 130nm technology and simulations showed that has the requirements for become the five-port receiver an attractive choice for that RF systems. Testbenches were made to demonstrate the improvement of five-port architecture in homodyne receivers. Also were made testbenches for VCO characteristics extraction as frequency tuning range, phase-noise and phase-shift variations. Monte-carlo analysis were realized aiming to provide VCO outputs phase-shift in function of process variations. Those analysis will be used to develop a behavioral model of the VCO with focus on five-port receiver simulations allowing time-saving.

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