ULTRA-LOW-POWER CMOS LOGIC

UNIVERSIDADE FEDERAL DE SANTA CATARINA
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OUTLINE:

- Introduction
- CMOS Logic Gates Operating in Weak Inversion
- Substrate Bias Compensation Technique
- Conclusion

Introduction

- Continuous increase in use of portable electronics
- Battery operated → low power consumption → CMOS

- Total Power = Dynamic Power + Static Power

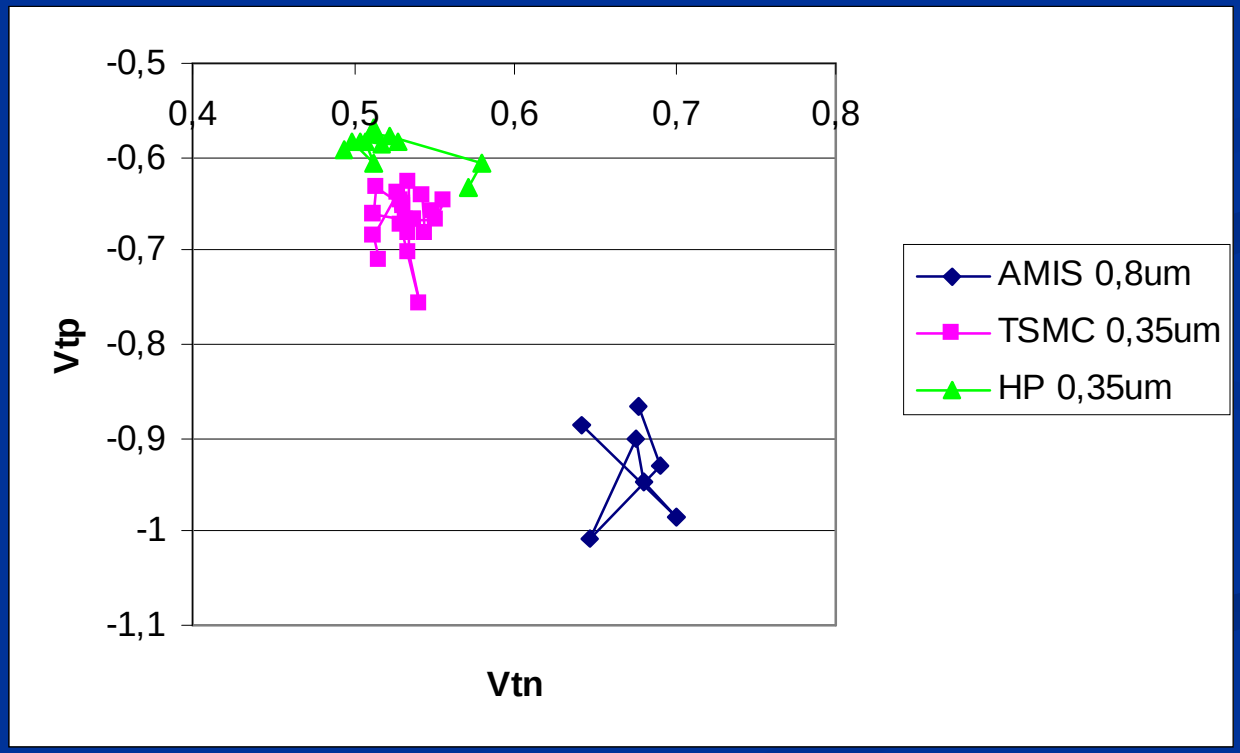
$$P_{DYN} \alpha V_{DD}^2 \qquad P_{ST} \alpha V_{DD}$$

- Low Consumption → Low Supply Voltage + Low Operating Frequency

→ Subthreshold or Weak inversion (W.I.) operation

Technological Parameter Variations

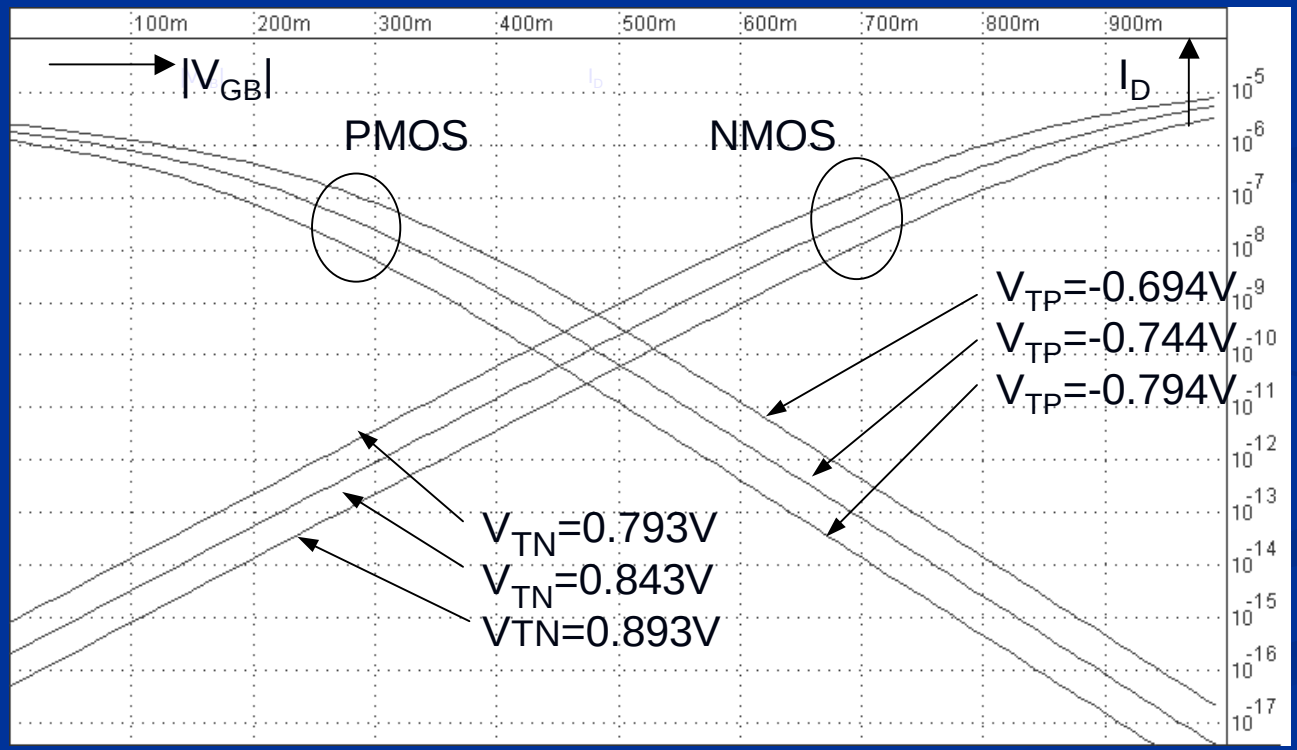
- *intrachip* parameter variation and *interchip* parameter variation → ±100mV Threshold Voltage
  ±30% Current Factor



Consequences of Technological Parameter Variations

- Weak inversion → exponential current law

$$I_{DN(P)} = I_{ON(P)} \cdot \exp\left((-)\frac{V_{GB} - V_{TN(P)} - n_{N(P)} \cdot V_{SB}}{n_{N(P)} \cdot \phi_T}\right)\left[1 - \exp\left(-(+)\frac{V_{DS}}{\phi_T}\right)\right]$$

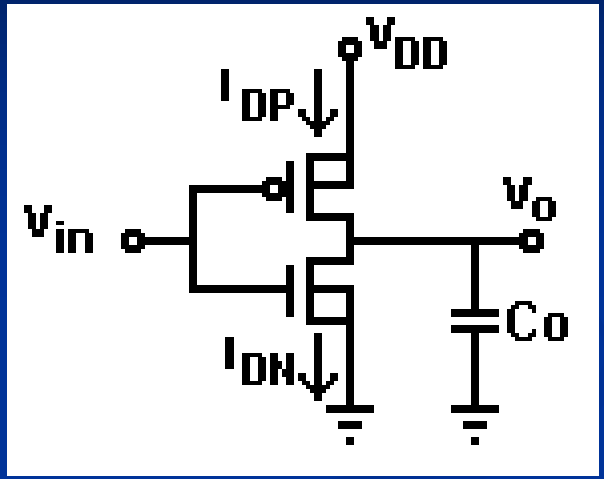


AMS0.8um

BSIM3v3

(W/L)=2um/0.8um

CMOS logic gates operating in weak inversion

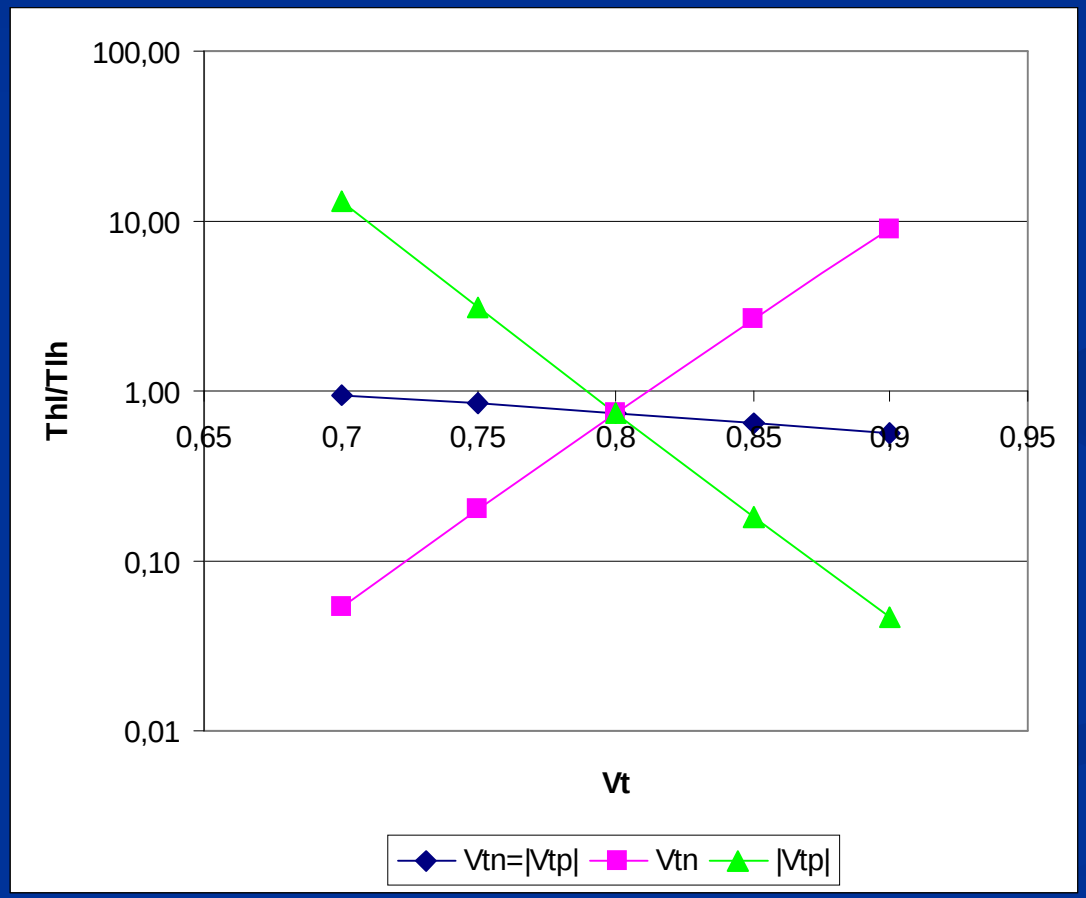


- **Rise Time (T_{LH}) and Fall Time (T_{HL}) – 10%-90%**

$$I_{DN(P)} = -(+)C_O \cdot \frac{dV_O}{dt}$$

$$t_{HL(LH)} = \frac{0.8\, C_O\, V_{DD}}{I_{ON(P)}\, e^{\frac{V_{DD} - |V_{TN(P)}|}{n_{N(P)} \cdot \phi_T}}}$$

Consequences of Technological Parameter Variations



INVERTER

0.8µm BET Technology

$V_{TN} = |V_{TP}| = 0.8V$

$(W/L)_N = 15µ/9µm$

$(W/L)_P = 45µm/9µm$

$C_O = 1.3pF$

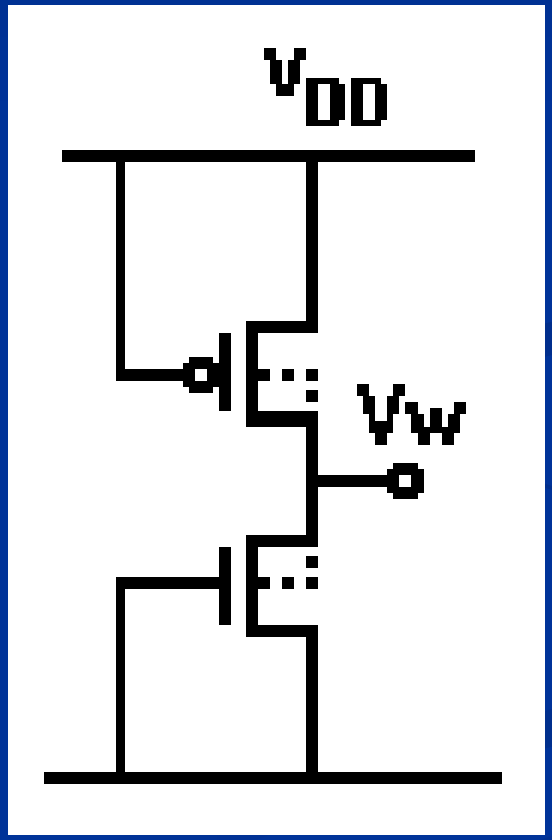
$I_{ON} \approx I_{OP}$

$T_{HL}/T_{LH}|_{max} = 400$!!!

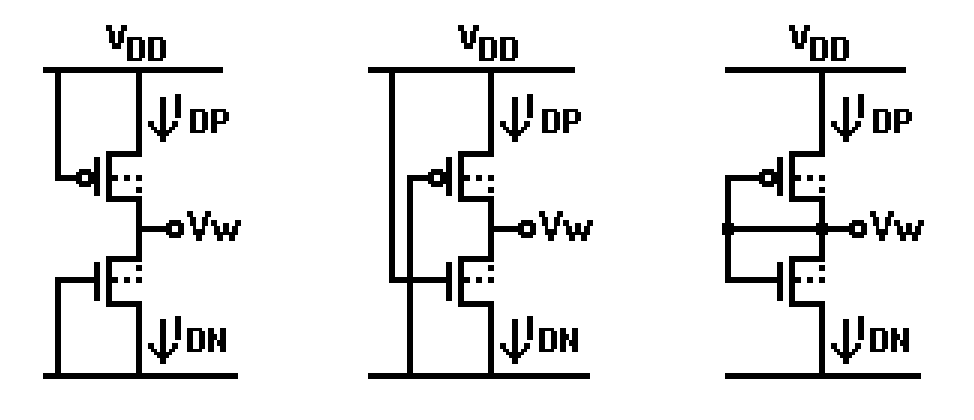
ULTRA-LOW-POWER CMOS LOGIC

Bryant, 2001

- **Substrate Bias Circuit: NMOS and PMOS are “cut off”!?.**



Proposed Compensation Technique

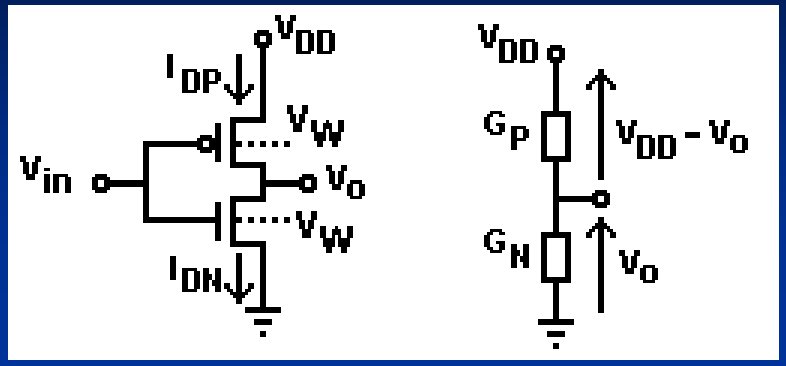


Bryant **Crossed** **In between**

$$I_{DP} = I_{DN}$$

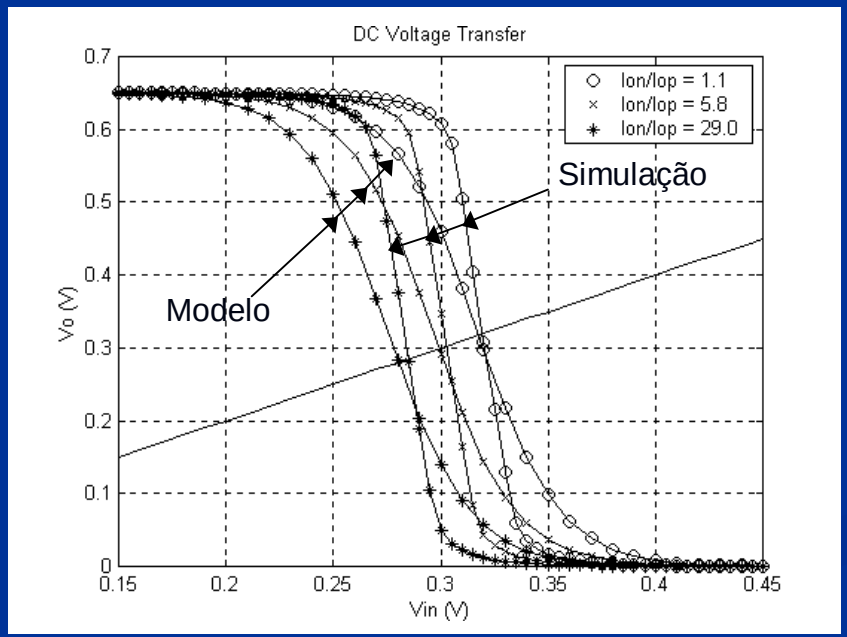
$$V_W = \frac{V_{DD}}{2} + \frac{V_{TN}}{2 \cdot n_N} - \frac{|V_{TP}|}{2 \cdot n_{PT}} + \frac{\phi_T}{2} \ln\left(\frac{I_{OP}}{I_{ON}}\right)$$

DC Transfer characteristic for the Inverter



$$V_O = \frac{V_{DD}}{1 + e^{\frac{V_{IN} - V_{TH}}{\phi_T} \cdot \left(\frac{1}{n_N} + \frac{1}{n_P} \right)}}$$

$$V_{TH} = V_W = \frac{V_{DD}}{2} + \frac{V_{TN}}{2 \cdot n_N} - \frac{|V_{TP}|}{2 \cdot n_{PT}} + \frac{\phi_T}{2} \ln\left(\frac{I_{OP}}{I_{ON}} \right)$$



0.8µm AMS Technology

ACM MOSFET Model

V_{DD} = 650mV

$(W/L)_N = (W/L)_P$ = 2µm/0.8µm

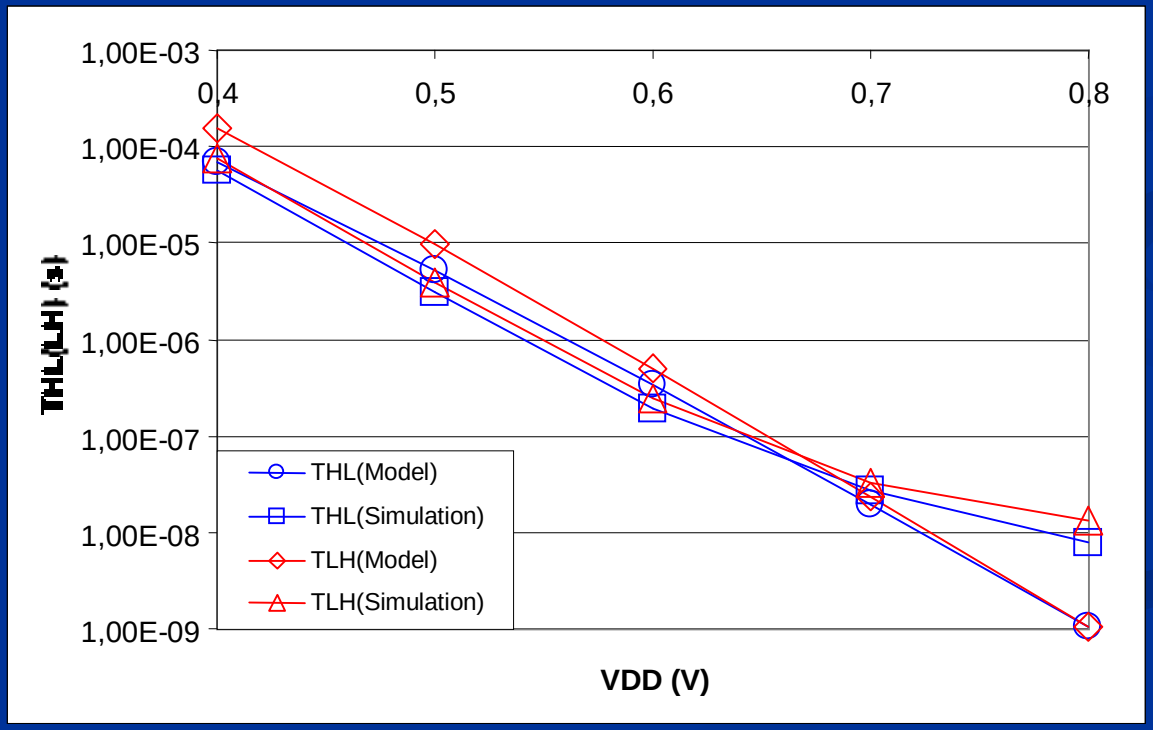
Inverter Transient

$$T_{HL(LH)} = \frac{0.8\, C_O\, V_{DD}}{I_{DRIVE,N(P)}}$$

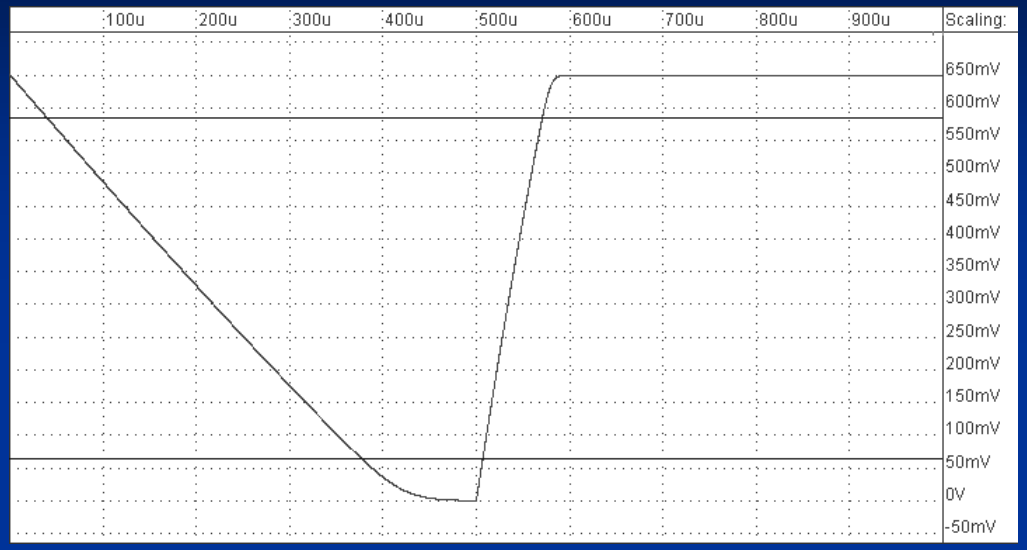
$$I_{DRIVE,N} = I_{ON} \cdot e^{\frac{V_{DD} - V_{TN} + V_W \cdot (n_N - 1)}{n_N \cdot \phi_T}}$$

$$I_{DRIVE,P} = I_{OP} \cdot e^{\frac{n_P \cdot V_{DD} - |V_{TP}| - V_W \cdot (n_P - 1)}{n_P \cdot \phi_T}}$$

0.8µm AMS



Inverter Transient (II)



0.8µm AMS
ACM model
$(W/L)_N$ = 2µm/0.8µm
$(W/L)_P$ = 2µm/0.8µm

Without compensation
X axis : 1000µs
f_{MAX} = 2.5kHz

With compensation
X axis : 40µs
f_{MAX} = 88kHz

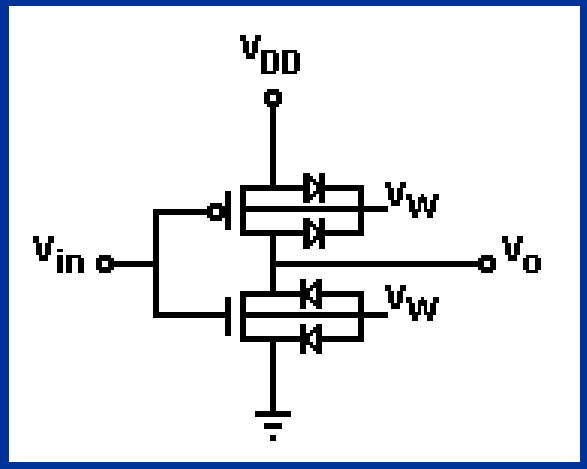
Power consumption

Dynamic Power

$$P_{DIN} = C_O \cdot V_{DD}^2 \cdot f$$

Static power → Diodes are forward biased

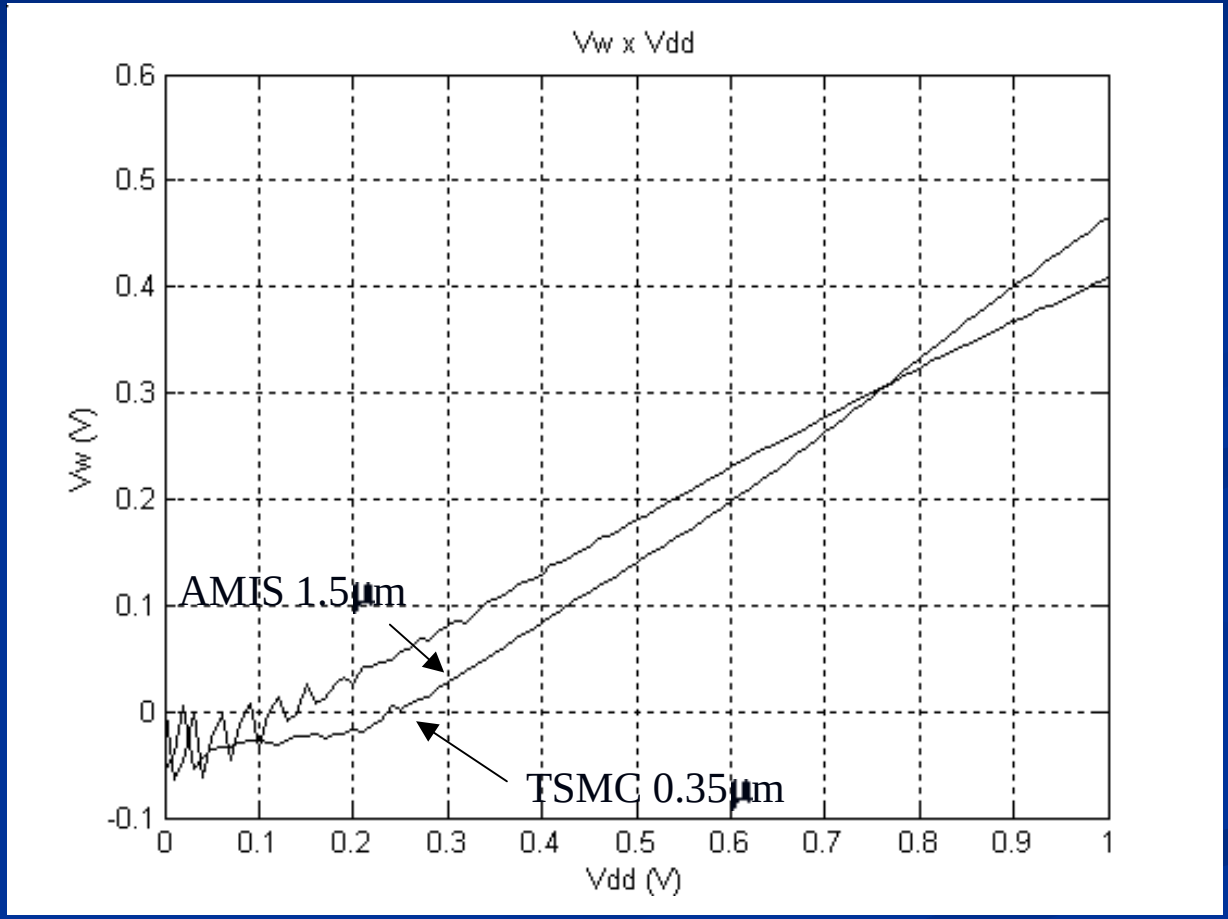
PTRANSISTORS << PDIODOS



$$P_{static} = \frac{3 \cdot V_{DD}}{2} \cdot e^{\frac{V_{DD}}{2 \cdot \phi_T}} \cdot \left(I_{SN} + I_{SP} \right)$$

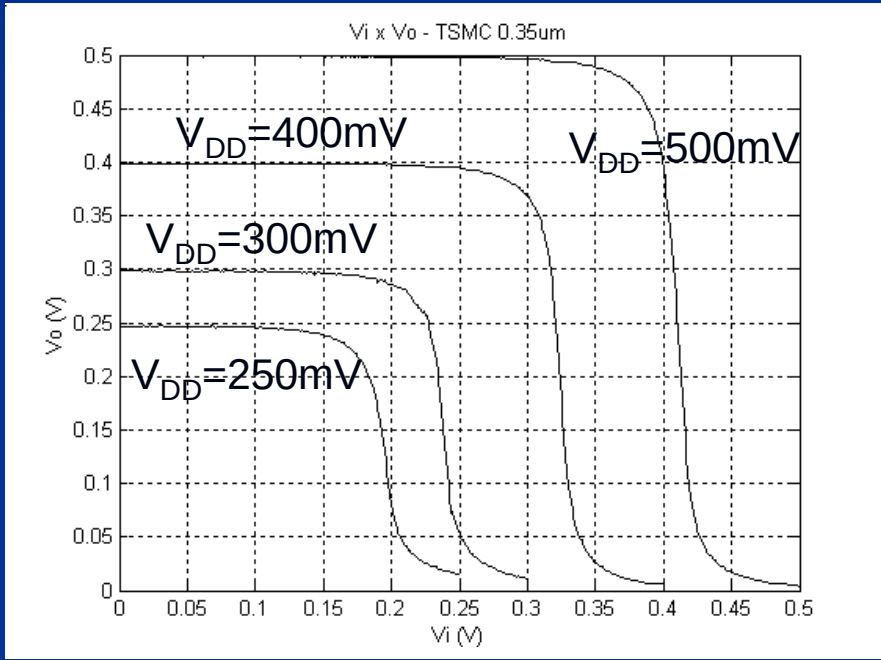
Experimental results

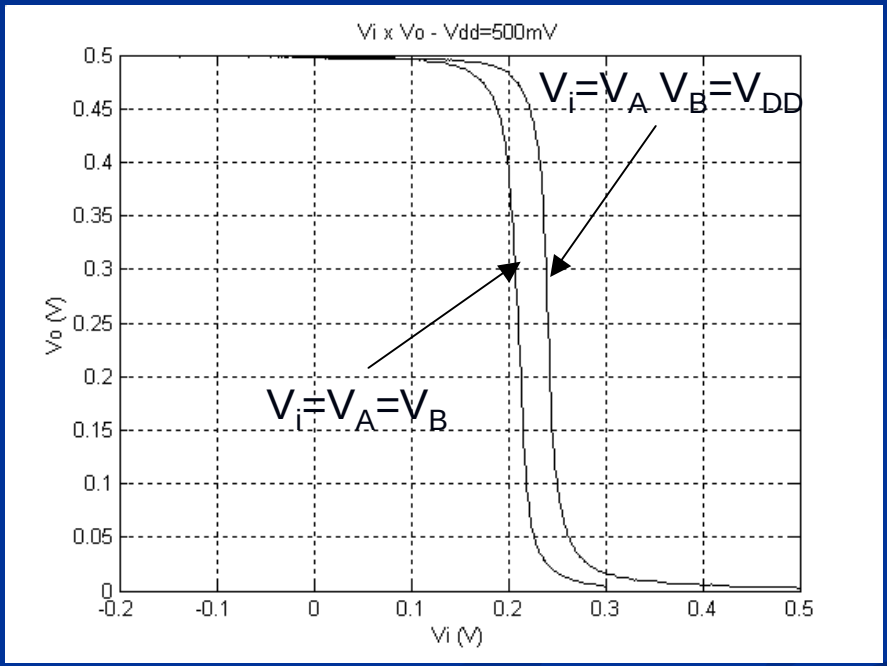
V_W BIAS



Experimental Results – INVERTER and NAND-2

0.35µm TSMC





INVERTER **NAND-2**

Conclusion

- The operation of CMOS logic circuits in conventional CMOS technology for supply voltage as low as 250mV was shown.

Application : ULTRA-LOW POWER-CMOS