A Switched-MOSFET Programmable Low-Voltage Filter

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Abstract

This paper describes a digitally programmable low-voltage low-power analogue filter that can be used in hearing-aid circuits [1-4]. The filter employs the recently introduced switched-MOSFET technique [5,11-15], a sampled-data technique suitable for low supply voltage operation since it avoids the conduction gap of the switches and does not need any dedicated process. The filter was implemented using the DIMES 1.6μm CMOS process and achieves 64 dB dynamic range under 2.2V supply. The total current consumption is 93μA.

1. Introduction

Sampled-data circuits have been extensively employed in VLSI chips. The switched-capacitor (SC) technique has prevailed, but in the last few years a lot of research has been done on switched-currents (SI). For low supply voltage operation, however, both techniques have as the main problem the so-called "conduction gap" of the switches [6,16]. There are some special techniques to deal with this problem, such as the use of dedicated processes, on-chip generation of a voltage higher than the power supply, bootstrap circuits and the switched op-amp [6, 17]. Of course, these techniques add some extra cost to the chip, and some other problems like lesser reliability and an increase in power consumption.

The recently introduced switched-MOSFET (SM) technique [5,11-15] overcomes the problem of the conduction gap of the switches. The SM technique uses current processing, allows easy programmability through MOSFET-only current dividers (MOCDs) [7] and does not need any dedicated process.

In this paper we present the design and implementation of a programmable switched-MOSFET low-voltage low-power filter that can be used in hearing-aid circuits. The filter contains a v-to-i converter, a delay cell, a biquadratic section (using auto-zero offset compensation and MOCDs for programming) and an i-to-v converter, forming a programmable band-pass filter where both the input and the output signals are voltages.

This paper is organised as follows. In section 2, the basic principle of the SM technique is explained. Section 3 focuses on the SM v-to-i and i-to-v converters. Section 4 presents the biquadratic section that is the core of the band-pass filter. In section 5, the complete integrated circuit is described.

2. The switched-MOSFET technique

The basic delay cell of the switched-MOSFET technique is presented in Figure 1 [12]. This cell, a switched current mirror, operates as follows. When the switch is closed, assuming the operational amplifier (op-amp) to be ideal, we have, neglecting transistor mismatch,

$$i_o = -\left[(W/L)_{M3}/(W/L)_{M2}\right] i_{in} \qquad (1)$$

since *M2* and *M3* are both biased with the same set of voltages. The output current i_o is an inverted replica of the input current i_{in}. The capacitor C_h is charged to a voltage V whose value depends on i_{in}, on the parameters of transistor *M2* and on the gate voltage. When the switch opens, the voltage V is held on the memory capacitor (C_h) and the current is sustained at the output. The n-MOS switch (S) operates at a constant voltage equal to V_X, which is generated by the series association of two identical transistors as shown in Figure 2 [12,16].

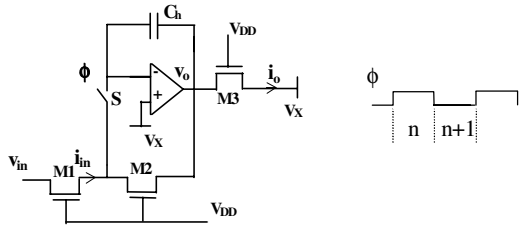

Figure 1. The delay cell of the switched-MOSFET methodology [12].

The network in Figure 2, apart from its nonlinearity, is similar to a resistive voltage divider with two identical resistors, one connected to V_{DD} and the other to ground, the output V_X taken at the common node. The connection of a transistor between V_X and V_{DD} or between V_X and

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ground would result in the same current with opposite directions. Thus, the voltage V_X provided by the circuit in Figure 2 allows for the highest current swing. It also guarantees that the n-switch operates outside of the conduction gap.

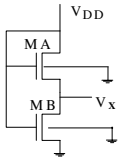

Figure 2. Bias circuit for the delay cell and integrators. MA and MB are identical transistors.

3. Voltage-to-current converter

Switched-MOSFET circuits process current signals. Therefore, if the input and output signals are voltage rather than current, v-to-i and i-to-v converters are required. Figure 3 shows conceptually the SM v-to-i converter, which is similar to the proposal in [9]. Because the voltage V_X at the intermediate node of the series association in Figure 2 is closer to V_{SS} than to V_{DD}, a current source is necessary to allow for large voltage swing operation.

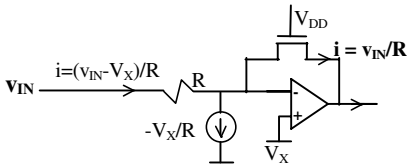

Figure 3. V-to-i converter.

The current source $-V_X/R$ in Figure 3 must be independent of technology. A circuit that generates this current is shown in Figure 4. The current $-V_X/R$ flows through R and M_{X1}. With $M_{X1} \equiv M_{X2}$, the current through M_{X2} is also $-V_X/R$, because the two transistors3 are under the same set of potentials. The i-to-v converter is analogous to the v-to-i converter (see Figure 5).

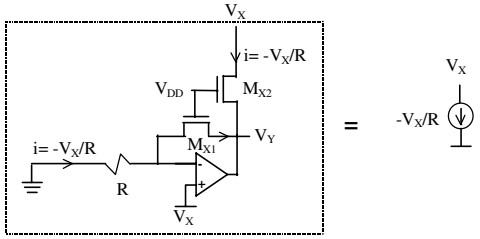

Figure 4. Current source $-V_x/R$ for the v-to-i converter.

4. The complete circuit

As stated in Section 1, the chip is composed of a v-to-i converter, a bandpass programmable filter (using 6-bit MOCDs) and an i-to-v converter. The simplified schematic for the chip is shown in Figure 5. The filter core is a biquadratic section (biquad) [13]. The biquad utilises two second order SM integrators and was designed using backward LDI transformation [10]. This transformation leads to smaller frequency prewarping errors than the Euler transformations. The output/input relation for the biquad is:

$$\frac{I_o^{\phi e}(z)}{I^{\phi e}(z)} = -\frac{K_2 \text{a.f.}\left(1-z^{-1}\right)z^{-1}}{1-\left(2-\text{a.f}-\text{a}^2\right)z^{-1}+\left(1-\text{af}\right)z^{-2}} \qquad (2)$$

In the biquad in Figure 5, the programmability can be achieved using MOCDs. The centre frequency (ω_o) and quality factor (Q) can be controlled independently if the sampling frequency is much higher than the centre frequency. In this case:

$$\omega_o T \cong \text{a} \qquad (2a)$$

where T is the sampling period, and

$$Q \cong 1/\text{f} \qquad (2b)$$

Even though we could control the central frequency, the quality factor and the gain, in the implemented prototype only the central frequency is controlled with the use of 6-bit MOCDs to control the parameter "a".

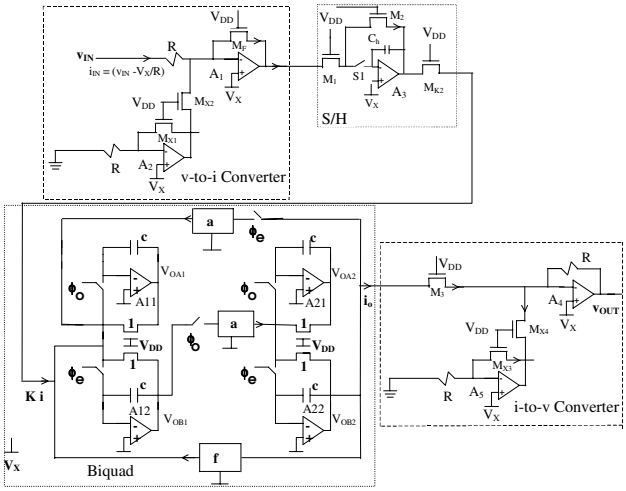

Figure 5. Simplified schematic for the SM filter.

Auto-zero (AZ) compensation was used for the operational amplifiers in the biquad (A_{11}, A_{12}, A_{21} and A_{22},

Figure 5). Figure 5 does not show the V_X generation circuit, which was implemented with 10µm/40µm transistors in a circuit like the one in Figure 2. The blocks "a" and "f" represent MOCDs, and a buffer (not shown) is used to deliver V_X to the MOCDs without charging the V_X generation circuit.

All operational amplifiers of the SM technique operate at constant common mode voltage, V_X, which is close to V_{SS}. Therefore, the design of the input stage of the op-amp is considerably simplified and even a simple Miller-compensated op-amp can operate at 2.2V supply. However, we decided to choose the PMOS input stage op-amp in Figure 6 [9] for two reasons: i) its gain and bandwidth are larger than those of the Miller-compensated op-amp; and ii) it is able to operate at supply voltages as low as 1V [9]. The op-amp in Figure 6 was designed using the equations of the current-based ACM model [8], which are written in terms of the transistor current density. Table 1 presents specifications for the SM filter design.

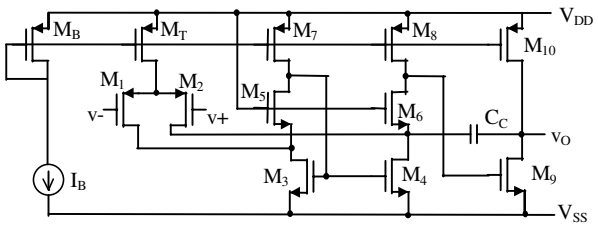

Figure 6. Low-voltage class A opamp [9].

Table 1. Specifications for filter design.

Supply Voltage	2.2V
Maximum input voltage swing	± 200mV
Resistor for v-to-i conversion (working current per unit load)	200kΩ 1µA
SM transistors Switches	10µm/20µm 2.4µm/1.6µm
Hold capacitors, C_h	5pF
Op-amp compensating capacitor	C_C= 1.2pF
Sampling frequency, f_S	50kHz
Op-amp GBW	≥ 500kHz

The choice of some of the parameters in Table 1 was based on factors such as settling time, charge injection and noise [14].

The microphotograph of the chip is shown in Figure 7. The chip area is approximately 3600µm x 1950µm with pads. The floorplan for the chip is shown in Figure 8. Note the small area occupied by the two 6 bits MOCDs, responsible for the filter centre frequency programming. The pads for the digital inputs include protection diodes.

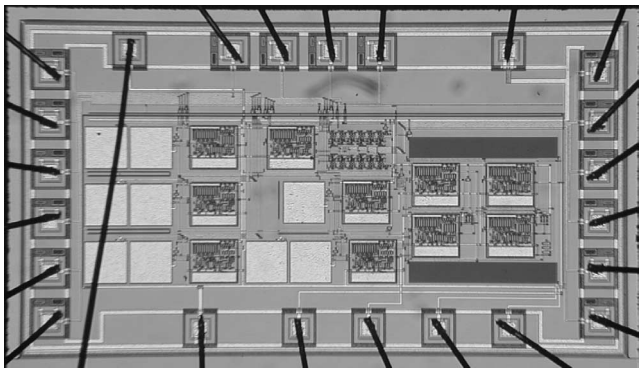

Figure 7. Chip microphotograph.

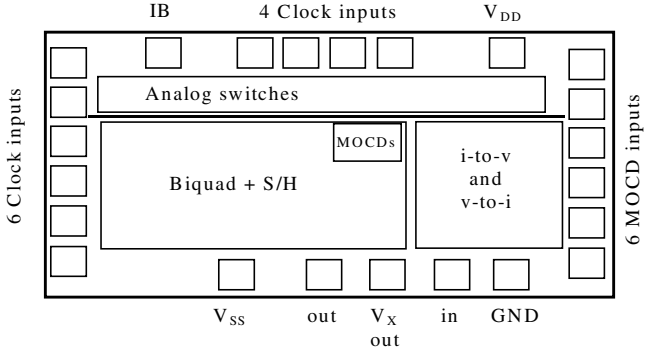

Figure 8. Floorplan for the SM filter.

5. Experimental results

Several measurements were performed on the filter. The AC response for several digital words in the MOCDs is shown in Figure 9. Table 2 summarises the obtained results. As can be seen in Table 2, some imperfections were detected through the measurements. These are the centre frequency deviation, the Q error and the gain error. However, none of this errors is unacceptable as the filter is programmable. In applications such as hearing aids in general the audiologist (or the system itself) must program the filter response to each patient.

Figure 10 shows the noise measurement for the chip. Using a $200mV_{peak}$ input signal the achieved dynamic range is 63.8dB. This is very close to the calculated dynamic range, 66.8dB.

The maximum measured output swing without clipping was ± $450mV_{peak}$. Figure 11 illustrates the measured distortion results as a function of the input voltage for the centre frequency (f_o), the –3dB inferior frequency (f_i) and the –3dB superior frequency (f_s). Table 3 summarises the obtained results. The results are considered adequate for the specified input voltage range (up to the input voltage of $200mV_{peak}$).

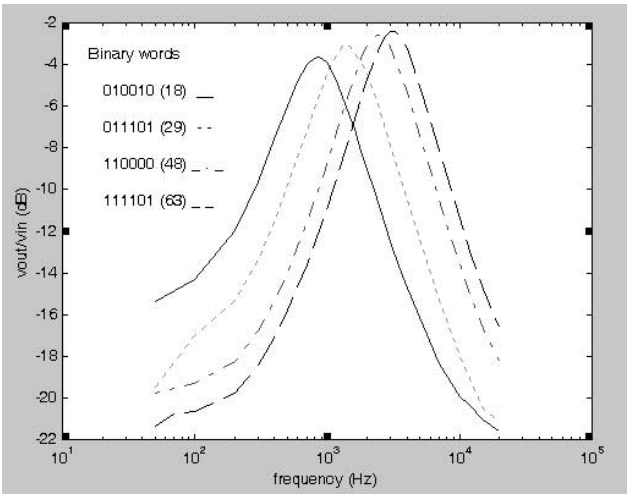

Figure 9. Measured AC response for several MOCD words.

Table 2. AC response details.

Digital word, DW	Calc. centre freq. f_o (Hz)	Meas. centre freq. f_o (Hz)	f_o error (%)	Calc. Q	Meas. Q	Q error %	Gain error (dB)
$010010_2 = 18_{10}$	1130	860	23.9	0.92	0.81	- 13	-3.6
$011101_2 = 29_{10}$	1810	1400	22.6	0.88	0.92	+ 4	-3.1
$110000_2 = 48_{10}$	3000	2420	19.3	0.81	0.90	+ 10	-2.6
$111101_2 = 61_{10}$	3834	3200	16.5	0.76	0.88	+ 13	-2.4

All the above measurements were performed under a supply voltage of 2.2V, and the total current consumption is 93µA. It is important to emphasise that this current consumption can be reduced significantly with the use of class AB operational amplifiers. This is because in the SM technique the op-amps drive resistive loads.

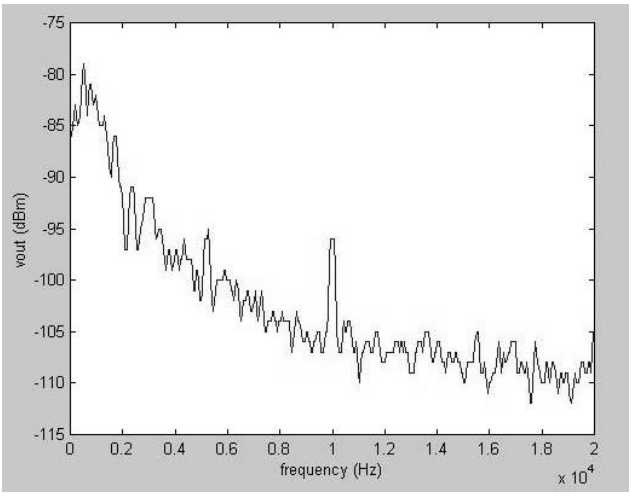

Figure 10. Measured noise.

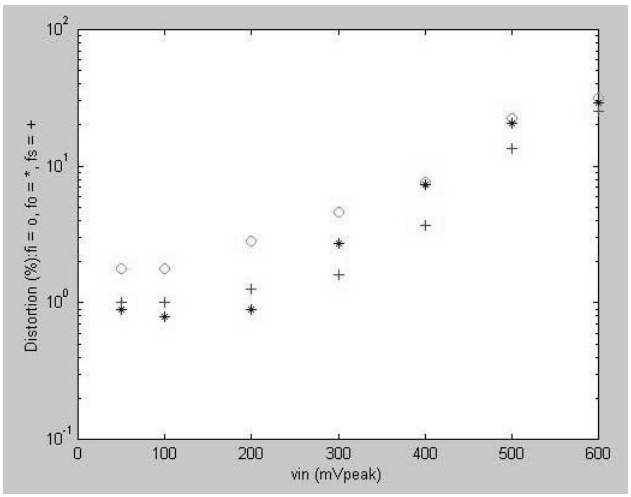

Figure 11. Measured distortion.

Table 3. Distortion results.

vin (mV_{peak})	50	100	200	300	400	500	600
distortion f_i (%)	1.8	1.8	2.8	4.6	7.6	22.3	31.5
distortion f_o (%)	0.9	0.8	0.9	2.7	7.3	22.7	29.1
distortion f_s (%)	1	1	1.26	1.6	3.7	13.4	25.2

The chip is still functional down to a supply voltage of 1.7V. However, the distortion levels in this voltage are considerably higher than the ones obtained under 2.2V supply. It is important to notice that the process used, DIMOS 01, an 1.6 micron CMOS process adopted from Philips, presents threshold voltages higher than 1V. The supply voltage of 2.2 is less than two stacked gate-source voltages and two saturation voltages and thus the SM filter can be considered to be a low-voltage circuit [18].

6. Conclusions

A digitally programmable low-voltage low-power filter suitable for hearing instruments was described. The circuit contains a v-to-i converter, a delay cell, a biquadratic section and an i-to-v converter and was implemented in a 1.6 micron CMOS process. The programmability is achieved by means of MOCDs and does not require a large silicon area. The results show applicability of the switched-MOSFET technique as an alternative technique for low-voltage discrete-time signal processing without the need for a special process.

Acknowledgements

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