AN ULTRA-LOW-POWER SELF-BIASED CURRENT REFERENCE

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1. Introduction

References:

- Voltage: \( V_{\text{ref}} \rightarrow \phi_t, V_{G0} \)
- Current: \( I_{\text{ref}} \rightarrow V_{\text{ref}} / R, \mu C'_{ox} \phi_t^2 \)

Required for:

- A/D and D/A conversion
- Biasing (analog and digital circuits)
1. Introduction

Objective:

➢ Design a CMOS current reference for low-voltage & ultra-low-power applications

Characteristics of the current reference:

1. Autonomous;
2. Low consumption;
3. Simple to design.
2. Basic concepts

ACM model

\[ I_D = I_F - I_R = I_S (i_f - i_r) \]

\[ I_S = \mu C_n \frac{\phi_t \phi_n}{2} \frac{W}{L} \]

\[ \frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_f(r)} - 2 + \ln(\sqrt{1 + i_f(r)} - 1) \]

\[ V_P \approx \frac{V_{GB} - V_{T0}}{n} \]

\( V_{SB} = 0 \) & saturation
3. Self-biased current references

[Vittoz, 1977]

- $I_{\text{ref}} = (\phi_t / R) \ln K$
- $I_{\text{ref}} = 0.6nA (6nA)$
- $\phi_t \ln K = 60mV \rightarrow R = 100(10)M\Omega$
- Efficiency = 33%

[Oguey, 1996]

- S.I. $(M_{a,b})$ not appropriate for LV
- $NK_2 > 1$ (M.I) and $NK_2 > 4$ (S.I)
- $I_{\text{ref}} \propto \mu C_{ox} n\phi_t^2$
- Efficiency = 14% for $N=4$
4. Proposed self-biased current reference

SCM (Self-Cascode MOSFET)

- W.I → $V_X = \phi_i \ln \alpha$ - PTAT
- M.I, S.I → $V_X = f(i_f, \alpha)$

$\alpha = \left[ 1 + \frac{S_2}{S_1} \left( 1 + \frac{1}{N} \right) \right]$  

There is an OP stable for $\alpha$(W.I) > $\alpha$(M.I) > 1
4. Proposed self-biased current reference

- SCM (M.I.)
- Voltage following current mirror
- PTAT
- Voltage

\[ \alpha(M.I. > 1) \]

\[ \alpha(W.I. >> 1) \]

\[ V_{DD\min} \]

\[ V_{DSSATP} \]

\[ V_{GSN} \]

\[ V_{GSP} \]

\[ V_{DSSATN} \]

\[ V_{x(M.I.)} \]
4. Proposed self-biased current reference

**Design**

- $I_{ref} = 400\text{pA}$, $V_{DD_{min}} = 1.2\text{V}$ (Possible?)
- $V_X < 100\text{mV}$, e.g., $\alpha(\text{w.i}) = 9$ results in $V_X = 57\text{mV}$
- $i_{f2} = 3$ - w.i. not allowed $\rightarrow$ current very sensitive to $V_X$
  - s.i. operation increases $V_{GSN}$ & $V_{DD_{min}}$
- $V_X = 57\text{mV}$, $N=1$ and $i_{f2} = 3$ results in $\alpha(\text{M.I}) = 3.4 < \alpha(\text{W.I})$
- For the P-mirrors $i_f < 1 \rightarrow V_{DSSATP} = 100\text{mV}$
5. Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simple topology K=9, N=1</th>
<th>Symmetric topology, K=1 N=1</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>AMIS 1.5µm</td>
<td>0.35µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{DDmin}</td>
<td>Simulation * 1.1</td>
<td>Experiment 1.1</td>
<td>1.05</td>
</tr>
<tr>
<td>Power (at 1.1V)</td>
<td>1.5</td>
<td>1.5</td>
<td>2.0</td>
</tr>
<tr>
<td>V_{ref} sensitivity to V_{DD}</td>
<td>0.9</td>
<td>1.6</td>
<td>0.85</td>
</tr>
<tr>
<td>V_{ref} sensitivity to T</td>
<td>+0.32</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>I_{ref} sensitivity to V_{DD}</td>
<td>4.7</td>
<td>6.2</td>
<td>4.0</td>
</tr>
<tr>
<td>I_{ref} sensitivity to T</td>
<td>+0.047</td>
<td>0.3</td>
<td>0.32</td>
</tr>
<tr>
<td>Efficiency (I_{ref}/I_{total})</td>
<td>25</td>
<td>25</td>
<td>20</td>
</tr>
</tbody>
</table>

* Simulation run with BSIM3 parameters provided by MOSIS
5. Results

TRANSISTOR SIZES FOR THE SYMMETRIC TOPOLOGY IN TSMC 0.35µm

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W [µm]</th>
<th>L [µm]</th>
<th>i_f</th>
</tr>
</thead>
<tbody>
<tr>
<td>M_1</td>
<td>2</td>
<td>18x60*</td>
<td>10.2</td>
</tr>
<tr>
<td>M_2</td>
<td>2</td>
<td>15x60*</td>
<td>3</td>
</tr>
<tr>
<td>M_3</td>
<td>10</td>
<td>6</td>
<td>0.008</td>
</tr>
<tr>
<td>M_4</td>
<td>4x10</td>
<td>6</td>
<td>0.001</td>
</tr>
<tr>
<td>M_{5-7, 10} &amp;</td>
<td>4</td>
<td>10</td>
<td>0.04</td>
</tr>
<tr>
<td>M_{8-9} &amp;</td>
<td>10</td>
<td>6</td>
<td>0.004</td>
</tr>
</tbody>
</table>

*Trapezoidal transistors. Dimensions of transistor connected to the source are W and L while the one connected to the drain is sized 8W and L. * Series association of 18 (15) transistors having W=2µm and L=60µm.
5. Results

Experimental (1.5µm)

Simulation

Experiment

Vref

Micrograph

200µm

230µm

Iref [A]

VDD [V]

Vref

http://eel.ufsc.br/LCI/work_master.html
5. Results

Experimental (0.35um)

Micrograph
6. Summary and conclusions

• Successful generation of current references of the order of 400 pA in AMIS 1.5µm & TSMC 0.35µm;

• The consumption of the core cell is 4*I_{ref} or 3*I_{ref};

• Experimental results demonstrated the design correctness;

• Circuit operates from 1.1 V in 1.5 µm technology and potentially operates from 0.7 V in 0.18 µm technology;

• Performance of the self-biased current reference is better than other SBCS reported so far.
Acknowledgments

We are specially indebted to MOSIS for providing us access to silicon