Operation of the Classical CMOS Schmitt Trigger As an Ultra-Low-Voltage Amplifier

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***Abstract*—In this brief, we analyze the operation of the classical Schmitt trigger (ST) circuit as an ultra-low-voltage (ULV) amplifier. Small-signal analysis is employed in order to determine optimum relative transistor sizes, which maximize the voltage gain. A comparison of the classical ST with the standard inverter highlights the relative benefits and drawbacks of each for operation as an amplifier in ULV applications. It is shown that the theoretical minimum supply voltage of the ST for voltage amplification (absolute voltage gain ≥ 1) is 31.5 mV at 300 K, which is below the well-known 36 mV limit of the standard inverter. Two test chips in a 180 nm technology with ST circuits built from transistors with different relative sizes were fabricated. For $V_{DD} = 60$ mV and 100 mV, the values measured for the voltage gain of the ST were 6 and 32 dB, respectively, which are significantly higher than the values of 4.4 and 15 dB simulated for the standard inverter at the same supply voltages.**

***Index Terms*—Schmitt trigger, ultra-low voltage, subthreshold operation, ultra-low-voltage amplifier.**

I. Introduction

CONVENTIONAL methods for achieving high voltage gain under extremely low supply voltages are not appropriate due to the difficulty associated with imposing that the transistors operate in saturation [1], [2]. An interesting technique to mitigate this drawback is the use of positive feedback to generate a compensating negative conductance for the purpose of enhancing the amplifier gain [3], [4]. However, the structures proposed in [3] and [4] rely on the existence of differential signals to generate a negative resistance to compensate the positive resistance at the output. Generating differential voltages with low supply voltages is not an easy task. Thus, we have opted to make use of the positive feedback in the Schmitt trigger circuit to obtain a high-gain amplifier.

The classical Schmitt trigger (ST) shown in Fig. 1 has been employed as a key element in several low voltage circuits [5]–[8]. One of the main results of [9] is the determination of the minimum supply voltage to obtain hysteresis with the ST circuit. Below this voltage the ST can be advantageously used as a high-gain amplifier for ULV applications, *i.e.,* supply voltages of the order of 100 mV, or less. As presented in [6], ST-based logic gates can operate at voltages as low as 62 mV.

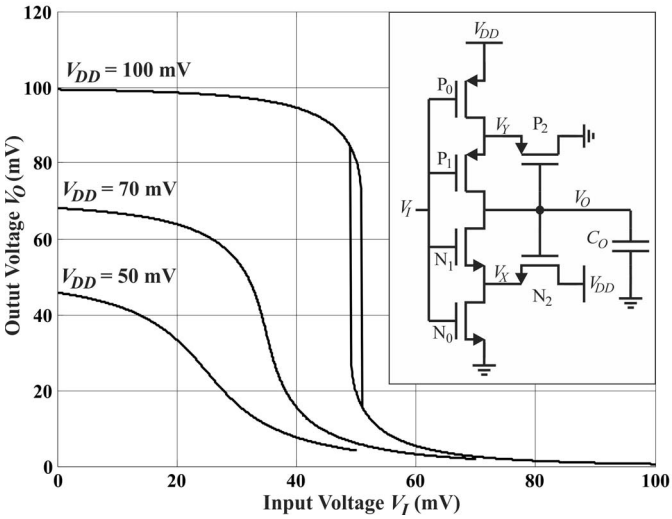

Fig. 1. VTCs of the classical 6-transistor Schmitt trigger circuit with $I_1/I_0 = I_2/I_0 = 1$ for $V_{DD} = 50$ mV, 70 mV, and 100 mV, and $n = 1$.

This brief explores the use of the conventional 6-transistor ST as an amplifier for ULV applications. In Section II, the voltage transfer characteristic of the ST is shown briefly. In Section III, the small-signal voltage gain is determined as a function of both the relative aspect ratios of the transistors and the supply voltage and optimum transistor aspect ratios are calculated to maximize the absolute voltage gain. In Section IV, the ST voltage gain is compared with that of the standard CMOS inverter. Section V presents experimental and simulation results, while the main conclusions of this brief are summarized in Section VI.

II. DC Transfer Characteristics

Figure 1 shows the voltage transfer characteristic (VTC) of the ST, from the DC node equations of [9], under the assumption of a symmetric ST for which the transistors operate in the subthreshold region [1], [10]. The transistor current scaling factor, $I_{N(P)}$, in Eq. (1), which represents the transistor strength, is dependent on both technological and geometrical parameters. μ is the carrier mobility, n is the slope factor, C'_{ox}

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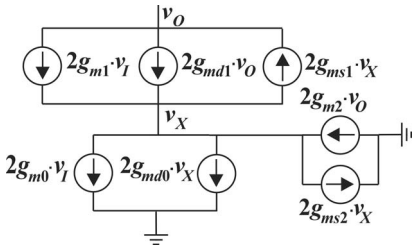

Fig. 2. Small-signal model of the Schmitt trigger, for $V_I = V_O = V_{DD}/2$. The NMOS and PMOS subcircuits are assumed to have the same strength.

is the oxide capacitance per unit area, ϕ_t is the thermal voltage, W/L is the aspect ratio, and V_{T0} is the threshold voltage. For a symmetrical ST, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, and $I_{N2} = I_{P2} = I_2$, and $n_N = n_P = n$.

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C_{ox}^{'} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{T0N(P)}|}{n_{N(P)}\cdot\phi_t}+1} \tag{1}$$

For $V_{DD} = 100$ mV, the VTC shows hysteresis, but for $V_{DD} = 70$ mV and for $V_{DD} = 50$ mV it does not. It has been proved in [9] that the ST of Fig. 1 does not present hysteresis for supply voltages of less than 75 mV at room temperature. In real cases, where the slope factors of the transistors are higher than the unity, the ST does not exhibit hysteresis for supply voltages of below around 100 mV.

In the following, we assume that the ST is symmetric and operates as an amplifier (without hysteresis), unless otherwise noted.

III. Small-Signal Analysis

To derive the AC characteristics of the Schmitt trigger, the equivalent small-signal model [9], [10], composed of three transconductances, replaces each MOSFET of Fig. 1. In the AC model, g_m, g_{md}, and g_{ms} are the gate, drain and source transconductances, respectively.

The small-signal circuit of an ST composed of NMOS and PMOS subcircuits with the same strength, for $V_I = V_O = V_{DD}/2$, the voltage at which the gain is maximum, is shown in Fig. 2. Here v_I, v_O, and v_X are small-signal voltages. Note that for a symmetric ST with $V_I = V_O = V_{DD}/2$, we have $v_X = v_Y$. The factor 2 in the small-signal model accounts for the symmetric PMOS and NMOS networks.

Applying KCL to v_X, and v_O, results in

$$\begin{aligned} G_m &= \left.\frac{i_O}{v_I}\right|_{v_O=0, V_O=V_I=V_{DD}/2} = -2\frac{g_{m1}\cdot(g_{ms2}+g_{md0})+g_{ms1}\cdot g_{m0}}{g_{ms1}+g_{ms2}+g_{md0}}; \\ G_o &= \left.\frac{i_O}{v_O}\right|_{v_I=0, V_O=V_I=V_{DD}/2} = -2\frac{g_{md1}\cdot(g_{ms2}+g_{md0})-g_{ms1}\cdot g_{m2}}{g_{ms1}+g_{ms2}+g_{md0}}. \end{aligned} \tag{2}$$

G_m and G_o are the transconductance and output conductance, respectively. The values of the transconductances are given in Table I for $V_I = V_O = V_{DD}/2$ [9]. The value of $V_{X0} = V_X(V_I = V_O = V_{DD}/2)$, also derived in [9], is

$$e^{\frac{V_{X0}}{\phi_t}} = \frac{I_0 + I_1 + I_2}{I_0 + I_1\cdot e^{-\frac{V_{DD}}{2\phi_t}} + I_2\cdot e^{-\frac{V_{DD}}{\phi_t}}}. \tag{3}$$

By substituting the transconductances of the MOSFETs from Table I and (3) into (2), we obtain, after some lengthy algebra

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{G_m}{G_o} = \frac{\left(e^{\frac{V_{DD}}{2\phi_t}}-1\right)\cdot\left(1+\frac{I_1}{I_0}+2\frac{I_2}{I_0}\right)+\left(\frac{I_2}{I_0}\right)^2\cdot\left(e^{-\frac{V_{DD}}{2\phi_t}}-1\right)}{\frac{I_2}{I_0}\cdot\left(e^{\frac{V_{DD}}{2\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)+\frac{I_1}{I_0}\cdot\frac{I_2}{I_0}\cdot\left(1-e^{-\frac{V_{DD}}{2\phi_t}}\right)-n\cdot\left(1+\frac{I_2}{I_0}\right)\cdot\left(1+\frac{I_1}{I_0}+\frac{I_2}{I_0}\right)} \tag{4}$$

The plot of the ST voltage gain, equation (4), is shown in Fig. 3 as a function of the transistor ratios I_1/I_0 and I_2/I_0, for $V_{DD} = 60$ mV, and $n = 1$. As shown in the figure, when the feedback strength I_2/I_0 is high, the ST voltage gain is positive. It is important to note that there is a maximum absolute gain for I_0 close to I_2 and I_1 much smaller than I_0.

TABLE I
Transconductances of the Schmitt Trigger for $V_{DD} = V_O = V_I = V_{DD}/2$ [9]

	g_{ms}	g_{md}	g_m
N_0 or P_0		$\frac{I_0}{\phi_t}e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_0}{n\phi_t}e^{\frac{V_{DD}}{2n\phi_t}}\left(1-e^{-\frac{V_{X0}}{\phi_t}}\right)$
N_1 or P_1	$\frac{I_1}{\phi_t}e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$	$\frac{I_1}{\phi_t}e^{\frac{V_{DD}}{2\phi_t}\left(\frac{1}{n}-1\right)}$	$\frac{I_1}{n\phi_t}e^{\frac{V_{DD}}{2n\phi_t}}\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}\right)$
N_2 or P_2	$\frac{I_2}{\phi_t}e^{\frac{V_{DD}}{2n\phi_t}-\frac{V_{X0}}{\phi_t}}$		$\frac{I_2}{n\phi_t}e^{\frac{V_{DD}}{2n\phi_t}}\left(e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}\right)$

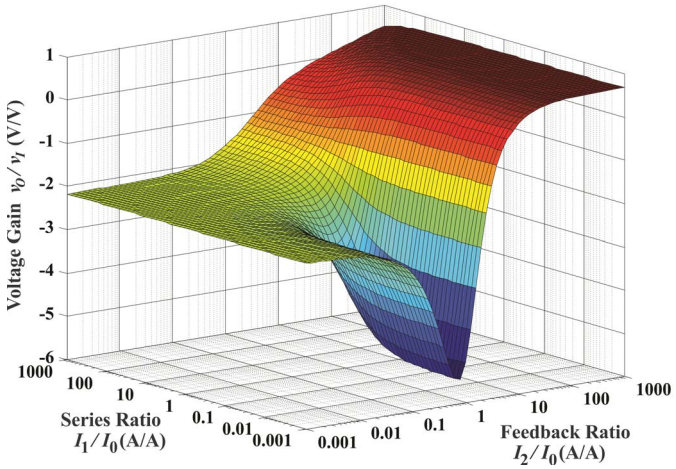

Fig. 3. Small-signal voltage gain for $V_{DD} = 60$ mV and $n = 1$.

A. Optimum Series Transistor Ratio I_1/I_0

Rearranging (4) in terms of I_1/I_0 results in the bilinear function given in (5). Coefficients A_1, B_1, C_1, and D_1 are dependent on both the supply voltage and the ratio I_2/I_0. The maximum absolute gain is obtained when $I_1/I_0 \to 0$, as given in (6). The effect of the transistor ratio I_1/I_0 is shown in Fig. 4.

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{\frac{I_1}{I_0}\cdot A_1 + B_1}{\frac{I_1}{I_0}\cdot C_1 + D_1}. \tag{5}$$

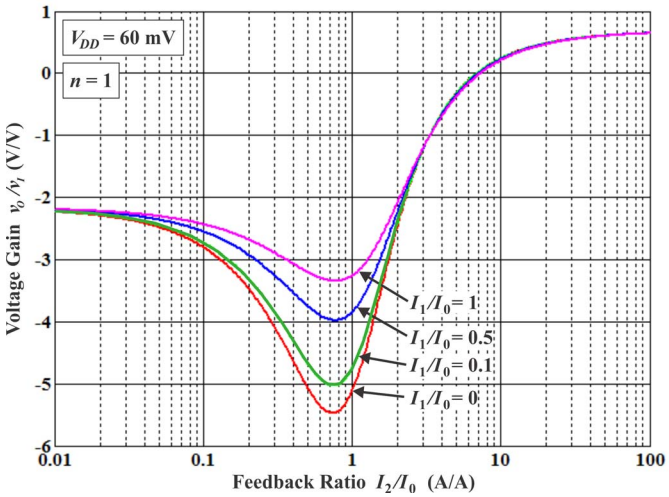

Fig. 4. Small-signal voltage gain of the ST for $V_{DD} = 60$ mV, and $n = 1$, for different I_1/I_0 ratios, as a function of the I_2/I_0 ratio.

$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} \to 0. \tag{6}$$

For $V_{DD} = 60$ mV, a I_1/I_0 ratio higher than 0.1 results in a considerable reduction in the maximum achievable voltage gain, *e.g.*, it is -5.0 V/V and -3.3 V/V, for $I_1/I_0 = 0.1$ and $I_1/I_0 = 1$, respectively.

B. Optimum Feedback Transistor Ratio I_2/I_0

Rearranging (4) in terms of I_2/I_0, results in

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{\left(\frac{I_2}{I_0}\right)^2 \cdot A_2 + \left(\frac{I_2}{I_0}\right) \cdot B_2 + C_2}{\left(\frac{I_2}{I_0}\right)^2 \cdot D_2 + \left(\frac{I_2}{I_0}\right) \cdot E_2 + F_2}. \tag{7}$$

Coefficients A_2, B_2, C_2, D_2, E_2, and F_2, are dependent on both the supply voltage and I_1/I_0. For $I_1/I_0 = 0$ we have

$$\begin{aligned} A_2 &= e^{-\frac{V_{DD}}{2\phi_t}} - 1; B_2 = C_2 = e^{\frac{V_{DD}}{2\phi_t}} - 1 \\ D_2 &= F_2 = -n; E_2 = e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}} - 2n. \end{aligned} \tag{8}$$

The gain given by (7), for $I_1/I_0 = 0$, is maximum for

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{\left(n^2 - n + 1\right) + e^{\frac{V_{DD}}{2\phi_t}} \cdot (2 \cdot n - 1) - e^{-\frac{V_{DD}}{2\phi_t}}} - n}{2 \cdot n - 1 + e^{-\frac{V_{DD}}{2\phi_t}}}. \tag{9}$$

Table II shows the optimum values of I_2/I_0 which result in the maximum absolute voltage gain, for different supply voltages, with $I_1/I_0 = 0$ and $n = 1$. It is important to observe that at ultra-low voltages the optimum I_2/I_0 is strongly dependent on the supply voltage. It varies from 1/3 at 31.5 mV to 1 at the hysteresis voltage (75 mV).

IV. Comparison Between the ULV Schmitt Trigger and the Conventional Inverter

Without feedback ($I_2 = 0$) the ST reduces to the conventional CMOS inverter; thus, Eq. (4) yields

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{e^{\frac{V_{DD}}{2\phi_t}} - 1}{n}, \tag{10}$$

TABLE II
Optimum Values of I_2/I_0 for Different Supply Voltages

V_{DD} (mV)	Optimum I_2/I_0	Optimum Gain (V/V)
75	1.00	-∞
70	0.91	-20.23
60	0.73	-5.58
50	0.58	-2.76
40	0.44	-1.57
31.5	0.33	-1.00

which was derived for the first time in [11] and verified by many authors, *e.g.,* [12] and [13]. The well-known minimum allowable supply voltage of the inverter of $2\phi_t \ln 2 = 36$ mV at room temperature [11]–[14] is obtained by making the gain given by (10) equal to -1 for $n = 1$.

In the case of the ST, on substituting the optimum values of I_1/I_0 and I_2/I_0 from (6) and (9), respectively, into (4), the minimum value of the supply voltage for a voltage gain equal to -1 is

$$V_{DD\,\min} = 2\phi_t \cdot \ln\left(\frac{8 + \sqrt{73}}{9}\right) = 31.5\text{mV at 300K}, \tag{11}$$

which is achieved for $I_1/I_0 \to 0$, $I_2/I_0 = 1/3$, and $n = 1$.

Interestingly, the ST inverter is theoretically capable of operating as a unity-gain amplifier for supply voltages down to 31.5 mV. This reduction on the minimum supply voltage is a consequence of the positive feedback which increases the voltage gain of the ST. Although the difference between the minimum supply voltage of the inverter, and that of the Schmitt trigger is small (12.2%), only 4.4 mV at 300 K, it is of relevance because it exceeds the previously stated limit for the low-voltage operation of CMOS logic. It is important to remark that a slight reduction in the minimum supply voltage does not imply a reduction in the minimum switching energy since the capacitances of the ST are always higher than the capacitances of the equivalent inverter. As derived in [14] the *fundamental limit* on binary switching energy of $kT \cdot \ln 2$ occurs for a *single electron* CMOS inverter operating at the minimum supply voltage of $2\phi_t \ln 2$.

The ST has another beneficial characteristic when operating with ultra-low supply voltages: it is less susceptible to variations in technological parameters than the conventional inverter. This is due to the fact that, in contrast to the standard inverter, the pull-up network of the ST inverter is composed of both P-channel (P_0 and P_1) and N-channel (N_2) transistors. Thus, if the strength of the NMOS transistors is higher than that of the PMOS transistors, this difference is partially compensated in the pull-up circuit. A comparison between the VTCs of the standard inverter and the ST inverter is shown in Fig. 5, for $V_{DD} = 70$ mV, and ± 30 mV variations in the threshold voltage of the NMOS and PMOS transistors, with $I_1/I_0 = I_2/I_0 = 1$. As can be observed, for $V_{DD} = 70$ mV, the VTC of the ST is appropriate for logic circuits even considering the process variation, which is not the case for the conventional inverter.

V. Simulation and Experimental Results

The analytical and simulation results motivated us to design and fabricate test chips in an IBM 180-nm technology. In both the simulation and the fabricated designs, the length of the

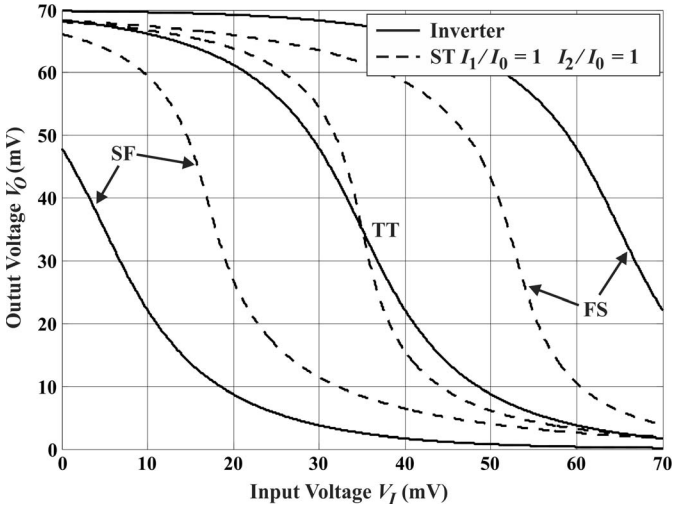

Fig. 5. Comparison between the VTCs of the standard inverter and the ST, with $I_1/I_0 = I_2/I_0 = 1$, under a ±30 mV threshold voltage variation, for $V_{DD} = 70$ mV, and $n = 1$. T: typical, S: slow, F: fast.

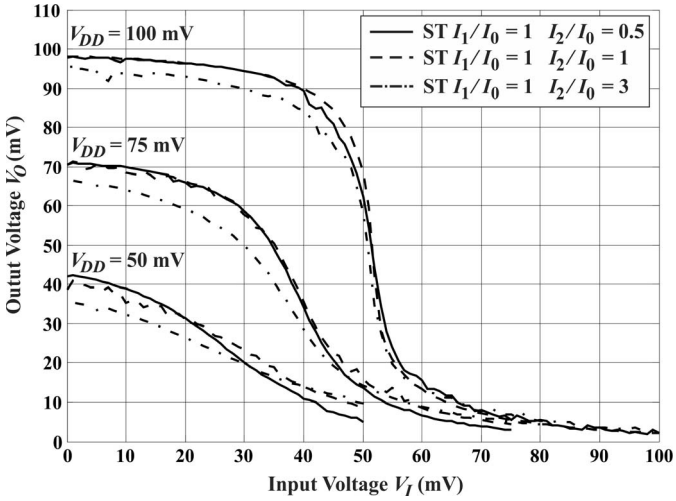

Fig. 6. Measured VTCs of the ST with $I_1/I_0 = 1$ and $I_2/I_0 = 0.5, 1$, and 3 for $V_{DD} = 50$ mV, 75 mV, and 100 mV.

transistors was fixed at 6 times the minimum transistor length allowed by the technology ($L_{MIN} = 180$ nm), in order to minimize both the short-channel effects and the threshold voltage spread. The simulations were run in Cadence Spectre, with BSIM 3v3 transistor model, and design kit provided by the foundry.

The VTCs of 3 ST circuits with different relative transistor strengths ($I_1/I_0 = 1$, and $I_2/I_0 = 0.5, 1, 3$), measured on an HP 4145C semiconductor parameter analyzer, are shown in Fig. 6 for supply voltages of 50 mV, 75 mV, and 100 mV. As expected, for supply voltages of 100 mV or less, none of the curves exhibit hysteresis [9]. For $V_{DD} = 50$ mV, the maximum absolute voltage gain is higher than unity only in the case of the ST with $I_2/I_0 = 0.5$. For $V_{DD} = 100$ mV, the maximum absolute gain for the ST with $I_2/I_0 = 0.5$ is around 10.3 V/V (or 20.2 dB), whereas for the other two, it is greater than 10 V/V (or 20 dB).

In order to compare some specifications of the ST and the standard inverter, we ran some simulations, with the NMOS and PMOS networks having the same relative current strengths for the ST and the standard inverter.

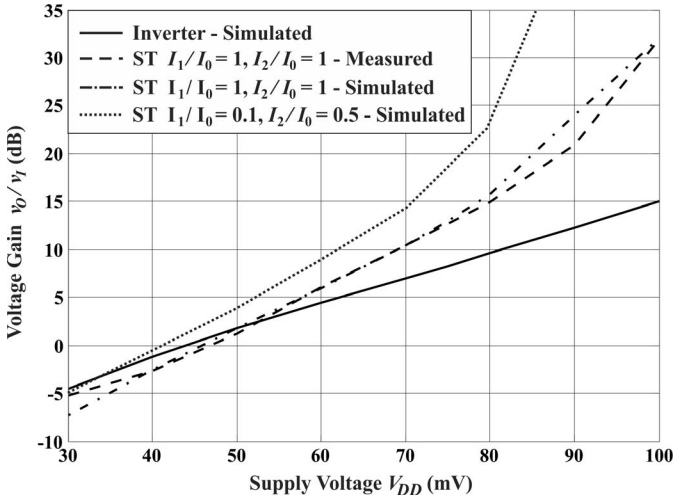

Fig. 7. Comparison between the voltage gains of a simulated inverter with simulated and measured values for STs.

TABLE III
ASPECT RATIOS (μm/μm) OF THE TRANSISTORS FOR FIG. 7

Device	I_1/I_0	I_2/I_0	P_0	P_1	P_2
ST1	1.0	1.0	14/1.08	14/1.08	14/1.08
ST2	0.1	0.5	10x 14/1.08*	14/1.08	10x 7/1.08*
Inverter	–	–	14/1.08	–	–
Device	I_1/I_0	I_2/I_0	N_0	N_1	N_2
ST1	1.0	1.0	1.08/1.08	1.08/1.08	1.08/1.08
ST2	0.1	0.5	10x 1.08/1.08*	1.08/1.08	10x 0.54/1.08*
Inverter	–	–	1.08/1.08	–	–

* x is associated with the number of transistors in parallel

A comparison between simulated and measured voltage gains for a simulated inverter and for two STs with different transistor ratios, designed as shown in Table III, is shown in Fig. 7 for supply voltages ranging from 30 mV to 100 mV.

The simulation and measurement results for the STs are well matched and show that, for supply voltages higher than around 34 mV, the voltage gain of ST2 is higher than that of the simulated inverter. At 80 mV, the voltage gain of ST2 is 13.2 dB higher than that of the standard inverter.

A second test chip was also fabricated in a 180 nm technology. Measurements in 30 available chip samples reveal that, in all cases, the minimum supply voltage that results in a voltage gain equal −1 V/V is lower for the ST than for the inverter, as summarized in Fig. 8. The minimum supply voltage for a unity voltage gain of the ST ranges between 40 mV and 43 mV, and between 44 mV and 45 mV for the inverter. Although the difference is only a few millivolts, the minimum V_{DD} for achieving a voltage gain of unity is always lower for the ST than for the inverter. The measured minimum supply voltage higher than the value of 31.5 mV of Eq. (11) is due to two reasons. First, the slope factor of the MOSFETs is higher than unity and, second, the ST was optimized for having maximum gain at $V_{DD} = 40$ mV.

In order to compare the frequency response of the ST with that of the inverter, two ST-based (one with $I_1/I_0 = I_2/I_0 = 1$ and another with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$) and one

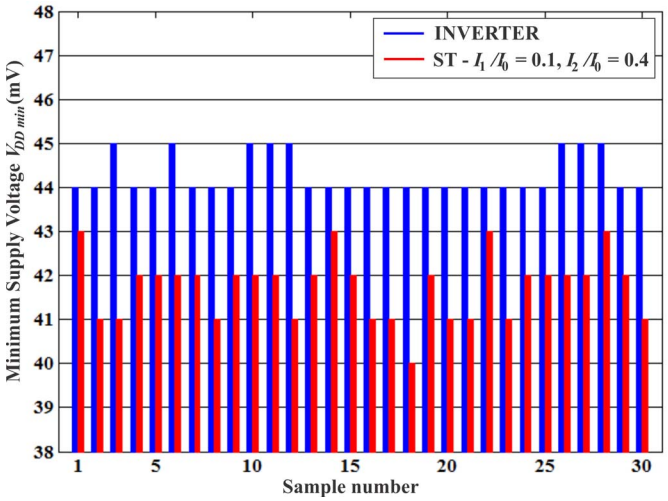

Fig. 8. Measured minimum supply voltage of both the ST and the inverter on 30 samples. The ST transistor sizes are: $(W/L)_{P0}$ = 22μm/1.08 μm, $(W/L)_{P1}$ = 2.2μm/1.08 μm, $(W/L)_{P2}$ = 8.8μm/1.08 μm, $(W/L)_{N0}$ = 2.2μm/1.08 μm, $(W/L)_{N1}$ = 0.22μm/1.08 μm, $(W/L)_{N2}$ = 0.88μm/1.08 μm. The inverter transistor sizes are: $(W/L)_P$ = 7.7μm/1.08 μm, $(W/L)_N$ = 2.2μm/1.08 μm.

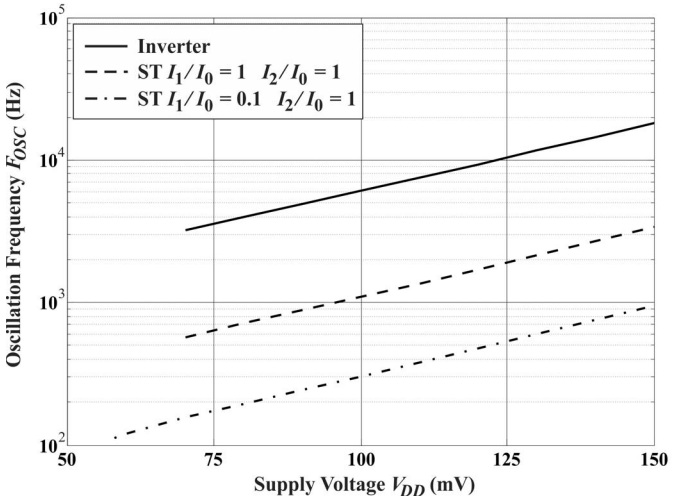

Fig. 9. Comparison between the oscillation frequencies of the simulated ST and inverter based 3-stage ring oscillators.

inverter-based 3-stage ring oscillators (ROs) were simulated. As expected, the operating frequency of the ST-based RO at a fixed supply voltage is lower than that of the inverter-based RO, because the ratio of the current drive capability to the output node capacitance is smaller for the ST than for the standard inverter.

Figure 9 shows a comparison between the oscillation frequency of the ST and the inverter-based ROs as a function of the supply voltage. Below 70 mV of supply voltage, both the ST with $I_1/I_0 = I_2/I_0 = 1$ and the inverter ROs do not oscillate due to the low voltage gain. However, the RO composed of STs with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$ oscillates at a supply voltage as low as 57 mV, even though the frequency is extremely low. It can be seen that the oscillation frequency of the inverter-based RO is around 5.5 times higher than that of the ST-based RO with $I_1/I_0 = I_2/I_0 = 1$, and 19.6 times higher if compared to the ST-based RO with $I_1/I_0 = 0.1$ and $I_2/I_0 = 1$.

VI. Conclusion

In this brief, analytical expressions were derived for the operation of the Schmitt trigger as an amplifier. When no hysteresis is present, optimum transistor aspect ratios can be determined for maximum voltage gain. It was shown that, theoretically, the ST is able to provide a voltage gain higher than unity for a supply voltage as low as 31.5 mV at room temperature, which is lower than the previously reported value of 35.9 mV [12]–[14] of the CMOS technology for the operation of logic circuits.

Not only the higher gain, but also the weaker dependence of the transfer characteristic of the Schmitt trigger on the process parameters, compared to the standard inverter, is of great importance in ultra-low-voltage applications. The price to be paid for using STs rather than standard circuits for ultra-low-voltage applications is the larger area and slower time response.

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