ABOUT THE CONCEPT OF THRESHOLD IN MOS TRANSISTORS

M. C. Schneider, C. Galup-Montoro, M. B. Machado, and A. I. A. Cunha*

Department of Electrical Engineering, Federal University of Santa Catarina,
Florianópolis, SC, CEP 88040-900, Brazil,
*Department of Electrical Engineering, Federal University of Bahia
Escola Politécnica, Salvador, BA, CEP 40210-630, Brazil
e-mails: {marcio,carlos,marciobm}@eel.ufsc.br, aiac@ufba.br

ABSTRACT

This paper presents a brief discussion on the main MOSFET threshold voltage definitions available in the literature as well as on associated extraction methodologies. In order to compare these definitions and methodologies, we take advantage of the Advanced Compact MOSFET (ACM) model, which accurately relates surface potential to inversion charge density in all regions of operation.

INTRODUCTION

The threshold voltage V_T is a fundamental parameter in the modeling and characterization of MOS transistors.

Several different definitions of threshold voltage have been presented in the literature (1). To shed some light on the V_T-extraction problem we will use a one-equation-all-regions model (2,3) to calculate the band bending, total inversion charge at threshold, and the slight differences among the threshold voltages for the main extraction procedures.

Out of the many extraction methods available for determining V_T, most of them use some transfer characteristic measured under low drain-to-source voltages ($V_{DS}<2kT/q$) (1). At least, a dozen of methods (with their relative advantages/disadvantages) to extract the threshold voltage in the linear region (low drain-to-source) are available (1,4,5,6). However, no matter what method the user chooses to determine V_T, the measurements should be clearly interpreted in terms of a decent model.

In this study, we compare the traditional ELR (Extrapolation in the Linear Region), the TC/SDL (Transconductance Change / Second Derivative Logarithmic), the constant-current (CC), and the g_m/I_D (transconductance-to-current ratio) (5) methods for threshold voltage extraction.

The ACM (Advanced Compact MOSFET) model (2,3) is summarized in the following Section. In the third Section, simple formulas for different definitions of the threshold voltage and the corresponding extraction methods are summarized. In the fourth Section we show experimental results obtained in accordance with the methods described here for devices in a 0.18 μm CMOS technology. The fifth Section summarizes the definitions and interpretation of the threshold voltage corresponding to each extraction procedure discussed in this paper.

THE ACM MODEL

The ACM model consists of simple, accurate, and single equations that represent the device behavior in all regimes of operation, using well-known physical parameters (2,3).

$$Q'_I \cong C'_{ox}\, n[\phi_s - \phi_{sa}] \tag{1a}$$

$$n = 1 + \frac{C'_b}{C'_{ox}} = 1 + \frac{\gamma}{2\sqrt{\phi_{Sa}}} \tag{1b}$$

$$\phi_{Sa} = \left(\sqrt{V_G - V_{FB} + \frac{\gamma^2}{4}} - \frac{\gamma}{2} \right)^2 \tag{1c}$$

In (1), Q'_I is the inversion charge density, C'_{ox} is the oxide capacitance per unit area and C'_b is the depletion capacitance calculated assuming the inversion charge to be negligible. n is the slope factor, slightly dependent on the gate voltage V_G, γ is the body factor, and V_{FB} is the flat-band voltage. ϕ_s is the surface potential and ϕ_{sa}, given by (1c), is the value of the surface potential deep in weak inversion, neglecting the inversion charge. Unless stated otherwise, the voltages herein are referred to the substrate.

The pinch-off voltage V_P is given by (2):

$$V_P = \phi_{Sa} - \phi_0 \tag{2a}$$

with

$$\phi_0 = 2\phi_F + \phi_t \left[1 + \ln\left(\frac{n}{n-1} \right) \right] \tag{2b}$$

In (2b), ϕ_F is the Fermi potential of the substrate and ϕ_t is the thermal voltage.

In the ACM model, the static and dynamic characteristics are expressed either in terms of inversion charge densities at source (Q'_{IS}) and drain (Q'_{ID}), or in terms of forward saturation (I_F) and reverse saturation (I_R) components of the drain current (2,3). The expressions of the ACM model to be used in this work are summarized in Table I. In this table, q'_{IS} and q'_{ID} represent the charge densities normalized with respect to the pinch-off charge Q'_{IP}. $V_{S(D)}$ is the source(drain)-bulk voltage. I_D is the drain current and $g_m = \partial I_D / \partial V_G$ is the gate transconductance.

The normalized saturation currents (i_f and i_r) are equal to the saturation currents (I_F and I_R) normalized with respect to the specific current I_S (2,3).
Expressions (3), (4) and (5) are derived in (2,3).

Table I: Expressions of the ACM model

Variable	Charge-Based Expression	Current-Based Expression	
I_D	$I_S(q'_{IS}-q'_{ID})(q'_{IS}+q'_{ID}+2)$	$I_S(i_f-i_r)$	(3)
g_m	$\frac{2I_S}{n\phi_t}(q'_{IS}-q'_{ID})$	$\frac{2I_S}{n\phi_t}\left(\sqrt{1+i_f}-\sqrt{1+i_r}\right)$	(4)
V_P-$V_{S(D)}$	$\phi_t\left[q'_{IS(D)}-1+\ln\left(q'_{IS(D)}\right)\right]$	$\phi_t\left[\sqrt{1+i_{f(r)}}-2+\ln\left(\sqrt{1+i_{f(r)}}-1\right)\right]$	(5)

The expression of the surface potential ϕ_S can be derived from (1a), (2) and (5), resulting in

$$\phi_S = 2\phi_F + V_C + \phi_t \ln\left(\frac{n}{n-1}q'_I\right) \tag{6}$$

In (6), V_C is the quasi-Fermi splitting (channel-to-substrate-voltage) and q'_I is the normalized inversion charge density.

THRESHOLD VOLTAGE DEFINITIONS AND ASSOCIATED EXTRACTION PROCEDURES

In this Section, we review some common methods to determine the threshold voltage and interpret the results obtained using the ACM model. In all the extraction methods discussed here, we assume that the drain-to-source voltage is small to such an extent that the inversion charge densities (or surface potentials) at source and drain are about the same.

A. Classical definition of the threshold voltage

V_{T0} is the gate voltage for which the electron concentration at the semiconductor interface equals the hole concentration in the bulk or, equivalently, $\phi_S = 2\phi_F$. Using this value of the surface potential in (6), one finds that the normalized charge $q'_{IT0} = (n-1)/n$ for V_G=V_{T0} and V_C=*0*. Substituting $q'_{IT0} = (n-1)/n$ for q'_{IS} in (3) and (4) results in

$$\frac{g_m}{I_D}\Big/\left(\frac{g_m}{I_D}\right)_{\max} = \frac{n}{2n-1} \tag{7}$$

Expression (7) means that the determination of the classical threshold voltage from the relative (to the maximum) transconductance-to-current ratio requires the accurate determination of the slope factor *n* for values of gate voltage around the threshold voltage.

B. Threshold definition by extrapolation of strong inversion current characteristic

The description of the ELR (Extrapolation in the Linear Region) method, which relies on the linear relation between the drain current and the gate voltage (in the linear region and in strong inversion), is described in (1,6). Even though the ELR method is very simple, it is prone to the influence of factors such as mobility degradation due to transversal field, series resistances of source and drain, and nonlinear relationship between inversion charge density and gate voltage (6).

C. Threshold definition by maximum of $\partial g_m/\partial V_G$ or minimum of $\partial^2 \ln I_D/\partial V_G^2$

A conceptually correct method to determine the (approximate) threshold voltage is based on the transconductance change (TC) (1). This method consists in measuring the variation in the transconductance with respect to the gate voltage and determining the maximum of this variation.

The application of the charge-based expression in (5) to both the source and drain terminals allows writing

$$\frac{V_{DS}}{\phi_t} = \left(q'_{IS} - q'_{ID}\right)\frac{q'_{IS}+1}{q'_{IS}} \tag{8a}$$

for $V_{DS}<<\phi_t$. Now, substituting the value of $\left(q'_{IS} - q'_{ID}\right)$ given by eq.(4) into (8a) one obtains

$$g_m = \mu C'_{ox}\frac{W}{L}V_{DS}\frac{q'_{IS}}{q'_{IS}+1} \tag{8b}$$

We calculate the transconductance change assuming the mobility to be constant (an approximation quite acceptable for gate voltages near the threshold voltage). Thus, from (8b)

$$\frac{dg_m}{dV_G} = \mu C'_{ox}\frac{W}{L}V_{DS}\frac{d}{dq'_{IS}}\left(\frac{q'_{IS}}{q'_{IS}+1}\right)\frac{dq'_{IS}}{dV_P}\frac{dV_P}{dV_G} \tag{8c}$$

Recalling that the rightmost derivative in (8c) equals *1/n* and using eq.(5) we find that

$$\frac{dg_m}{dV_G} = \mu C'_{ox}\frac{W}{L}\frac{V_{DS}}{n\phi_t}\frac{q'_{IS}}{\left(q'_{IS}+1\right)^3} \tag{8d}$$

The normalized inversion charge density at which the derivative of the transconductance is a maximum is $q'_{IS} = 0.5$ or, equivalently, $Q'_{IS} = 0.5Q'_{IP}$.

As regards the method based on the determination of the minimum of the second difference of the logarithm (SDL) of the drain current (1) to extract the threshold voltage,

we just give below the expression that relates the SDL and TC methods for small $V_{DS} \rightarrow 0$:

$$\frac{dg_m}{dV_G} = -2I_S \frac{V_{DS}}{\phi_t} \frac{d^2 \ln I_D}{dV_G^2} \tag{9}$$

For the derivation of eq.(9) we have assumed that the variation of n with the gate voltage is negligible. From eq.(9), one can conclude that, for low values of V_{DS}, the threshold voltages determined by the TC and SDL methods are quite close to each other.

D. Threshold voltage definition by the constant current method

In the CC method (1), the gate voltage at which the drain current normalized by the transistor aspect ratio (W/L) equals a given value $I_{D.CC}$ is defined as the threshold voltage. Of course, the definition of the threshold voltage depends on the value chosen for $I_{D.CC}$. In the derivation that follows, we show that a choice of $I_{D.CC}$ based on the nominal values of mobility and gate oxide capacitance results in a value of the threshold voltage very close to its value based on the classical definition.

The substitution of the value of $\left(q'_{IS} - q'_{ID}\right)$ given by eq.(3) into expression (8a) results in

$$I_D = 2I_S \frac{V_{DS}}{\phi_t} q'_{IS} = 2I_{SQ} \frac{W}{L} \frac{V_{DS}}{\phi_t} q'_{IS} \tag{10a}$$

$$I_{SQ} = \mu C'_{ox} n \frac{\phi_t^2}{2} \tag{10b}$$

I_{SQ} is the sheet specific current (2), a technology parameter slightly dependent on bias through μ and n. I_{SQ} can be determined either from typical technology parameters or from test devices. Once the sheet specific current is known, the threshold voltage can be chosen as the gate voltage at which, e.g., $q'_{IS} = 1$ or, equivalently,

$$I_D \Big/ \left(\frac{W}{L}\right) = 2I_{SQ} \frac{V_{DS}}{\phi_t} \tag{10c}$$

Except for a possible difficulty in determining the effective channel length and width, the CC method is quite attractive for its simplicity and accuracy.

E. Threshold voltage definition based on the g_m/I_D characteristic

Basically, in the g_m/I_D method, the threshold voltage is defined as the gate voltage at which the value of g_m/I_D drops to one half of its peak value, as described in (5).

EXPERIMENTAL RESULTS

Measurements of the common-source characteristic in the linear region, with $V_{SB} = 0$ and $V_{DS} = 13\ mV$ have been taken for NMOS and PMOS transistors for a 0.18 μm CMOS technology. The devices were fabricated by TSMC.

Table II: Experimental results from proposed methodology (g_m/I_D), ELR, SDL, and CC methods for extracting the threshold voltage for a 0.18 μm CMOS technology. Sheet specific currents are I_{SQN}= 168 nA and I_{SQP}= 45.3 nA

Mask channel length (μm)	V_{T0} (mV) - NMOSFET				V_{T0} (mV) - PMOSFET			
	ELR	SDL	g_m/I_D	CC	ELR	SDL	g_m/I_D	CC
0.2	481	490	520	501	-486	-490	-523	-493
0.3	483	478	510	508	-453	-455	-480	-471
0.4	482	468	503	509	-449	-440	-470	-468
0.5	476	463	495	504	-446	-443	-468	-468
0.6	473	455	493	501	-442	-433	-463	-465
0.8	462	448	483	491	-438	-420	-455	-461
2.0	435	423	458	466	-424	-410	-443	-451

Table II exhibits the value of threshold voltage extracted for each test device through the g_m/I_D-based methodology, the ELR, the SDL, and the CC methods. One major drawback of the SDL method is the need for calculating the usually extremely noisy second order derivative of the current. On the other hand, the ELR method is not based on a physical definition of threshold voltage.

The comparison of the results obtained from the SDL and g_m/I_D methods show that the results follow the same trend for either P or N transistors. According to the result shown in Table II, $V_T(g_m/I_D) - V_T(SDL) = n\phi_t(0.5+ln2) \cong 1.2\ n\phi_t$. Since n is slightly higher than 1, the differences of the measurements obtained from the g_m/I_D and SDL methods should be, at least, 30 mV.

The CC method provides results very close to the g_m/I_D method, except for very short channel lengths. In fact, the CC and the g_m/I_D methods must give the same results for the threshold voltage as long as the aspect ratio of the transistor is correctly evaluated.

SUMMARY

In order to summarize the definitions and results concerning some methods for defining the threshold voltage, we have prepared Table III.

Table III - Threshold definitions and associated meaning and features

Threshold Definition	Physical Meaning	Value of ϕ_S at threshold	Value of $\mathbf{Q'_I}$ at threshold	Difference in equilibrium threshold voltage relative to V_{T0}**(#)**
$\boldsymbol{\phi_S = 2\phi_F + V_C}$	Surface concentration of electrons= bulk concentration of holes	$2\phi_F + V_C$	$-(n-1)C'_{ox}\phi_t$	0
$\boldsymbol{Q'_I = -nC'_{ox}\phi_t}$	50% drop (relative to the peak) in the g_m/I_D curve	$2\phi_F + V_C + \phi_t \ln\left(\frac{n}{n-1}\right)$	$-nC'_{ox}\phi_t$	$\phi_t\left[1+n\ln\left(\frac{n}{n-1}\right)\right]$ **(+)**
Extrapolated drain current (ELR)	Not clear physical meaning	Dependent on operating point (see text for details)	Not well defined	Dependent on operating point (see text for details)
$\boldsymbol{\max\left(\frac{dg_m}{\partial V_G}\right)}$ **or** $\boldsymbol{\min\left(\frac{d^2 \ln I_D}{dV_G^2}\right)}$	Peak on the second derivative curve	$2\phi_F + V_C + \phi_t \ln\left[\frac{n}{2(n-1)}\right]$	$-nC'_{ox}\frac{\phi_t}{2}$	$\phi_t\left\{1+n\left[\ln\left(\frac{n}{2(n-1)}\right)-0.5\right]\right\}$ **(+)**
Constant current (*)	Equal drift and diffusion components of drain current	$2\phi_F + V_{CB} + \phi_t \ln\left(\frac{n}{n-1}\right)$	$-nC'_{ox}\phi_t$	$\phi_t\left[1+n\ln\left(\frac{n}{n-1}\right)\right]$ **(+)**

(#) V_{T0} is the classical threshold voltage.

(*) In the CC method, we have set $q'_{IS}=1$.

(+) For the calculation of the equilibrium threshold voltage, we have linearized expression (5) as given below

$$\frac{V_P}{\phi_t} \cong \frac{V_G - V_{T0}^*}{n\phi_t} = q'_{IS} - 1 + \ln q'_{IS} \tag{11}$$

In eq.(11), V_{T0}^* is the gate voltage at which $q'_{IS}=1$, or the threshold voltage defined in accordance with the ACM model.

CONCLUSIONS

The interrelations between the main threshold voltage definitions and extraction procedures have been clarified using a one-equation-all-regions MOSFET model. Unambiguous definitions of threshold have been emphasized and relative advantages/disadvantages of some common extraction procedures have been commented on.

Owing to its ease of extraction, the CC method is the most suitable for measuring threshold voltage mismatch or time-dependent variation, but it is not convenient for determination of length dependence of the threshold voltage since the CC method requiries the knowledge of both W and L. On the other hand, the g_m/I_D is the most appropriate for determining the threshold voltage for usage as a MOSFET model parameter.

ACKNOWLEDGMENTS

The authors would like to thank CAPES and CNPq for the financial support and the MOSIS Educational Program for supplying the test devices.

REFERENCES

1. A. Ortiz-Conde, F. J. García Sánchez, J.J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, *Microelectronics Reliability*, 42, 583 (2002).
2. A. I. A. Cunha, M.C. Schneider, and C. Galup-Montoro, *IEEE J. Solid-State Circuits*, 33, 1510 (1998).
3. C. Galup-Montoro, M.C. Schneider, and A.I.A. Cunha, in *Low-Voltage/Low-Power Integrated Circuits and Systems* E. Sánchez-Sinencio and A. Andreou, Editors, p.7, IEEE Press, 1999.
4. H. S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, *Solid-State Electronics,* 30, 953 (1987).
5. A.I.A. Cunha, M.C. Schneider, C. Galup-Montoro, C.D.C. Caetano and M.B. Machado, *in Symposium on Microelectronics Technology and Devices/2004*, E. J. P. Santos, R. P. Ribas and J. Swart, Editors, PV 2004-03 p. 69 The Electrochemical Society Proceedings Series, Pennington, NJ (2004).
6. Y. Tsividis and G. Massetti, *IEEE Trans. CAD*, 3, 72 (1984).